Results of Radiation Test of Cathode Front-end Board in the CMS Endcap Muon System

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Reported by T.Y. Ling
LEB 2000
Radiation Levels in Endcap Muon

Calculations by M. Huhtinen

Integrated over 10 LHC years
(5x10^7 s at 10^{34} cm^{-2}s^{-1})

**Neutron Fluence (>100 keV):** (0.02 - 6) x 10^{11} cm^{-2}
**Total Ionizing Dose:** (0.007 - 1.8) kRad
Test Requirements

• Since all *on-chamber* ASIC’s and COTS are the same for all chambers, they should survive the worst-case radiation environment. (Use calculated levels times a safety factor of 3)

• Expose ASIC’s COTS on CFEB to radiation
  – Measure SEE (SEU and SEL) cross sections for COTS and ASIC’s. Use the measurements to predict SEE rates for neutron fluence of $2 \times 10^{12} \text{ cm}^{-2}$
  – Measure degradation of analog performance for ASIC’s due to TID effects up to a dose of 5 kRad
  – Measure degradation of analog performance due to displacement damage of *bipolar* for an equivalent neutron fluence of $2 \times 10^{12} \text{ cm}^{-2}$
Modeling and Calculations by Huhtinen and Faccio shows:

- At LHC environment SEU dominated by high energy hadrons (>20 MeV)
- For these energies, SEU cross section ~independent of particle type and energy

**Measure SEU Xection using 60-200 Mev proton beam**

<table>
<thead>
<tr>
<th></th>
<th>63 MeV Protons (UC Davis)</th>
<th>1 MeV Neutrons (Ohio State)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMOS Devices</strong></td>
<td>SEU, SEL, TID</td>
<td></td>
</tr>
<tr>
<td><strong>Bipolars Devices</strong></td>
<td>SEU, SEL, TID</td>
<td>Displacement</td>
</tr>
</tbody>
</table>
Cathode Front-end Board

- Preamp-shaper ASIC
- SCA ASIC
- Comparator ASIC
- Control FPGA (XILINX Spartan XCS30XL)
- CPLD (XILINX XC9536XL)
- MUX FPGA (XILINX Spartan XCS30XL)
- ADC
- Channel Links

Dimensions:
- 11.5" height
- 7" width
Test Setup

- Beam collimated to irradiate one ASIC or COTS at a time
- Readout data through DAQ chain intended for the “final” system

63 MeV proton beam
Preamp-shaper ASIC

- No single event latch-up for proton fluence of $2.28 \times 10^{12} \text{ p/cm}^2$
- No shift register errors
- Gain decreases by factor of 2.8, from 0-300 Krams (~ 2 hr run). Not a problem at LHC rates.
- No change in amplifier noise 0-30 kRad.
Switched Capacitor Array ASIC

- No single event latch-up for proton fluence of $1.7 \times 10^{12}$ p/cm$^2$
- No degradation of analog performance
- Slight decrease in digitized pulse height vs dose due to output amp gain drop. Not a problem at LHC rates.
- Negligible change in noise and pedestal 0 - 10 kRad.
Comparator ASIC

- No single event latch-up for proton fluence of $1.1 \times 10^{12} \text{ p/cm}^2$
- Shift of thresholds and offsets < 0.4 mV
ADC

- No single event latch-up for proton fluence of $2.7 \times 10^{11}$ p/cm$^2$
- No degradation of performance
**Readout Controller FPGA**

**XILINX Spartan XCS30XL**

Irradiation: $9.9 \times 10^{10}$ p/cm$^2$

(2 runs; TID=13.4 Krads)

- No Single Event Latch-up.
- Capacitor block numbers predicted and checked with blocks numbers read back.
- SCA read/write addresses read back and checked.
- 27 Errors detected. All are recoverable by reloading FPGA.
  - 70% of these errors associated with a change in configuration memory. For these, only 1 in 16 configuration memory changes related to observed controller error
- **SEU cross section** $= 2.7 \times 10^{-10}$ cm$^2$
XILINX Spartan XCS30XL
Irradiation: $2.86 \times 10^{11}$ p/cm$^2$
(6 runs; TID=38.1 Krads)

- No Single Event Latch-up
- 34 MUX controller errors detected. All recoverable by reloading FPGA. (70% of these errors associated with a change in configuration memory.)
- SEU cross section = $1.2 \times 10^{-10}$ cm$^2$
- Configuration errors occurs after 13.3 Krad and increase drastically after 23 Krad. These are not cleared by reset, but do not effect controller functioning.
- 5th run stops when MUX quit working (35.7 Krad). The same chip recovers after 2 hours.
XILINX CPLD XC9536XL

**Chip 1:** $2.8 \times 10^{11}$ p/cm$^2$ (3 runs; TID=37.8 Krads)
- No Single Event Latch-up
- No configuration errors
- 106 errors detected. All recoverable by reload.
- Chip died after exposed to 42.7 Krads

**Chip 2:** $3.1 \times 10^{11}$ p/cm$^2$ (2 runs; TID= 41.3Krads)
- No Single Event Latch-up
- No configuration errors
- 117 errors detected. All recoverable by reload.

SEU cross section = $3.8 \times 10^{-10}$ cm$^2$
XILINX Virtex XCV50
Irradiation: $9.3 \times 10^{10} \text{ p/cm}^2$
(5 runs; TID=12.5 Krads)

- No Single Event Latch-up.
- Capacitor block numbers predicted and checked w/ blocks numbers read back.
- SCA read/write addresses read back and checked.
- 16 Errors detected. All are recoverable by reloading FPGA.
- SEU cross section $= 1.7 \times 10^{-10} \text{ cm}^2$
## Summary of SEU Measurements

<table>
<thead>
<tr>
<th>Device (Function)</th>
<th>Proton Fluence (10^{11} \text{ cm}^{-2})</th>
<th>Dosage (kRad)</th>
<th>Number of SEU's</th>
<th>SEU Xection (10^{-10} \text{ cm}^{2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>XILINX Spartan XCS30XL (Readout Controller)</td>
<td>1.0</td>
<td>13.4</td>
<td>27</td>
<td>2.7</td>
</tr>
<tr>
<td>XILINX Spartan XCS30XL (Multiplexer)</td>
<td>2.9</td>
<td>38.1</td>
<td>34</td>
<td>1.2</td>
</tr>
<tr>
<td>XILINX CPLD XC9536XL (Chip 1)</td>
<td>2.8</td>
<td>37.8</td>
<td>106</td>
<td>3.8</td>
</tr>
<tr>
<td>XILINX CPLD XC9536XL (Chip 2)</td>
<td>3.1</td>
<td>41.3</td>
<td>117</td>
<td></td>
</tr>
<tr>
<td>XILINX Virtex XCV50 (Readout Controller &amp; MUX)</td>
<td>0.9</td>
<td>12.5</td>
<td>16</td>
<td>1.7</td>
</tr>
<tr>
<td>Channel Link Receiver</td>
<td>14.8</td>
<td>200</td>
<td>277</td>
<td>1.9</td>
</tr>
<tr>
<td>Channel Link Transmitter</td>
<td>14.8</td>
<td>200</td>
<td>1023</td>
<td>6.9</td>
</tr>
</tbody>
</table>
Irradiated with 1 MeV neutrons at OSU
Fluence = $2.8 \times 10^{12} / \text{cm}^2$
Following devices passed the test
- LM1117-adj (adjustable voltage regulator)
- LM4120-3.3 (voltage reference; 3.3 V, 5 mA)
- LM4120-1.8 (voltage reference; 1.8 V, 5 mA)
- LM4041 (shunt voltage reference)
- SDA321 (Diode Array – reversed biased)
- Red LED
- AD8011 (300 MHz Current Feedback OpAmp)

Need a rad-tolerant 2.5 V regulator
  - Good candidate identified. Need to be tested.
Conclusions

- **Cumulative effects**
  - **Total ionization dosage (with 63 MeV protons)**
    - No deterioration of analog performance up to 10 krad for all three CMOS ASIC’s
    - All FPGA’s survive beyond dosage of 30 krad
  - **Displacement damage (with 2x10^{12} cm^{-2} n’s @ 1 MeV)**
    - Usable voltage regulators and references identified
    - Protection diodes OK

- **Single-Event Effects**
  - No latch-up for all ASIC’s up to 2x10^{12} p cm^{-2}
  - **Single Event Upset (SEU)**
    - Cross sections measured for all FPGA’s, C-Links.
    - All SEU’s in recoverable by reloading FPGA’s