DAQMBM

CMS CSC DAQ Motherboard Control FPGA
Data Readout, Trigger Controller

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210
DAQMB Control FPGA Design

This FPGA coordinate the LCT, L1ACC signals, Control DATA transfer from CFEB, LCT/TMB to DDU. And CFEB calibration

Modification history:
- Nov. 2, 2000: Redesign the FPGA logic, based on the new DAQMB PCB design, GU
- Nov. 16, 2000: Finished first iteration design
- Feb. 2, 2001: Move the design from m:\wv\d741mbc\ to m:\wv\cmsdaqmb\daqmbc\
- Mar. 9, 2001: Major modifications, targeted device: XCV200E-FG456
- Apr. 11, 2001: Loc pins according to PCB design
- Aug. 1, 2001: Optimization of the design
- Aug. 7, 2001: Modify the design to talk to Giga-bit Ethernet card
- Aug. 30, 2001: Invert all the CCB related GTLP signals, because the CCB use inverted logic
- Sept. 19, 2001: Add the CFEB data transfer error detection
- Dec. 4, 2001: Add the Random Trigger, Trigger Rate Settable
For TLK2501, use 40MHz clock to generate 80MHz clock, CLKGEN1
For TLK2201, use external clock as GLINK clock, CLKGEN2
L1LATENCY[5:0] Set by JTAG. Fixed for fixed peripheral crate setup.
For LCT delay, 500ns, L1Acc delay 3.2us, not to be
Minimize the LCT & L1Acc delay on DAQMB.

For other LEDs, refer to page 2D.

For LCT delay 500ns, L1Acc delay 3.2us, set to 0F.

TRGDLY[1:0] is the fine delay
TRGDLY0 is used to adjust the LCT/L1Acc phase relative to CFEB clock.
TRGDLY1 is used to adjust the cable length 0 for 4-8m, 1 for 9m and longer.

TRGDLY1: One clock cycle delay, TRGDLY0: half clock cycle delay

TRGOUT[1:0] is the fine delay
For other LEDs, refer to page 2D.

For LCT delay 500ns, L1Acc delay 3.2us, set to 0F.
Block Diagram of Serial Flash Memory Interface
DAQ Motherboard Controller
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DAQMBC
GU 1
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MBCCTRL .4
2C
Block Diagram of CCB fast control

From the other FPGA

Global Reset for CFEBs

L1Release to CCB

CCBCODE

CCBCMD[5:0]

CMOSTR PB

CCBDATA[7:0]

DATASTR PB

CLKCMS CLKENA

L1ARST L1ARST INC

RESET

SOFTRST

CCBCMDSTRB

CCBDATASTRB

CCBCMD0 CCBCMD1 CCBCMD2 CCBCMD3 CCBCMD4 CCBCMD5 CCBCMD6 CCBCMD7

CCBDATA0 CCBDATA1 CCBDATA2 CCBDATA3 CCBDATA4 CCBDATA5 CCBDATA6 CCBDATA7

CCBDATA7 CCBDATA6 CCBDATA5 CCBDATA4 CCBDATA3 CCBDATA2 CCBDATA1 CCBDATA0

DCBA
For TLK2201, use external 62.5MHz clock as Glink clock.
This IFD_1 is just used to sync with the Fake backplane, should do the change at Fake BP
Use IFD for real backplane to replace the IFD_1 and FD here
LCT delay for the length of L1 Latency, and take into account of one clock cycle uncertainty to match with L1ACC
Total delay: (2350 + 750*delay5 + 375*delay4 + 200*delay3 + 100*delay2 + 50*delay1 + 25*delay0) ns

set the Delay as 011000, so the delay of mid-one is 29025ns, to match with current CFEB --Jan. 2, 2002
L1 FIFO push delay relative to L1ACC (100ns -- 850ns)
Total Delay: (100 + 375*dly4 + 200*dly3 + 100*dly2 + 50*dly1 + 25*dly0) ns
Program procedure:

PROGRAM command: 82H, (MSB first), Page Address 5, Byte Address 5
Shift in 32-bits (command + Address) while PADDR6 low, PADDR7 high
Shift in 32-bit data, Paddr6 high, Paddr7 high
Disable Clock when Paddr7 low

This Order is Reversed because bit0 read first, while command needs MSB first

SERFMEM:0 Load Cable Delay fine adjustment to Register
SERFMEM:1 Load DAQMB Board ID to register
SERFMEM:2 LOADID Load the register into Flash Memory
SERFMEM:3 PROGRAM Program the Serial Flash Memory, or Load the register into Flash Memory
SERFMEM:4 LOADFEB Clock Delay to Register
(Save for future use)
SERFMEM:5 LOADCMP Initialize the Cable delay detection logic, and reset the fine delay to 0
SERFMEM:6 REGTRG Save the Trigger (LCT/L1ACC) delay
SERFMEM:7 REGCABLE Save the Cable Length related delay
SERFMEM:8 LOADFEB Refresh the on-board CFEB clock delay register
SERFMEM:9 SFMRESET Reset the Serial Flash Memory
LOADINX must not be less than one CLKCMS cycle
Reason for this: The data come out of SFM, and save in FPGA using the same clock.

Here, the Bit30 as shift back from READ_SFM.
SFM Reading Header

Read Procedure: (needs about 7us)
Read Command: 52H, same page and byte address as PROGRAM
Reset, Delay 400ns, while RADDR6 low and RADDR7 low
Shift in 32 bits command and Address, while RADDR6 high and RADDR7 low
Shift in 32 Dummy bits, while RADDR6 low and RADDR7 high
Shift in/out 32 data bits, information, while RADDR6 high and RADDR7 high
Cable Delay detection procedure:
- Send INIT (SERFM5), to initialize FFs, and fine delay
- Load CFEB Clock Delay (SERFM2) at the nominal setting
- Update the CFEB clock delay setting (SERFM6) on the external register
- Trigger, send matched LIACC and LCT to CFEB3, either pulse or inject
- Latch the Trigger (LCT/LIACC) fine delay, REGTRGDLY (SERFM6)
- Update the fine delay (SERFM0) inside the FPGA
- Trigger, same as previous step
- Latch the Cable length-related fine delay, REGCABLE (SERFM7)
- Update the fine delay (SERFM0) inside the FPGA
- Reprogram the Serial Flash Memory

Comment: INIT will also set fine delays and other delays to a default value 000

Adjust this according to CFEB FPGA delay and maximum cable length delay to 111 on BIT[2:0]
Instruction Code: (8 bits, on SEL1)
00: NO-OPERATION (Page 50)
01: JTAG Reset (page 50)
02: Global Reset (page 50)
03: BUCKEYE Inject (page 58)
04: BUCKEYE Pulse (page 58)
05: Pedestal data taking (page 58)
06: Load Trigger Register (page 57)
07: Cycle Trigger Register Once (page 57)
08: Continuously Cycle Trigger Register (page 57)
09: Load CFEB Register (page 59)
0A: DAQMB Status (page 55)
0B: Trigger select in cal_mode (page 50)
0C: FIFO manual read control (page 52)
0D: CAM Delay Setting (page 56)
0E: FIFO Master Reset and GLINK Reset (page 50)
0F: Load DAQMB Crate ID (page 53)
10: Load CFEB Clock Delay (page 53)
11: Set Calibration timing (Calib Pulse Delay) (page 54)
12: Set Loop Back for Glink, toggling (page 70)
13: Load Random Trigger Frequency
14: Toggle Random trigger start control
15: Serial Flash Memory (page 40s)
16: ...
1F: Serial Flash Memory (page 40s)
20: Burst 1000 (really 512+256+128) Random events (L1ACC)
**Title**
The Ohio State University
Physics Department Electronics Lab
174 West 18th Ave, Columbus OH 43210

**Diagram**
Combination first, Register later to eliminate possible Instruction Glitches
decode first 15 OpCodes (4.5 bits)

**Diagram Description**
- **8 Bit Instruction Register**
  - SEL1
  - SHIFT
  - BTDI
  - CE
  - AL
  - D7

- **JTAG Instruction Decode**
  - NDHIGH
  - D0
  - D1
  - D2
  - D3
  - F7
  - F15
  - F1
  - F2
  - F3
  - F4
  - F5
  - F6
  - F8
  - F9
  - F10
  - F11
  - F12
  - F13
  - F14

- **DAQ Motherboard Controller**
  - DDHIGH
  - DDLOW
  - SEL1
  - UPDATE
  - NDHIGH
  - D0
  - D1
  - D2
  - D3

**Additional Notes**
- CMS CSC Electronics
- DAQ Motherboard Controller
- DAQMBC
- GU
- INSTRGDC
- Pages 50-51
- 1.14.2002_16:36
Do combination first, register later to eliminate possible instruction glitches

decode second 16 OpCodes (4.5 bits)
Check Status LOGIC (F10)
Check Status LOGIC (F10)
Check Status LOGIC (F10)
CAL_LCT_1 delay: 475ns + 25ns*CALLCTDLY[3:0]

CAL_GTRG delay: 3075ns + 375ns*CALGDLY4 + 25ns*CALGDLY[3:0]
LCT2SEL[3:1]  Trigger Rate (KHz)
7  620
6  310
5  160
4  80
3  40
2  20
1  10
0   0

CFEB1 LCT
BUSY mean event read

Delay the Busy for several clock cycles to wait for Block RAM data.
There is no need to disable DAV for fifo6 and fifo7, because the CLCT write to FIFO in double-word, and overlap FIFO is already filled with data.
To Overlap FIFO, This is a duplicate output of DOUT[15:0] to minimize the 80MHz Bus length
12 bit comparator, try to minimize the logic level.

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