D741FEB

CMS CSC Cathode Front End Board  Control Logic

SCA, Mux and Fast data transfer control
Design goal: CFEB control, SCA addressing, Data transfer

Revision history: Mar. 7, 2000: Combined the logic D741F(XC9536XL), D741G(XCS30XL) and D741H(XCS30XL) together
  Apr. 20, 2000, Refine the timing, logic for production version
  Apr. 25, 2000, Modify PREBLKEND logic
  June 12, 2000, Modify LCT and GTRG synch logic to accept 50ns signal
  June 20, 2000, Using VOTE logic to mitigate the radiation SEU
  July 14, 2000, Modified the MUX part to disable OE by DATALOAD
  Aug. 2, 2000, Modified the timing for 40MHz, 20MHz hybrid
  Aug. 8, 2000, Modified the ADC Clock, SCA write clock, so the external delay can be minimized, only one 1ns step delay needed
  Oct. 10, 2000, Add the Comparator Reset and Double the Comparator clock, re-arrange the pinout

RESET must last 800ns or longer
MUX150 must synchronize with OE[6:1]
The standard output setting are Fast 12mA. For other setting, there may be extra delay.
DATA transfer controller

SENDCHECK is a hand-wired positive logic signal from SCAM.
FPGA Multiplexer
The Six ADC inputs latched by 150ns clock,
Output latched by 25ns clock

Device virtex version
CHECKPUSH is controlled by OE2 at 150ns.
Checksum must be on the bus during OE3 (OE2 in MUX).
ADCCLK goes high when OE2 goes true here (also OE1 goes true in MUX).
ADCCLK goes low when OE5 goes true here (also OE4 goes true in MUX).

Assume that RST from FPGA comes (or goes) when C50NS goes high.

ADC and Clock Control
Cathode Front End Board
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ADC and Clock Control
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Reset the clock to synchronize the CLK50 with Motherboard CLK50

ADC clock generator

SCAM150

75ns delay

FD

25ns delay

FD

25ns delay

FD

6ns delay

OFD_1

SCA Write clock generator
Removable, but be careful!
It won't hurt to keep it...
CRC-15 check, Primitive Polynomial: $X^{15}+X+1$

For CRC-15 correctable logic, see this page
CRC-15 Primitive Polynomial: $X^{15}+X+1$
Bus $S[2:0]$ is the primary state machine of the device. PREBLOCKEND is the reference used to determine which blocks belong to the LCT. It is also used in READCONTROL to determine which blocks are saved for digitization.

Do not free addresses on EFLG!!
This will test if there is a write during read in the same block.
Choose NBASELVS for Vijay's Priority scheme.
Choose NBASELB for Ben's Priority scheme.
NOTE: LOW ON SEL WILL PASS THROUGH D0
Blocks 9,11,13,15 are always marked busy.
W[3:0] and DO[3:0] and DDO[3:0] go out of block

Must be reset to ZERO!

800ns LCT latency

400ns LCT latency

VKS

W[3:0] and DO[3:0] and DDO[3:0] go out of block

Must be reset to ZERO!
Will count 0 1 3 2 6 7 5 4 when up is high
Will count 4 5 7 6 2 3 1 0 when up is low
In TRIGREG: synchronize LCT and GTRG signals. Also pipeline LCT for 2400ns GTRG latency and generate MATCH signal (dataavail).
Then determine MATCHed LCT times relative to BLOCKEND and store in LCT Register DLCT[7:0].
Finally, write DLCT and SCA-BLOCKADR in FIFO3 and pop FIFO1. Free the block in NBADR if NOGTRG.
Delayed LCT Register.

The position of STATES on this loop depends on the total GTRG delay relative to LCT, that is the total delay length on page 71 plus the MATCH delay.
LCT is synchronized in DAQMB

Global Trigger Synchronized at DAQMB, Matching with pipelined LCT.
First part of LCT Pipeline, 875ns.
Second part of LCT Pipeline, 1050ns.
Second part of LCT Pipeline, 975ns.
Fifo3 stores LCT timing & SCA block number for blocks with matching triggers.
XCHECK causes checksum to be sent. It goes true on OE5==OEN4 in MUX

Changed delay time of PUSH and LASTWORD to MBRD
Changed from 16 samples to 8 samples, needs checked 12/11/98

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SCA Readout
SCA Controller
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VKS 40
D741FEB

READOUT 1
Lct0 is the first time-ordered LCT bin in the block. Lct7 is the last bin in a block. Serialized bits are written to memory lowest bit first!
Will count 0 1 3 2 6 7 5 4 when up is high
Will count 4 5 7 6 2 3 1 0 when up is low
JTAG Instruction Decode

OpCode | Function [OpName] |
-------|------------------|
0      | No Operation [NOOP] |
1      | SCAM Reset [] |
2      | Check CFEB status, Capture and shift |
3      | Check CFEB status, shift only |
4      | Program Comparator DAC [] |

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<tr>
<th>OpCode</th>
<th>Function [OpName]</th>
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8      | Load PRE_BLOCK_END |
9      | Load COMPARATOR mode and time |
10     | BUCKEYE mask, default 111111 |
11     | BUCKEYE shift in/shift out |

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**JTAG Signals**
- BTDI
- DRCK1
- DRCK2
- SELECT1
- SELECT2
- TDI
- TDO
- UPDATE
- SHIFT

**SCA Controller**
- LOADPREBLK
- LOADPREBLK[1:0]
- LOADPBLK END
- LOADPBLK[1:0]
- STAT_MON
- STAT[20:0]
- SEL[1:0]
- SEL2
- STATUS[20:0]
- TDO[16:0]
- TDOF[16:0]
- TDOFAB2
- TDOF4
- TDOF8
- TDOF10
- TDOF12
- TDOF24
- RAW0

**INSTRGDC**
- F0
- F1
- F2
- F3
- F4
- F5
- F6
- F7
- F8
- F9
- F10
- F11

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JTAG Signals
SCA Controller
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D741FEB
Check Status LOGIC (F2), shift test (F3)
Load Programmable Delay Bits
SCA Controller
CMS CSC Electronics