DMB6VME

--- VME interface FPGA design for DAQME version 8, production

CMS CSC DAQ Motherboard VME interface FPGA

VME interface and Slow control

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DAQMB VME interface FPGA Design
This FPGA do the slow control for CFEB and DAQMB by VME --> JTAG, or direct VME command
Modification history:
  Mar. 11, 2003: Copy from DMBS2V
  July 30, 2003: Replaced the CLKMAX and CLKMON in P50s and P80s by SLOWCLK and CLKMAX and CLKMON as CEs
  Sept. 29, 2003: Modify the Data Bus enable logic. May need further check
FastCLK: 40MHz
MidCLK: 10MHz
SlowCLK: 2.5MHz
SlowCLK2: 1.25MHz

Fastclk is in phase with Midclk, but they are not in phase with Slowclk. PROMs and ADCs use slowclk. Controller FPGA and DAC use Midclk.
CFEB JTAG Clock: 1.25MHz, which is controlled by ENABLE.
The DAC can work at 10MHz, FPGA can work at 33MHz, PROM can work at 10MHz, but it can only be Re-programmed at about 1.25MHz
The guess number for BUCKEYE is 5MHz
DAQMB Controller FPGA JTAG Clock: 10MHz, which is synchronized with MIDCLK
The FPGA can work at 33MHz, the Serial Flash Memory can work at 20MHz
DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK
The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz
The ISP does not work at 2.5MHz or faster

Both FPGA and CPLD will drive VPROM's JTAG line, tri-state when not in use
Serial ADC (MAX1270/1271) Interface clock: 1.25MHz, Divided SLOWCLOCK is used
The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz
Serial DAC (MAX5154/5155) interface clock: 5MHz

The MAX 5154/5155 requires the minimum clock period is 100ns.
Flash Memory clock: SLOWCLK2, which is 1.25MHz. There is a timer inside using this clock.

Comment: CFEB clock: 2.5MHz in normal JTAG mode.

For AT29LV256, call FLASH29LV256
For AT49BV512, call FLASH49BV512
DTACK for Load Instruction/Data Register command
CFEB Selection and Readback logic

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CFEBs JTAG control
DAQMB VME Interface
CMS CSC Electronics

GU    2A
DATE   20C
FILE   8-29-2001_14:03

DAQMBV

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CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register
08 || Write CFEB Select Register
09 || Read CFEB Select Register
CFEB JTAG commands:

- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register

DAQMB Control FPGA JTAG command Decoder

DAQMB VME Interface

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DAQMB Controller FPGA’s PROM JTAG control
DAQMB VME Interface
CMS CSC Electronics

GU 2C
DESCRIPT DMB6VME

DATE 3-11-2003_14:18
FILE CPROMJTAG .1
PAGE 40
CFEB JTAG command decode

- **00** Shift data, no header, no tailer
- **01** Shift data with header only
- **02** Shift data with tailer only
- **03** Shift data with header and tailer
- **04**
- **05** Read TDO register
- **06** Reset JTAG State machine
- **07** Shift Instruction register
DTACK for Load Instruction/Data Register command
CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register
Title

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Serial ADC Interface MAX1271
DAQMB VME Interface
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GU 2D PARENT PAGE
FILE
PAGE
PROJECT
7-30-2003_10:03
SERADC_150
Burr-Brown ADS7809, or Analog Devices AD9777 interface logic

Procedure:
- Pull BBBCONV low for 400ns after VME command, then go back high. Disable the counter.
- After ADC BUSY go low to high, send another BBBCONV low for 400ns, and enable the counter.
- At same time disable the BUSYSHOT. After 16 Clock cycles, set DTACK low to indicate Data Ready.
- Reset the DTACK after VME Address changed, the BB Read cycle ends.
Serial ADC Selection and Readback Logic

- ADC Selection and Readback
- DAQMB VME Interface
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ADC Selection and Readback
DAQMB VME Interface
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GU 2D
SUBJECT DMB6VME

3-11-2003_14:20 SERADC .3 50B
CFEB JTAG command decode

Serial ADC Command Decoder:
00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 || Read Data Back from Burr-Brown Register
04 ||
05 ||
06 ||
08 || Write Serial ADC Chip Select Register
09 || Read Serial ADC Chip Select Register
Parallel FIFO Read/Write Command Decoder:

- **00**: Write to FIFO, 00 for LastWord/Overlap (no last, no overlap)
- **01**: Write to FIFO, 01 for LastWord/Overlap (last, no overlap)
- **02**: Write to FIFO, 10 for LastWord/Overlap (no last, overlap)
- **03**: Write to FIFO, 11 for LastWord/Overlap (last and overlap)
- **04**: Read low order 16 bits, no FIFO read counter Increment
- **05**: Read low order 16 bits, and FIFO read counter Increment
- **06**: Read high order 2 bits, no FIFO read counter Increment
- **07**: Read high order 2 bits, and FIFO read counter Increment
- **08**: Write FIFO Select Register, (more than 1 FIFO can be enabled)
- **09**: Read FIFO Select Register, just to check 08 function
- **11**: Just Increment FIFO Read Counter
Serial ADC Selection and Readback Logic
Serial ADC Command Decoder:
- 00 || Write Control Byte to MAX1271's
- 01 || Read Data Back from 1271 Register
- 02 ||
- 03 || Write Low Voltage Power Register
- 05 || Read Low Voltage Power Register
- 06 ||
- 07 ||
- 08 || Write Low Voltage Monitoring Serial ADC Chip Select Register
- 09 || Read Low Voltage Monitoring Serial ADC Chip Select Register
It takes 10sec to erase the flash memory
Erase timing: Load six command, and wait for 10 Sec.

Address

-WE
-CE
OE

Data
Because the program happens on ~WE edge, the glitch on A/D lines do not matter.

Program timing:

- Address: 10ns
- Data: >100ns
- ~WE: >10ns
- PCOUNTs: >100ns
- TIMEs: 100ns
- SLOWCLK: 100B

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Flash Memory, Program the memory
DAQMB VME Interface
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GU 21
DMB6VME

3-21-2003_15:20 FLASH49BV512 .3 100B
Be careful to generate the Buckeye load data stream.

Bit 0 is the TMS, normally stay 0; set 1 for the very last bit and 1 for two extra bits
Bit[1:5] is the Buckeye bit stream for CFEB[1:5], put 2 extra bit at the end to properly end the JTAG data load

This includes shift in 111111 to enable all six buckeyes.

The Data files for Buckeye shift:

Bit 0: TMS: 0 0 0 1 1 0 0 0 ...... 0 0
Bit 1: TD1: x x x 0 a b c ...... y z Buckeye shift in bits for CFEB1, totally 288 + 3 + 2
Bit 3: TD3: x x x 0 a b c ...... y z Buckeye shift in bits for CFEB3, totally 288 + 3 + 2
Bit 4: TD4: x x x 0 a b c ...... y z Buckeye shift in bits for CFEB4, totally 288 + 3 + 2
Bit 5: TD5: x x x 0 a b c ...... y z Buckeye shift in bits for CFEB5, totally 288 + 3 + 2
Bit 6 and 7: Do not care

Data file Byte: 0 0 0 1 1 0 0 0 ...... 0 0 Low order byte first
CFEB JTAG commands:
00 || Initialize PROGRAM process
01 || Load in BUCKEYE pattern
02 || Program data to Flash Memory
03 || Read back Flash Memory
04 || Initialize Buckeye
05 || Erase the Flash Memory

Working process
INITIAL: to initialize the counters and ready for Load block RAM
LOADBUF: one byte each time, bit0: TMS, usually 0; bit[5:1]: Buckeye shift pattern for CFEB[5:1]
READFM: optional to check the Block RAM content
PROGRAM: Load the Block RAM into Flash Memory
BUCKEYE: Shift in Buckeye patterns by Flash Memory
Para-Out Shift Reg w/ Enable & Async Clr

Spartan2 Family SR16CRE Macro, Right Shift 16-Bit Loadable Ser/Para-In, right shift 1, Modified from XILINX, SR16CLE

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