DAQMBP

CMS CSC DAQ Motherboard PCB Schematic

PRODUCTION

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DAQMB, It check and concentrate the DATA (CFEB, CLCT/TMB/ALCT) from one chamber, and then send to DDU

Oct. 23, 2000: Modify the design based on m:\vdl741\rev3\, an intermediary design
Nov. 1, 2000: The new scheme is ready, need update the CCB link, and CLCT/TMB link, and possibly CLCT/TMB FIFO.
Nov. 2, 2000: Preliminary design is ready. Need feedback from Dan, and coordination with UCLA, Rice and Florida for backplane
Dec. 6, 2000: Double checked the signals by feedbacks from FPGA design
Jan. 18, 2001: Modify the ADC design, use three MAX1271, and one ADS7809/AD977
Jan. 22, 2001: Modify the Backplane interface design. For CCB, use GTLP/LVTTL transceiver, TMB, use FPGA GTLP property
Feb. 7, 2001: Modify according to backplane PCB design, Add Flash Ram
Feb. 14, 2001: Double check, and modify the VME interface and "emergency" handling
Feb. 26, 2001: Further check, Changed the DAC to MAX5154
Mar. 5, 2001: Add TLK2501/1501 for GLINK, and Changed the Temperature ADC Refs
July 3, 2001: Modifications by the Rev3 PCB debug
Mar. 12, 2002: Use radiation-tolerant part, like the SHARP regulator.
Dec. 17, 2002: Add one fifo for ALCT data, change the TMB fifo to 18-bit wide; using AT49BV512 flash memory
Jan. 10, 2003: Add the termination for clock signals
June, July, 2003: Modify the resister values, and add a clock driver for FPGA gigabit clock
Sept. 24, 2003: Finalize the Parallel Flash memory, added an inductor for +5V.
Sept. 25, 2003: Final check on the schematics for production of ten boards
Keep Channel Link and buffers close to FIFOs

End flag
FEB Error Flag
Usually Overlap

Serial SCAM data

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip. Shared by the two 16827s.
Need PULL-DOWNS on:
  Lastword, Eflag, OEN, read_one
Need PULL-UPS on:
  Overlap, rst, f_rst, kill_dav, dav, empty_f*
Keep Channel Link and buffers close to FIFOs

End Flag
FEB Error Flag
Usually OVERLAP
Serial SCAM Data

Three filter CAPs per power pin on Channel Link:

Otherwise, one filter CAP per power pin, one TANT per chip.

F2 Input/Output
Keep Channel Link and buffers close to FIFOs.

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip.
Keep Channel Link and buffers close to FIFOs

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip.

10H
Fifo F5
TMB Data Fifo

Fifo F6
Dan: Put the clock driver very close to the Oscillator and TLK2501 to minimize the GLCLK trace length.

For 821

For Flash Memory

Dan: Delete the extra filter Caps according to your layout. Only 16 0.1uf are needed.

Dan: There are some power pins on the edge of the chip. For VCCO: 2 4.7u, 1 0.1u per bank.
These are the functions if the LVDB monitor uses 6 ADCs.

Could be 100 Ohm

Default mode setting
Connect all the signals on this page to FPGA
For pin compatible with different FPGA, use IO** pins
Do the same trick as before, so that one is enabled and the other is disabled.
NOTE: All high speed serial lines must be smooth, no right angles and no layer changes.
TMB[14:0]: CLCT/TMB data to 18-bit fifo
TMB[29:15]: Additional CLCT/TMB data to 36-bit fifo
TMB30: DDU special word flag
TMB31: Last word flag bit
TMB32: 40MHz clock to write to FIFO
TMB33: Fifo write-enable inverted
Span[7:1]: Used to exchange information in CFEV calibration mode
Dan: The two parallel 100Ω is used to replace one 50Ω.