DCC3STX

CMS EMU DCC (rev3) Data Transmit FPGA

Through this FPGA, DCC communicate data with S-Link64
DCCSTX Design: This is the DCC to SLINK interface FPGA design. It receives ten DDUs, and sends to two (or one) Slink64.

The maximum data rate for each input FIFO is 150MHz at 36-bit wide, as fake DDR; the output is 75MHz at 72bit wide.

This FPGA can also talk directly to computer through the Gigabit Ethernet Interface

Mar. 8, 2005: Copied from DCCSTX, pinout needs be fixed by D785S
Mar. 17, 2005: Put in the pinout information
May 3, 2005: Finalize the pin location, All pins are located, Pin usage 491/556
June 2005: Redo the FIFO readout timing, backpressure logic
Dec. 2005: Add some diagnostic display on the LED, debug the FMM signals, deleted the PROG monitoring signals

BoardID will be stored in INPROM: XDCCYYYX: X is the board ID, 1 to 15, YYY: Date code. Day/2, Month, Year
Example: 2DCC4652: DCC board #2, Date: 2005, June, either 8th or 9th
Clock distribution

DCC <-> SLINK data interface FPGA

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Input FIFO and Output FIFO separately

Reset FIFO's data (FIFO Partial Reset) just before TRGSTART for a clean start

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TTCrx interface
DCC <-> SLINK data interface FPGA
CMS CSC Electronics
One-shot for every SLINK active

Output of the one-shot, (not shown) which are the data flow control information.
Design consideration:

- **CLK12C**: approximately 4MHz from DCM. The TTCrx I2C interface gets ~1MHz clock.

- When the DCM ok, shift in controller register of TTCrx. One bit per four clock cycles.

- Address: 0101010W  Data: 00000011
- Address: 0101011W  Data: 01111000

- Data to be shifted to TTCrx:
  - I2C stop: Data change from Low to High when CLK high
  - I2C start: Data change from High to Low when CLK high

- **I2C TTCrx initialization on Hard reset**:
  - 12C start: Data change from High to Low when CLK high
  - 12C stop: Data change from Low to High when CLK high
Device code:
00 This FPGA itself, XC2VP20-FF896
01  
02  This FPGA's PROMs, two XC18V04-VQ44 and/or one XCF32P
03  Input FPGA's PROM, XCF18V02-VO44
04  Input FPGA, middle one of the five xc2vp2
05  First Slink JTAG interface
06  Second Slink JTAG interface
07  TTCs I2C interface
08  Temp, voltage monitoring ADC
09 Emergency PROM Programming, Reserved for discrete logic
Similarly for SLINK's JTAG interface
The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz. Divided SLOWCLOCK is used.

The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz.
DTACK for Load Instruction/Data Register command
Serial ADC Command Decoder:
00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 ||
04 ||
05 ||
06 ||
08 ||
09 ||

CFEB JTAG command decode

DTACK for Load Instruction/Data Register command
CFEB JTAG commands:

- **00 **Writeln to I2C: Shift data and supply clock, it is a VME WRITE
- **01 **Read from I2C: Receive data and supply clock, but it is a VME WRITE
- **02 **VME Read: No I2C activity, put data on VME backplane
- **03 **
- **04 **
CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register
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CFEB JTAG command decode

VME→JTAG for data input FPGA's PROM
DCC Slink Interface FPGA
CMS CSC Electronics
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06 || Reset JTAG State machine
07 || Shift Instruction register
VME Registers:
00 || TTCrx Command Bus
01 || Read Status, Low 16 bits
02 || Read Status, High 16 bits
03 || Load FIFO_In_Use register, to mask off the no_DDU_input FIFOs
04 || Generate Fake L1A
05 || Read back TTC_Cmd
06 || Read back fifo in use
07 || software switch, and force TTC 'not ready'.
08 || Force FMM states
5A || Reset TTCrx
1X || Read back Date Rate Monitor

TTCrx Reset, it will last for many us
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VME registers, FPGA status monitoring
DCC Slink Interface FPGA
CMS CSC Electronics

1-26-2007 15:00
VMEREG 3 19B
The DATA[15:0] to control the L1A generation mode. L1A generation will auto stop. Internal BUSY will delay further VME command.

Data[15:8]: The L1A frequency control. Data[7:0]: Total number of L1As, if Data7=1, no stop.

Always trigger one event at least.
The Clock Phase needs be adjusted

DDFR FIFO Read

DTBD[71:68] is used for SLINK64 user bits?

FFIN39: Last Word bit, used in page 20E

one channel has too many words. One channel empty, other not, for too long
DDU status, will be stored in the SLINK tail2

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DDU data status
DCC Slink FPGA
CMS CSC Electronics

GU  2C,2D  3-18-2005 16:03
DCCSTX  SLINK  2  20A
Because the input FPGA will make sure every event has data in the FIFO with proper format, there is no need to check the data format, the readout can be simplified, but need check FIFO_USE

There are two modes to readout the FIFO data: (the default is mode 1, and it switches to mode 2 upon VME)
Mode one: For normal data taking, this is controlled by L1A, MODE = LOW
Mode two: This is controlled by fifo not-empty, mainly for calibration, or L1A is not available, MODE = HIGH

Event number counter: This duplication will detect if the L1A buffer ever overflow

Orbit number, assuming that the BC0 will only last for one CMS clock cycle, and comes every...

Sync L1A to CLKFIFO, L1AFF

New event processing stops at ~PAF, resumes at ~HF, during this time, the current event is finished with remaining data dumped
When \text{BUFEOVFL} is true, this is a serious error, the event readout is corrupted.

When \text{BUFNEMPTY} is true, there are events in the buffer to be read out.

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**S-link64 data format**

<table>
<thead>
<tr>
<th>63</th>
<th>60</th>
<th>59</th>
<th>56</th>
<th>55</th>
<th>32</th>
<th>31</th>
<th>20</th>
<th>19</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>K</td>
<td>BOE_1</td>
<td>Evt_ty</td>
<td>LV1_id (24)</td>
<td>BX_id (12)</td>
<td>Source_id (10+2)</td>
<td>FOV</td>
<td>Hx</td>
<td>$ $</td>
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<tr>
<td>K</td>
<td>BOE_2</td>
<td>Orbit number [55:24] (32)</td>
<td>Hx</td>
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<tr>
<td>K</td>
<td>EOE_2</td>
<td>Evt_length(24)</td>
<td>CRC(16)</td>
<td>Evt_stat(8)</td>
<td>Tx</td>
<td>$ $</td>
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<tr>
<td>K</td>
<td>EOE_1</td>
<td>xxx</td>
<td>Evt_typ: 0001 for normal physics trigger, 0010 for calibration trigger</td>
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**DDDR fifo bookkeeping, buffer size counter**

**DCC Slink FPGA**

**CMS CSC Electronics**

---

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The fifo is written as 71 bit wide

Make up the SLINK64 header and trailer

The Ohio State University
Physic Department Electronics Lab
174 West 18th Ave, Columbus OH 43210

Title: DDR fifo read and Slink fifo write control
DCC Slink FPGA
CMS CSC Electronics

GU 2C2D PAGE BY DATE FILE
12-26-2006 15:04 SLINK 6 20E
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDR fifo read control
DCC Slink FPGA
CMS CSC Electronics

GU: 2C,2D
REVC: DCCSTX
DATE: 1-31-2006 13:27
SLINK: 9
By swapping D0, D1 input, the output clock will be 180 degree shifted.
Spy path for data

Reserved for external use

This will enable the trigger all the times

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If the FIFO stay not empty for more than 1ms, dump the data

Readout logic to Gigabit Ethernet Buffer

Extract Header Information
(Trailer word of SLINK64 package, Bxxx)
BC0 code 0x01

L1 reset code 0x03

Start trigger code 0x06

Orbit Reset code 0x10

Calib code 0x14, 0x15, 0x16

Stop trigger code 0x07

Hard reset code 0x04

Hard reset code 0x34, for DDU only

FDC CALIB lasts for 25ns after CAL commands

Start_trigger code 0x06

Stop_trigger code 0x07

Hard_reset code 0x04

Hard_reset code 0x34, for DDU only
CRC-16 Primitive Polynomial: $X^{16}+X^{15}+X^2+1$, same as USB standard.
Use the following edge of CLKW for CE, to make sure proper register of WA
There may be side-effect that the CMPWA is not current
Para-Out Shift Reg w/ Enable & Async Clr

virtex2p Family SR16CRE Macro, Right Shift

16-Bit Loadable Ser/Para-In, right shift

Modified from XILINX, SR16CLE

Sheet Size: C

Date: 13th January 1993

Title: Para-Out Shift Reg w/ Enable & Async Clr

Ver: A
Rev: 1

Copyright (c) 1993, Xilinx Inc.

drawn by KS
2 to 1 multiplexer with default 0

Title: 2 to 1 Multiplexer
Comments: 2 to 1 Multiplexer
Date: 15th March 1993
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.