D785U
CMS CSC Data Concentrator Card (DCC) PCB Schematic

Version 4

MBRD_BLK

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210
DCC: It Collects 9 DTB data, and sends to CMS main DAQ via one or two S-LINK64 interfaces

June 9, 2003: Initial drawing, June 23, Need more check
June 26, 2003: Power and ground design
July 28, 2003: Copy the project from cmspe003:\wv\vdesign\dccp\ to m:\wv\edm\d785d785g\ July 31, 2003: Added six 100 Ohm resistors for clock termination
Apr. 1, 2004: Modifications according to the ver.1 tests
Apr. 6, 2004: Main FPGA pin re-assignment, and TTC backplane signal switching
Apr. 7, 2004: Change the hard reset logic.
June 15, 2005: Re-arrange the CMS_CLK, and L1A distribution, using 74fct20807 buffer
July 9, 2004: Final check on the schematics, tie FIFO TRST LOW
Jan. 28, 2005: replace the IDT72T40118 with IDT72V36110, start rev3 DCC
Feb. 2, 2005: removed the Program data line LEDs (16 in total)
Feb. 21, 2005: Add buffers for SLINK

Aug. 31, 2005: Added /AS to Emergency Load Logic
Aug. 31, 2005: Changed FMM LED Power from V3PIO to V33P
Aug. 31, 2005: Added thevin terminator to TCMSCLK
Sept, 6, 2005: Added series LED to V5PRAW Front Panel LED
Sept, 6, 2005: Changed V5PRAW, SLDONE, RXDONE LED current limiting resistor to 330Z
Sept, 6, 2005: Added (10) 10uF tantalums to the Analog FPGA 2.5V powers
Sept, 7, 2005: Increased size of P1 Test Port Power Trace
Sept, 7, 2005: Converted all regulator back to the adjustable type (placement and ordering purposes)
Sept, 7, 2005: Added (20) 220nF caps to the input FPGA's
Sept, 7, 2005: Added (7) 220nF caps to the control FPGA

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210
Major changes for rev3:
1. Main FPGA uses V3PIO. 3V compatible IOs
2. Use IDT72V3610 FIFOs, remove the IDT72T40118 fifos
3. Add many test points on the input FPGA
4. Add many monitoring LEDs on the front panel, with 'cable' connection
5. Remove all the in-board LEDs
6. Add a buffer on the input FPGA program lines for monitoring
7. The input FPGA will keep 2.5V IO except one bank will be V33P.
8. Add some aux point on FIFOs if FIFO pins need swapped
9. Add buffers before the SLINK

Minor changes for rev3:
1. the 156.25MHz clock goes to main FPGA
2. Re-arrange the front panel LED position, 8 in between optical transceivers, all the others at top
3. Move the upper SLINK mezz board lower, delete the voltage Keyholes
4. The SLINK mezz cards get separate power supply
5. Add a SLINK Jtag 5-pin connector
DCC layout and minimum signal required for data flow

---

![Diagram showing top-level block diagram of CMS CSC Data Concentrator Card (DCCGU) with various modules and connections.](image-url)
Paralleling the regulator is more complicated.
Set one bank on the FPGA to 3.3VIO (V3PIO), all the others remain 2.5V
Dan: This is to replace the program LEDs for input FPGAs.
The test points are farther away from the PROM.
Fifo Setting
36 bits IN, 36 bits OUT
Fifo Setting
36 bits IN, 36 bits OUT

Fifo Control

- FCTRL0: REN~
- FCTRL1: OE~
- FCTRL2: RCS~
- GCTRL0: MRST~
- GCTRL1: PRST~
- GCTRL2: L1A
- F1CTRL[2:0]: RCS~
- F2CTRL[2:0]: PRST~
- FSEL[1:0]: L1A

Fifo Status

- FSTAT0: F1 Empty~
- FSTAT1: F2 Empty~
- FSTAT2: F1 PAE~
- FSTAT3: F2 PAE~
- FSTAT4: F1 Full~
- FSTAT5: F2 Full~
- FSTAT6: FPGA Status
Fifo Setting
36 bits IN, 36 bits OUT
DIR high: BusA→BusB, so TOVME should be positive logic

The Diode here to maintain (Vcc5 > Vcc3-0.5V) requirement
GROUND POINTS

DISCHARGE UNIT

BOARD STIFFENER

FRONT PANEL MOUNTS

PART FIDUCIALS

Core power for all the six FPGAs

2.5V power for SLINK mezz cards

Aux power for all the FPGAs and Slink FIFOs

Power for FPGAs' IOs, to be adjusted at 3.0V

3.3V power for SLINK mezz cards

1.8V power for VME, 3U Power, Ground, stiffener
Discrete logic to load the VPROM in emergency
Enable these transceivers when there is no TTC available
Use three pads for a pair of resistors. This is used to set the TTCrx ID

Tsadd7: Test mode when 1
Tsadd6: Disable Serial/Parallel Converter when 1

Dan: put these two sets of LEDs in between the optical transceiver

For TTCrx chips

File: TTCrx interface

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
If BAP and BAN is connected on the backplane, the SENSEOUT will be high, or else it will be low.

The bus signals are terminated on both ends of the backplane with 100 Ohm.

The clock signals are terminated on this board and the backplane, except the passive DCC slot.

clock3: slot 3,4,5,6,7; clock5: 8,9,10,11,12,13; clock6: 14,15,16,17; clock4: 18,19,20

(slot 8 is the active DCC, slot 17 is the passive DCC)
Default setting:
72 bits IN, 72 bits OUT
1K as PAE_B, PAF_B
Implement basic S-LINK architecture on DDU board?

Replace these control with S1STAT[4:0] and S1CTRL[4:0]

S1QW[0:1] = 11 FOR 64 BIT TRANSFERS

Not Used on Current LSC

SLINK64 Connector 1
SLINK64 Connector 2 EXT 64

SLINK64/LSC Standoff Holes
Isolated per SLINK Spec pg. 43/62
Default setting:
72 bits IN, 72 bits OUT
1K as PAE_B, PAF_B
Implement basic S-LINK architecture on DDU board?

Replace these control with S2STAT[4:0] and S2CTRL[4:0]

JTAG NOT IMPLEMENTED ON SLINK

SLINK64/LSC Standoff Holes
Isolated per SLINK Spec pg. 43/62

SLINK64 Connector 1
SLINK64 Connector 2 EXT 64

AMP 120521-1

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

Second SLINK INTERFACE
CMS CSC Data Concentrator Card
CMS CSC Electronics