Pre-production Opto-board Status & Plan

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Outline

- Opto-pack measurements
- Soldering jig development
- Opto-board construction status
- Opto-board QA setup & measurements
- Proton irradiation status
- Schedule & plan

VCSEL Opto-Pack Characterization

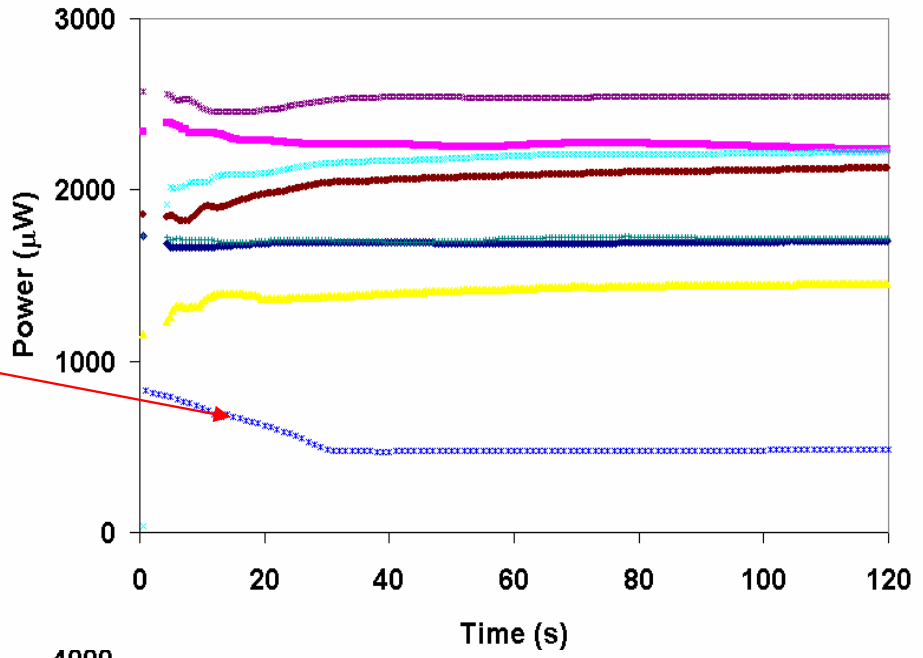
- Measure power vs. time for 120 s to check stability
- Measure power and forward voltage vs. current
  - Require:
    - V_{VCSEL} < 2.1 V at I_{VCSEL} = 10 mA
    - < 40% difference compared to Taiwan power or > 1 mW
  - 22 packs characterized
    - 5 packs on loan from Siegen
    - 2 packs failed the Power vs. Time test
      - One from Siegen
    - 3 packs failed the VCSEL voltage test
      - Two from Siegen
    - 1 pack on opto-board replaced after 3 VCSEL channels died during pre burn-in test
    - 2 packs have cracked ground leads
    - ~50% of packs required large force to mount MT ferrule
    - ➢ ~64% acceptance rate

PIN Opto-pack Characterization

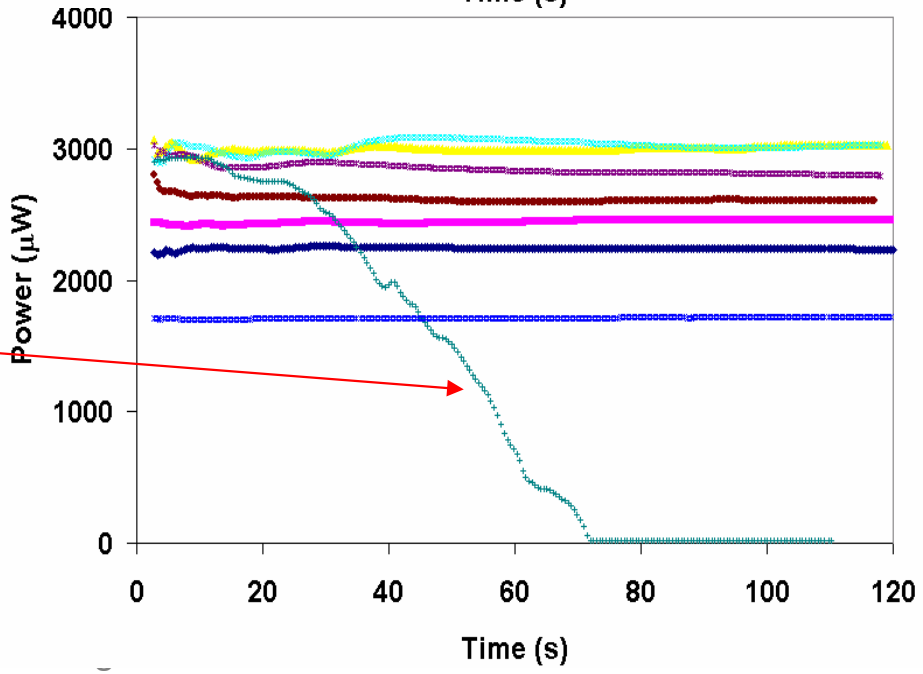
- Measure responsivity
  - Require: Responsivity > 0.5 μA/μW
  - ➢ 19 packs were characterized with none failing
  - ➢ Typical responsivity range 0.5-0.6 μA/μW

Power vs. Time Failures

- Power decreases to ~500 μW after ~25 s



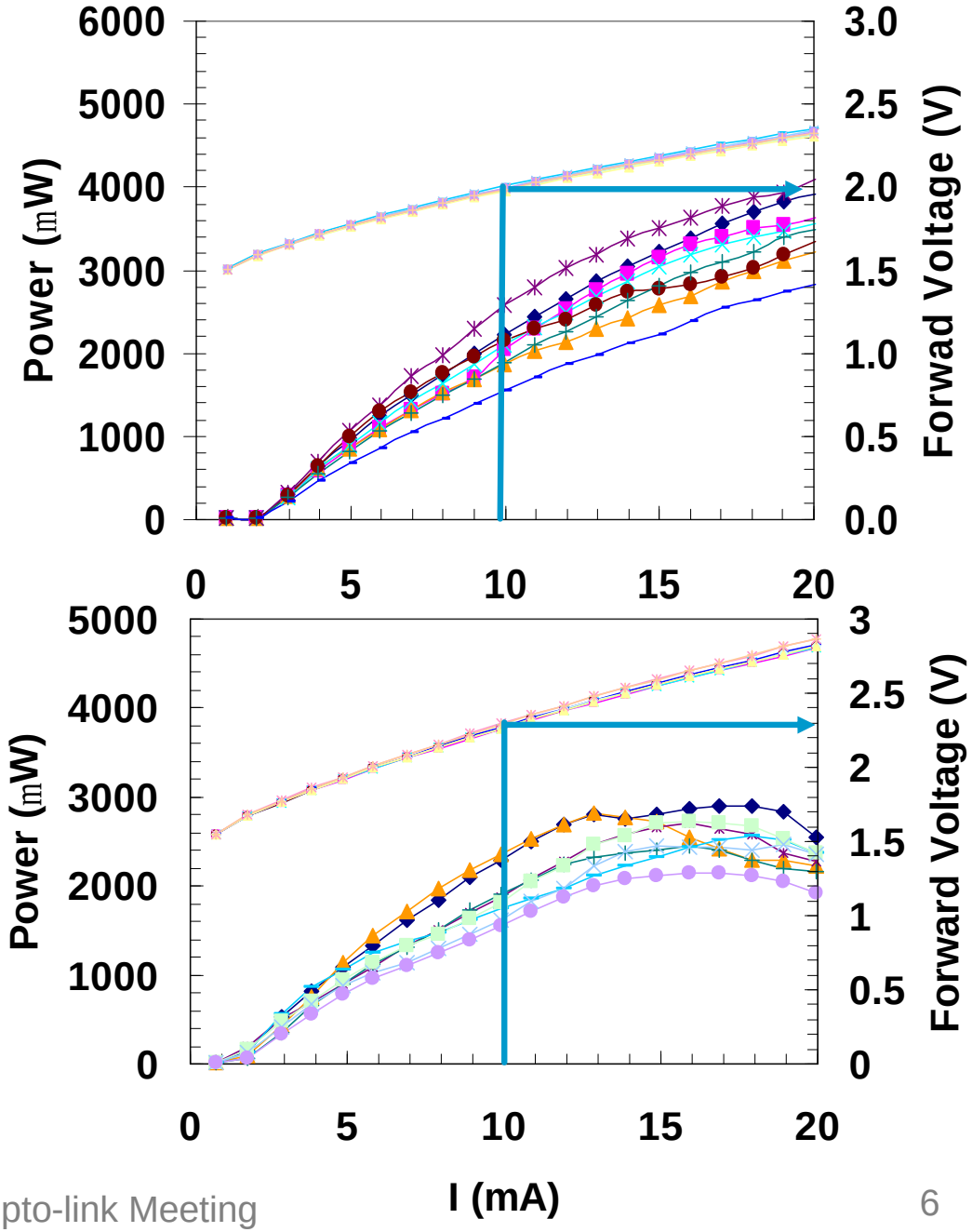
- Power decreases to zero after ~70 s



Power and Voltage vs I_{VCSEL}

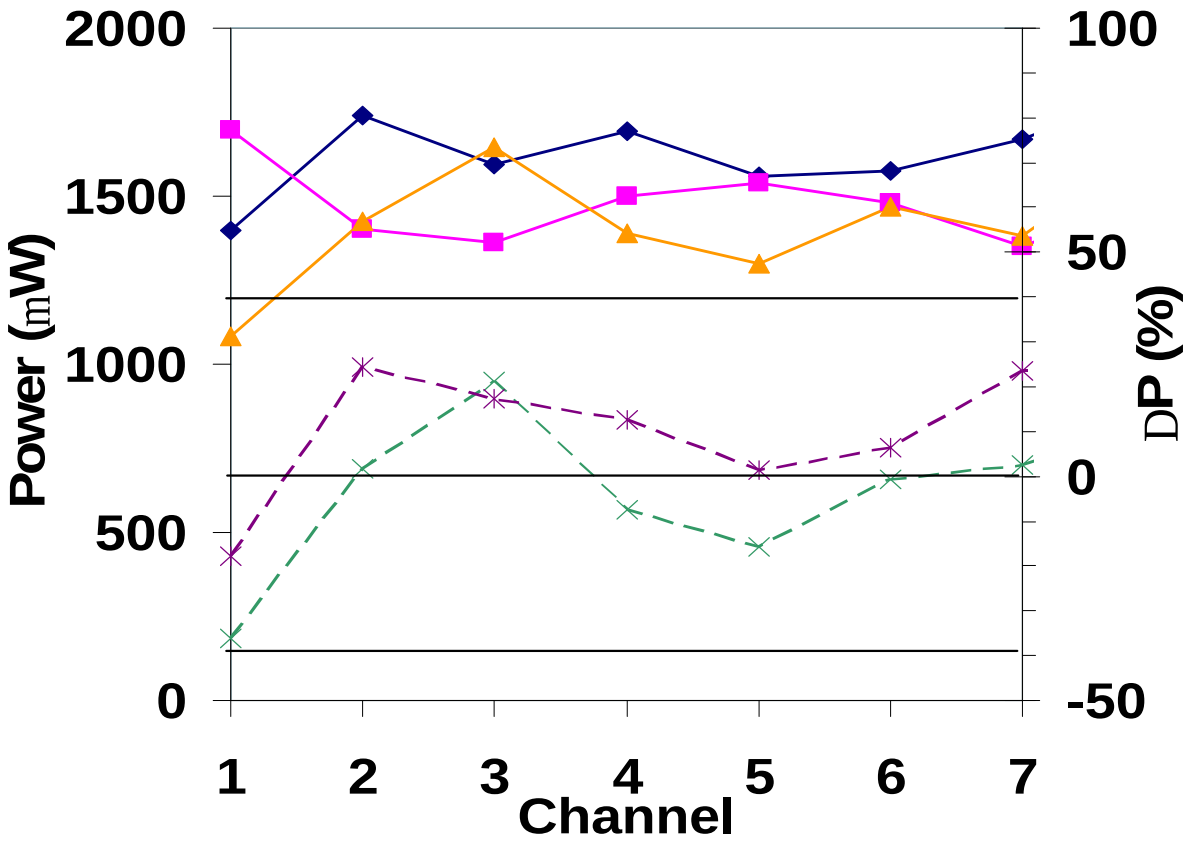
- Good optical power and low forward voltage
  - V_{VCSEL} ~ 2.1 V at 10 mA

- ~200 mV higher forward voltage.
  - V_{VCSEL} ~ 2.3 V at 10 mA
  - Failed the QA



Optical Power QA

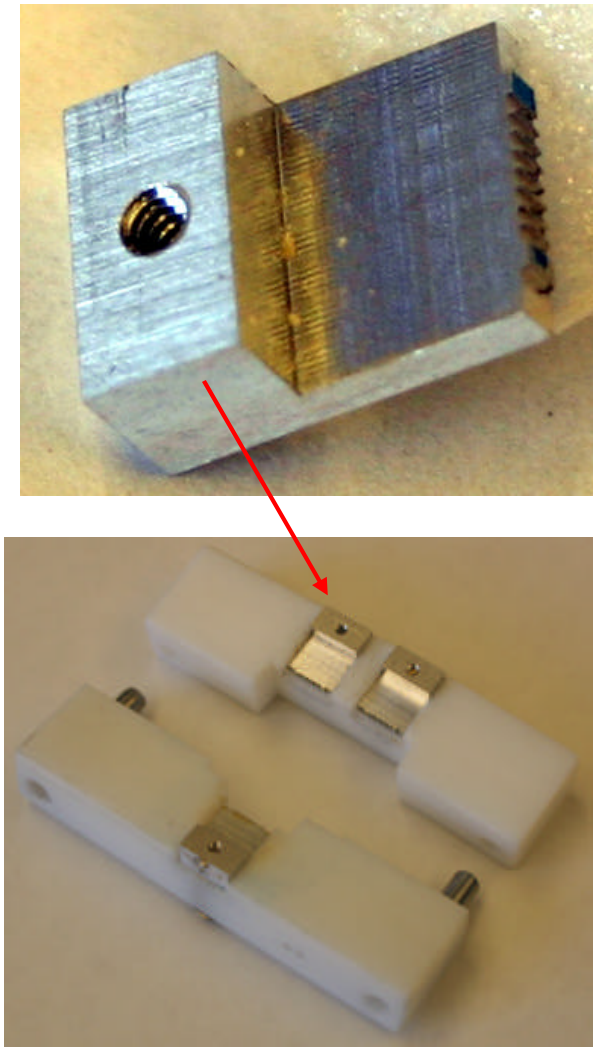
- Compare optical power data from Taiwan, OSU before and after mounting for consistency
  - Require < 40% difference or > 1 mW
  - Good optical power in all opto-boards



- Taiwan
- OSU before mounting
- OSU after mounting
- Power difference between OSU and Taiwan before mounting
- Power difference between OSU and Taiwan after mounting

Soldering Jig Development

- Goal: simultaneous soldering of 10 leads
- 4 design revisions:
  - Teflon jig with flat aluminum blocks
    - Opto-pack leads slid sideway resulting in poor soldering joints and shorts
  - Shorter aluminum blocks with dividers
    - Improve lead alignment
    - Prevent leads from sliding sideway
    - Better heat transfer
  - Modified Teflon jig
    - Allow for better visual alignment of leads before soldering
  - Encapsulate chips/wire bond pads before soldering instead of using Teflon covers to prevent flux contamination



Production Problems/Solutions

- 12 opto-boards at various stages of completion
- Problems encountered:
  - Shorts between opto-pack leads after soldering
    - Added dividers in the aluminum blocks to prevent leads from sliding sideways
  - Cold/open solder joints
    - Decreased the aluminum block length
    - Optimized the soldering time by trial and error
  - Leads detached inside opto-pack
    - Re-soldered leads after removing optical epoxy
  - Ceramic guide pins pulling out when removing ferrule
    - Re-glued the guide pins
    - Large force needed to mount MT connector on some opto-packs
  - Housing clips breaking off
    - Replaced housing
  - Human errors/accidents
    - Broke one opto-board
    - Scratched a chip when removing protective encapsulant
      - Chips machined off
  - Bad chip?
    - Short between power and ground in a DORIC channel
      - Chips machined off

Production Problems/Solutions (Cont.)

- Problems encountered (cont.):
  - Detachments of surface mount devices (resistors/capacitors)
    - 5 detachments (3 opto-boards)
    - US Review: apply 50 gmf to SMD
      - no detachments on ~75 SMD (3 opto-boards) tested
      - 1 more detachment on opto-board with 3 detachments after 190 thermal cycles
    - discussion with vendor on probable cause/solution in progress
    - Reinforce SMD using five-minute epoxy?
    - No detachment of 80-pin connectors on 3 opto-boards after 50 matings
  - VCSELs died after mounting on opto-board
    - Replaced the opto-pack

Connector Alignment

- Bosses on connector: ~620 μm (spec: 600 μm)
- Holes on opto-board: 800 μm as recommended by JAE
  - ➢ Alignment is required in mounting connector
- AA did not align 80-pin connector on opto-board as requested
  - ➢ 8/14 boards failed mechanical tolerance test
- Plan:
  - Reduce hole diameter to 650 μm
  - If holes are undersized or shifted
    - ➢ Slice off bosses and use alignment jig
      - Alignment jig currently under development

Opto-board Construction Status

- 7 boards passed the QA
  - 3 B-layer boards
  - 4 non B-Layer boards
- 2 boards destroyed
- 3 boards in various stages of completion
- Yield: 5/9 = 56% if no chip/opto-pack removal allowed

Estimated Time to Complete an Opto-board

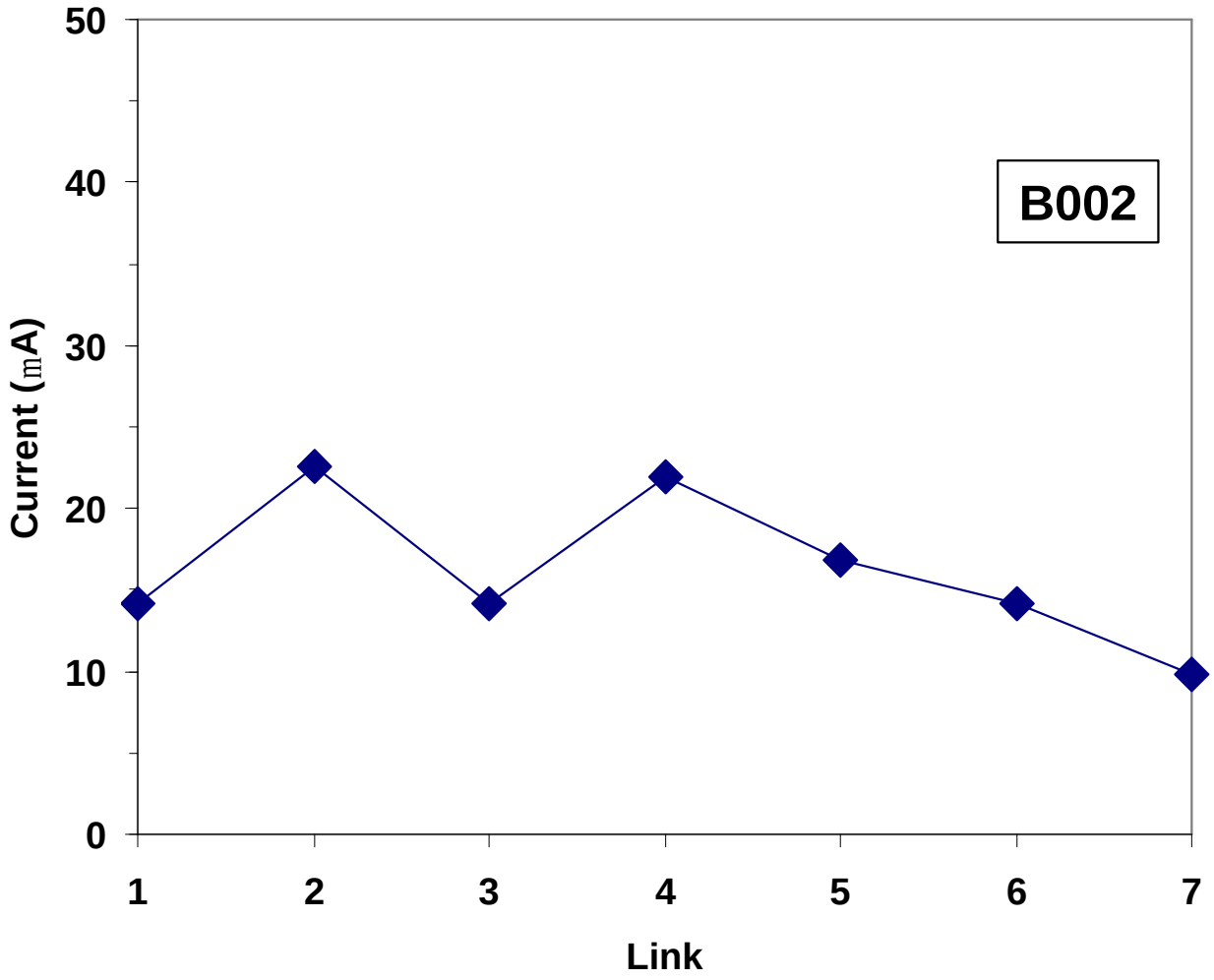
- Construction time: 13 hours
  - 8 man hours
  - 5 curing hours
- Burn-in: 3 days
- Temperature cycling: 17 hours
- QA time: 9 hours
  - 3.5 man hours
    - Optical measurements at -25, 10 and 50^{o}C
    - developing automated optical power measurement
  - 5.5 hours for automated measurement
- Total man hours/board : ~12 hours
- Start to finish: ~6 days

QA Setup

- Hardware and software work for QA are completed
  - Have successfully completed QA for 7 opto-boards using the automated system

PIN Current Thresholds

- Lower limit thresholds for no bit errors are significantly below 40 μA

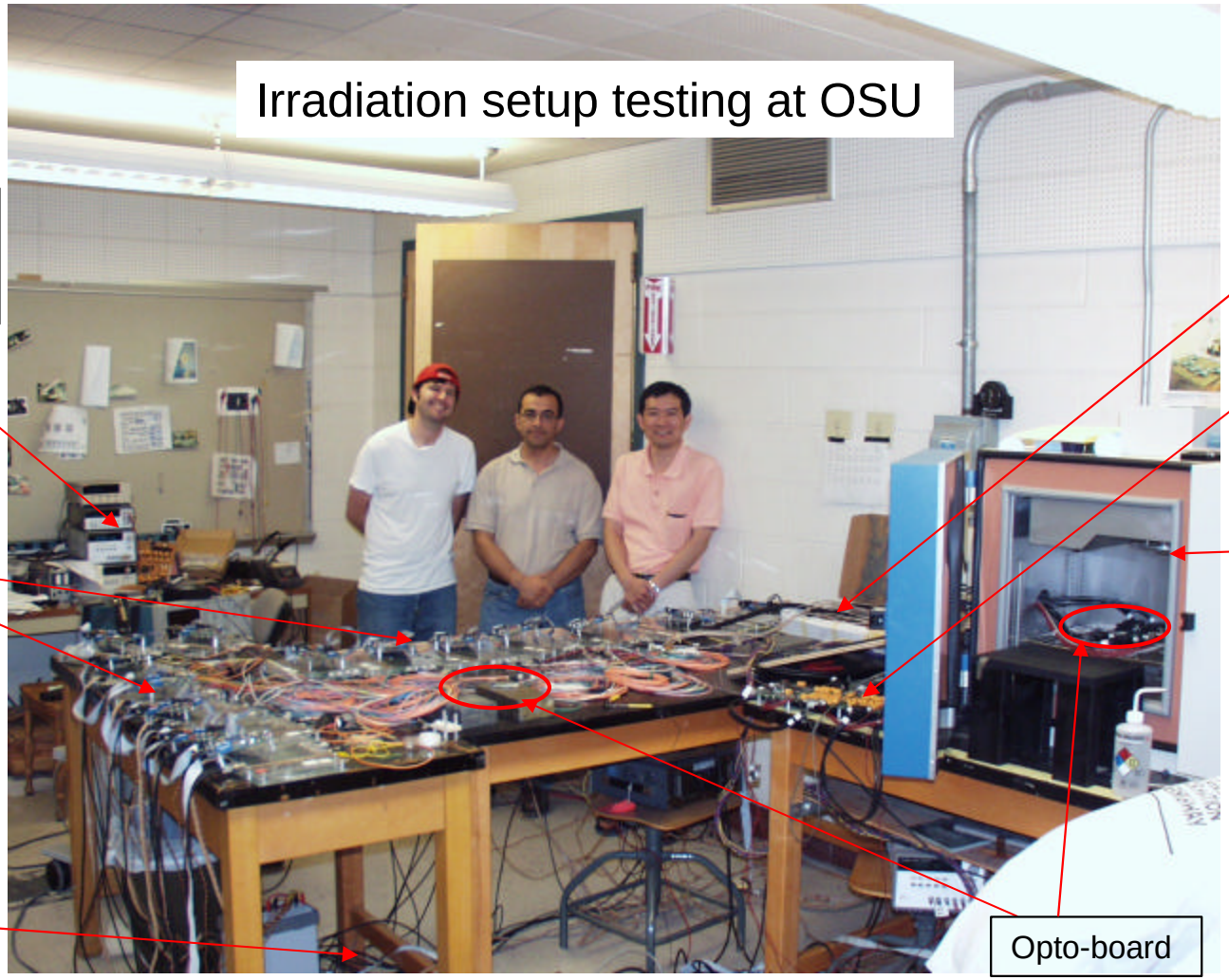


Plan/Schedule

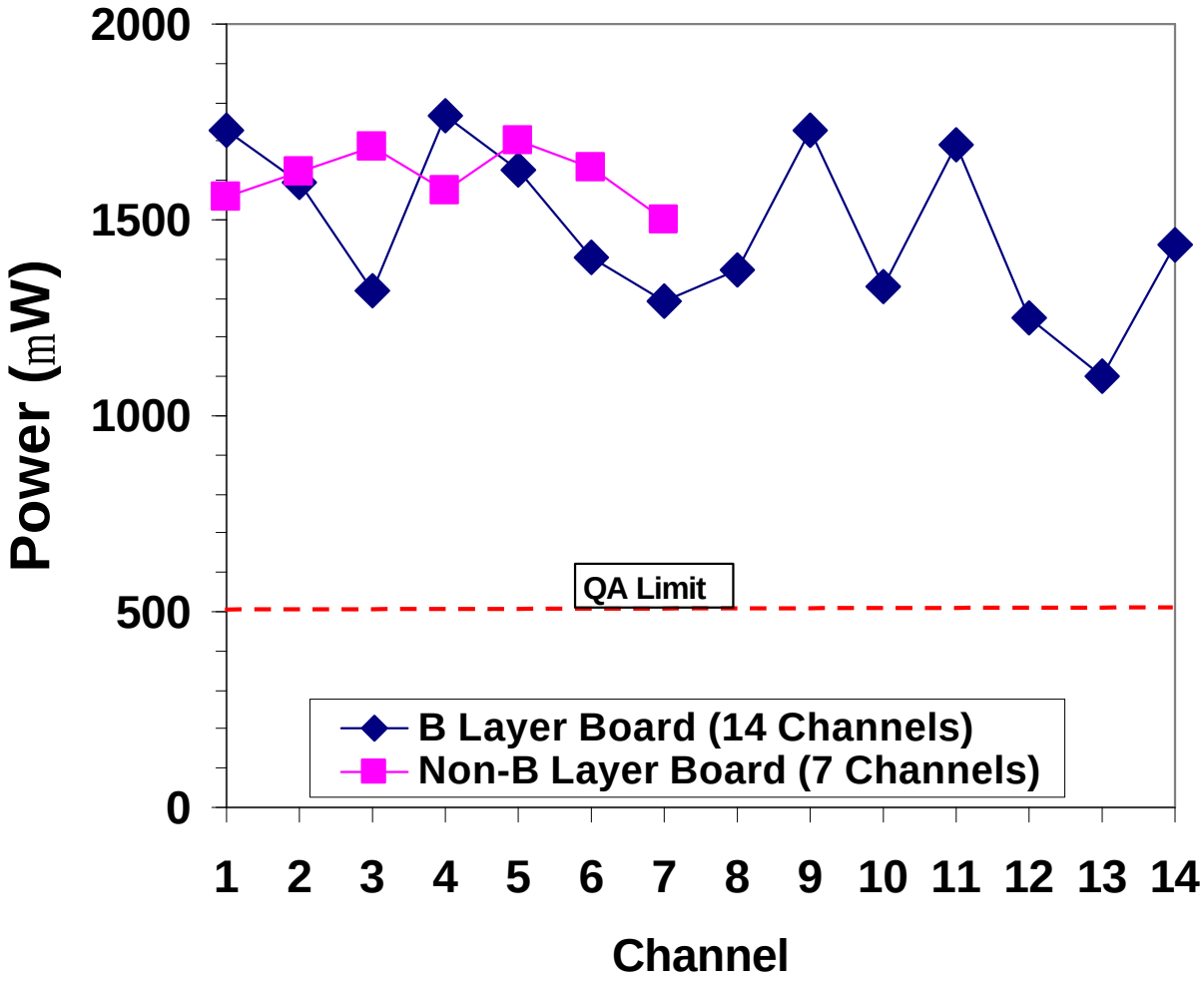
- Fabricate new opto-boards with no layout change needed
- Ordered blank BeO ($6K) already due to long lead time
- Authorize fabrication of BeO boards in July?
- Receive BeO boards in August?
- Estimate production time: 9 months?

June Proton Irradiation

- Setup is ready for beam at T7
- Expect to irradiate 2 B and 2 non B-layer boards using shuttle setup



Optical Power



- The power measured with opto-board mounted on shuttle with the 20 mete fiber
  - Significantly higher power than last year

Summary

- Have characterized all opto-packs
  - VCSEL opto-pack acceptance rate: 64%
- We have procedure for soldering opto-pack leads on BeO
  - Many problems encountered and solved
  - Latest temperature/time combination successfully solder leads on 6 opto-packs (60 leads)
- QA setup is running
  - QA for 7 opto-boards completed
  - Excellent optical power
  - Low PIN current thresholds for no bit errors
- No known problems in opto-board design
- Proton irradiation is ready and will start today