

Summary of Data Bits Passing Through CMS EndCap Muon Motherboard

Based on the discussions at the November 1998 meeting, it is proposed that 2 basic types of events from a given chamber be transmitted by its DAQ motherboard into the DAQ stream (via optical link to the DDU) for each level 1 accept (L1A). This serves as the basis for defining the interface between the MBD and the other boards in the crate.

Typical size in 16 (15 + 1 tag) bit words. The flow of the data in each case is described in the remarks column. 4 or 5 CFEBs per chamber; 3 – 7 AFEBs per chamber.

a) DAQ Event – Occurs for every L1A.

<i>Data kind</i>	<i>Estimated Word Size</i>	<i>Remarks</i>
Header – Event type, L1_id, Chamber_id, BXN, Cathode BXN, Anode BXN, ...	6 - 10	
CLCT data	4/CLCT (56 bits?)	from CLCTB
ALCT data	4/ALCT (56 bits)	from ALCTB
LCT data	4/LCT (?)	from MBT
Cathode Digitized SCA samples, CFEB_id	768 /CFEB (8 time samples)	from CFEB only if CLCT in delayed coincidence with L1A
Anode Latched Discriminator Bits, AFEB_id	30/AFEB (5 time samples)	from AFEB (via ALCTB) only if ALCT in delayed coincidence with L1A

b) Trigger Diagnostic Event – PRESCALED to once per N DAQ Events. *In addition to DAQ Event information:*

<i>Data kind</i>	<i>Estimated Word Size</i>	<i>Remarks</i>
Cathode Comparator output bits	60/CFEB (5 time samples)	from all CFEBs (via CLCTB)
Anode Latched Discriminator bits	30/AFEB (5 time samples)	from all AFEBs (via ALCTB)

Note: Special run **Synchronization Event** (read only DAQ header) occurs when the special run flag is set and LCT found.

Created 11/16/98 – T.Y. Ling (EMU Meeting)

Revised 1/5/99 – P. Nylander