eXtremely Fast Tracker; The Sequel

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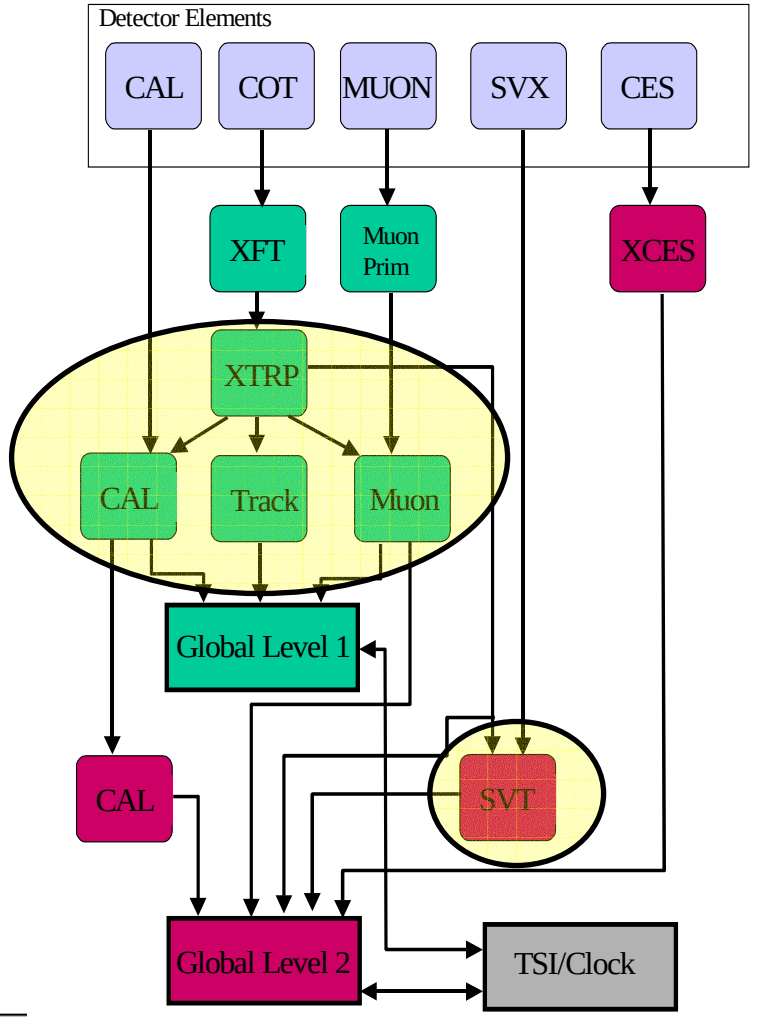
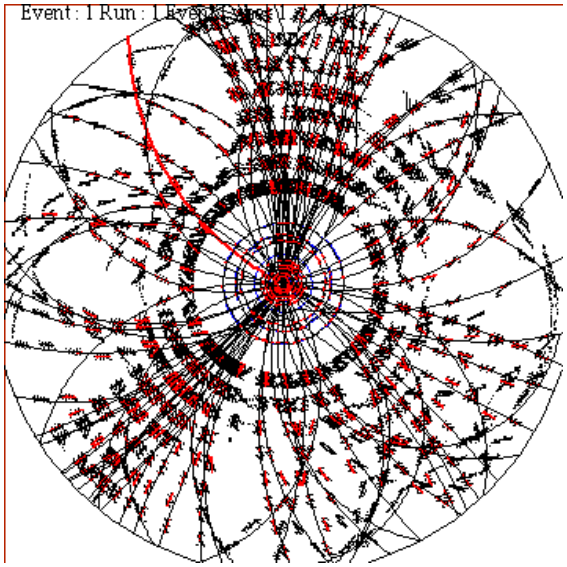
XFT = CDF Level 1 Track Finder

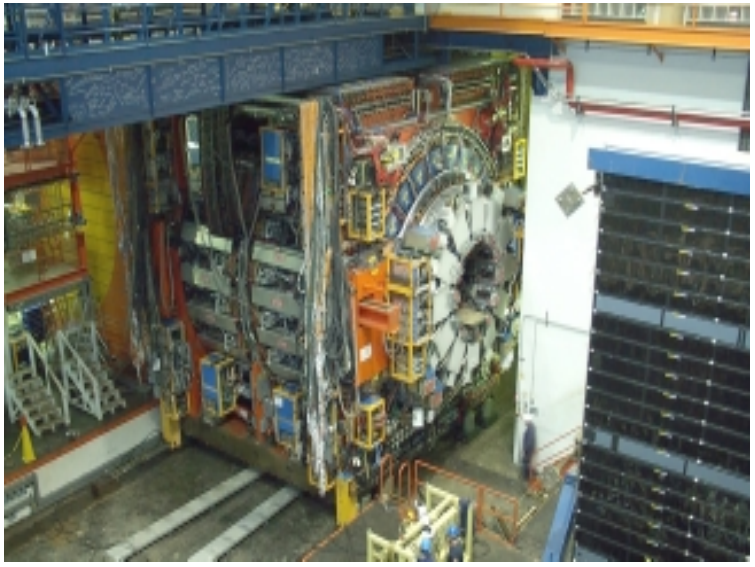
- Role of tracking
  - Top, W/Z, Exotic Physics triggers require High momentum electron and muon **Level 1 trigger** candidates
  - Bottom Physics require low momentum tracking at the **Level 1 trigger**
    - electrons
    - muons
    - hadronic tracks
- L1 Trigger Primitives
  - Electrons: XFT track + EM cluster
  - Muons: XFT track + muon stub
- L2 Trigger Tracks
  - XFT Track + Silicon Hits

CDF Trigger System



CDF Central Outer Tracker (COT)



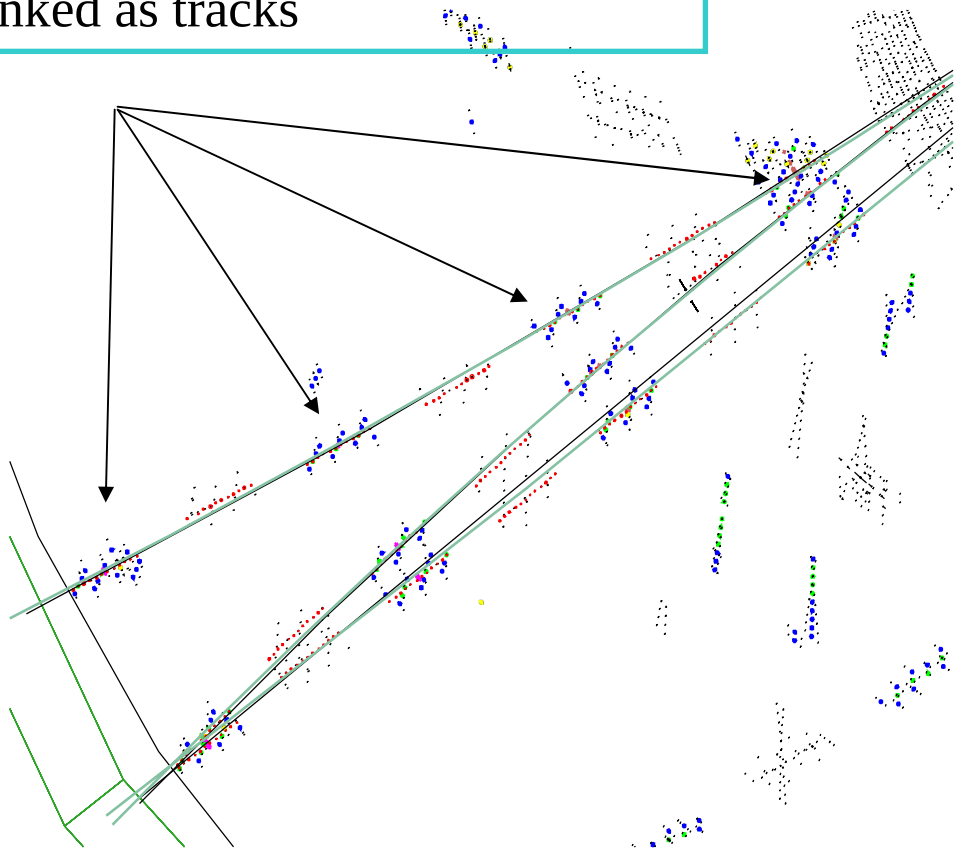


- 8 “superlayers”
  - 4 with axial wires: r - ϕ measurement
  - 4 with stereo wires: z measurement
- Small Cells
  - 0.88 cm drift (avg.)
  - Max drift time ~220 ns
  - 12 sense wires/cell: 96 measurements
  - 2540 cells, 30240 channels

Charged Track Finding

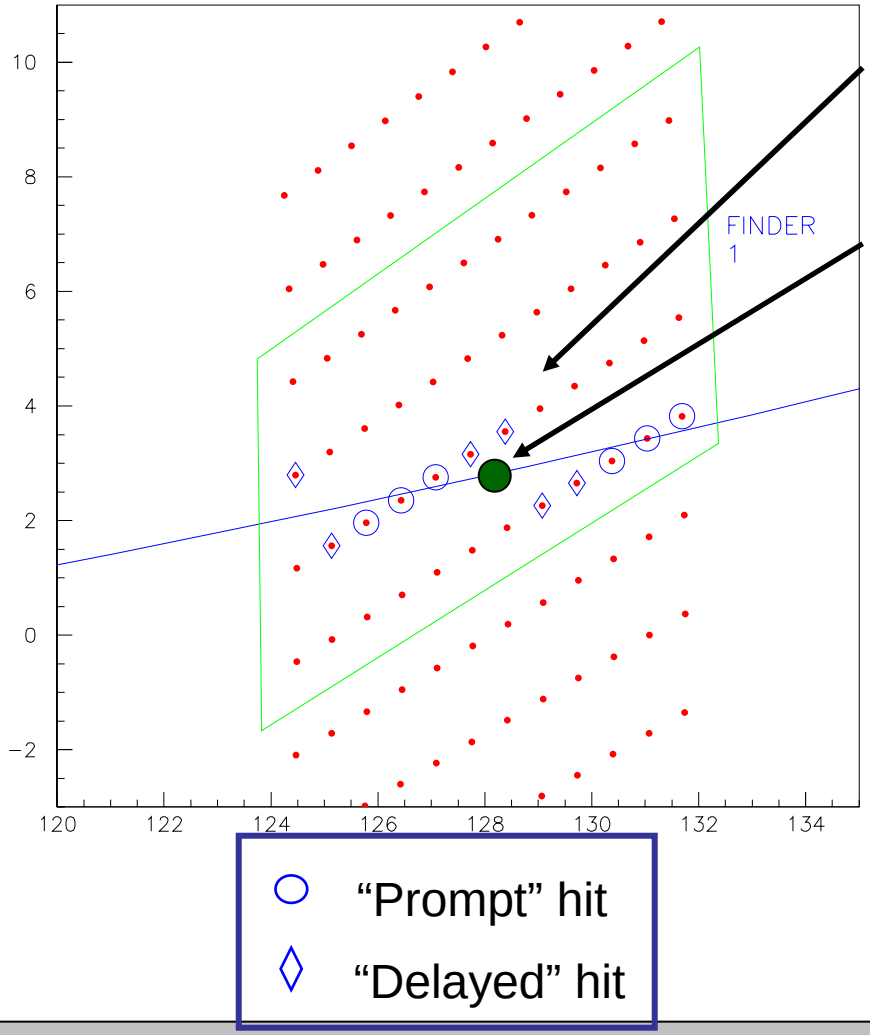
- Hit Finding: Mezzanine Card
  - Hits are classified as prompt or delayed
- Segment Finding
  - In the axial layers, search for patterns of prompt/delayed hits consistent with High Pt tracks
  - Each segment found is assigned a pixel (phi, all layers) and possibly a slope (outer 2 axial layers only)
- Track Finding
  - Looking across 3 or 4 axial layers, search for patterns of segments consistent with Pt>1.5 GeV/c
  - Resultant Pt and Phi of all 1.5 GeV/c tracks sent on to XTRP
  - Maximum of 288 tracks reported
- New Tracks found every 132nsec!
  - eXtremely Fast Tracker: **XFT**

Good hit patterns are identified as segment, then segments are linked as tracks



The Hit and Segment Finders

Track segments are found by comparing hit patterns in a given layer to a list of valid patterns or "**masks**".



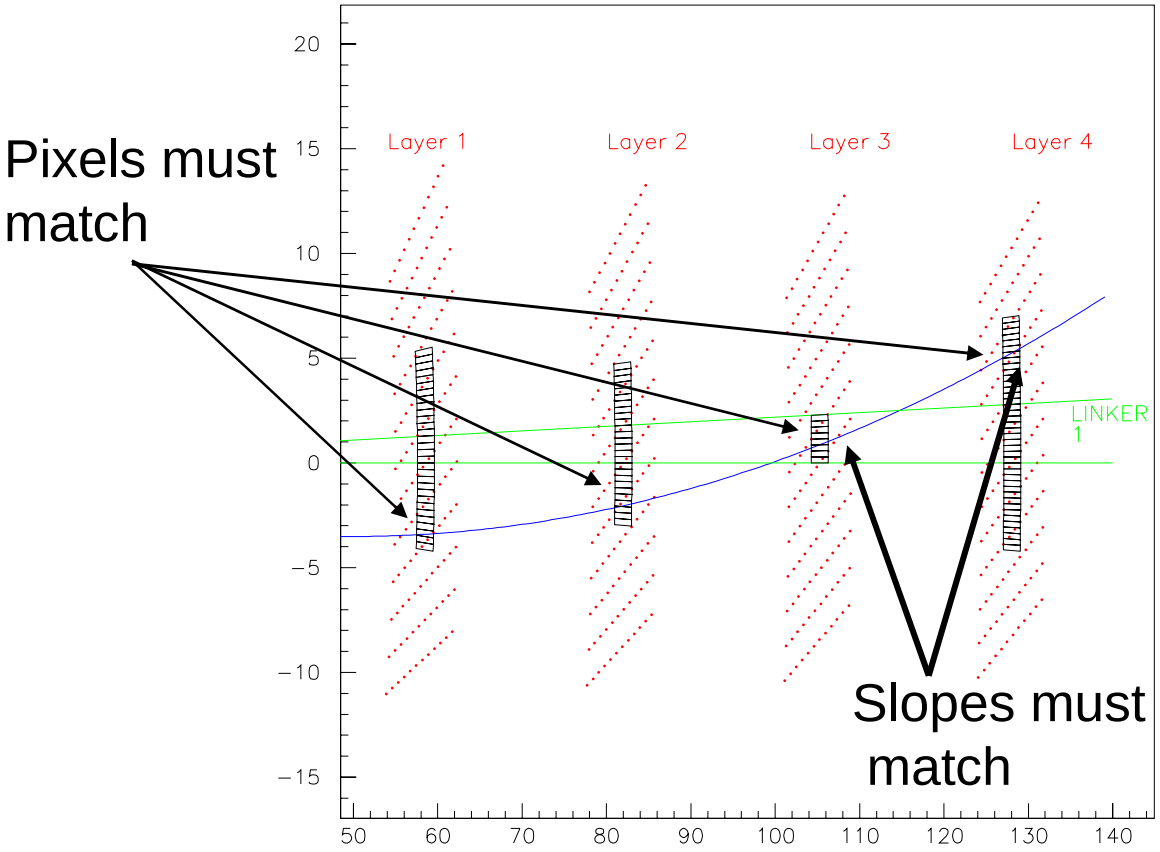
Mask : A specific pattern of prompt and delayed hits on the 12 wires of an axial COT layer

Pixel: represents the **phi** position of the track at the midpoint of the cell.

Layer	Cells	Pixels	Masks
1	192	2304	166
2	288	3456	227
3	384	2304	292
4	480	2880	345

The Linker

Tracks are found by comparing fired **pixels** in all 4 layers to a list of valid **pixel** patterns or "**roads**".



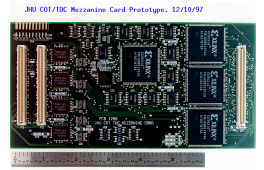
- Chamber is divided into 288 1.25–degree "identical" Linkers
- Each linker uses a look-up table of ~1200 roads

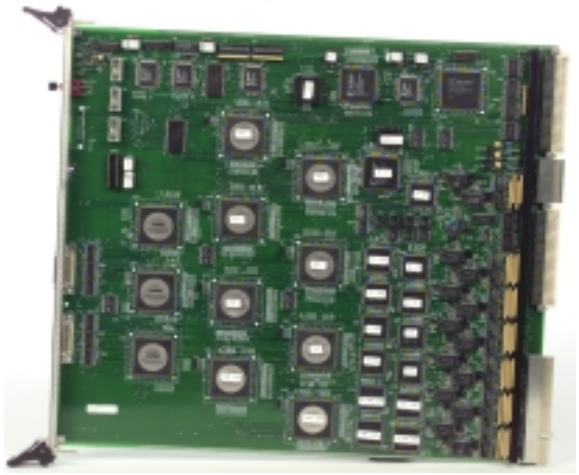
XFT System Electronics

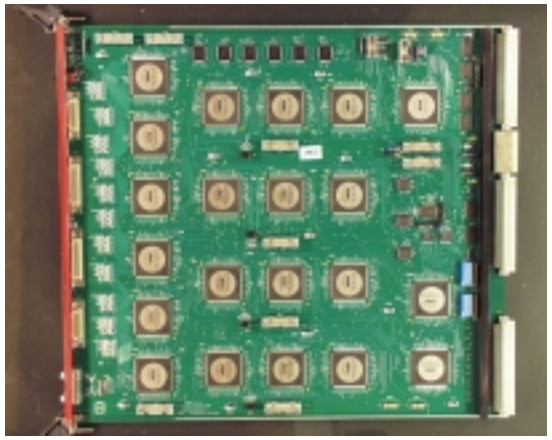
- Mezzanine Cards
  - 168 cards
  - Classifies hits as prompt/delayed

- Final Finder system
  - 24 SL1-3 boards
  - 24 SL2-4 boards
  - Heavy reliance on PLDs
    - Allows for some redesign: new patterns for number of misses, wire sag, faster gas, etc

- Final Linker System
  - 24 Linker boards
  - Heavy reliance on PLDs
    - Allows for new road set based on new beam positions
    - Have already developed 2 new roads sets due to accelerator changes.



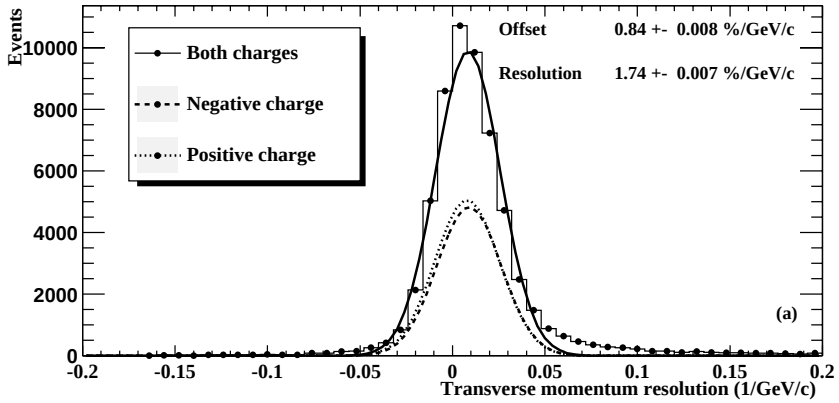


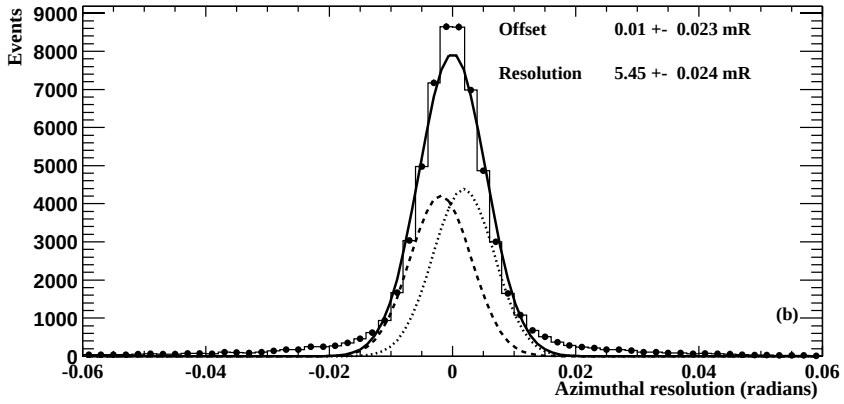


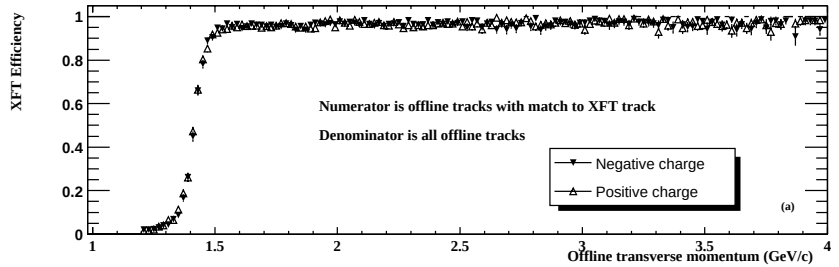
XFT Performance in CDF RunII

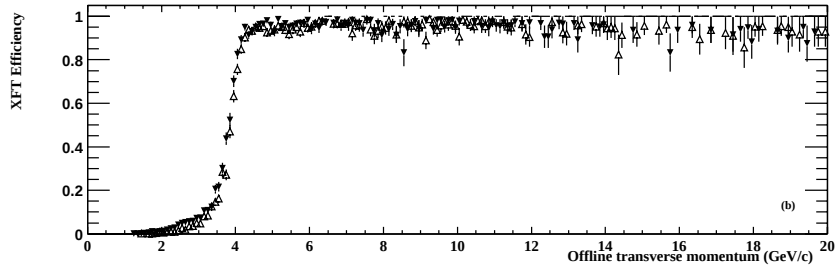
Performance of the XFT in CDF's RunII has been excellent

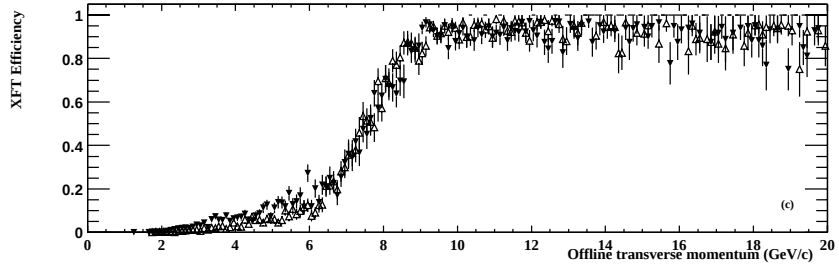
1. Momentum resolution 1.74%/GeV/c
2. Phi Resolution < 6mRad
3. Efficiency ~ 95%





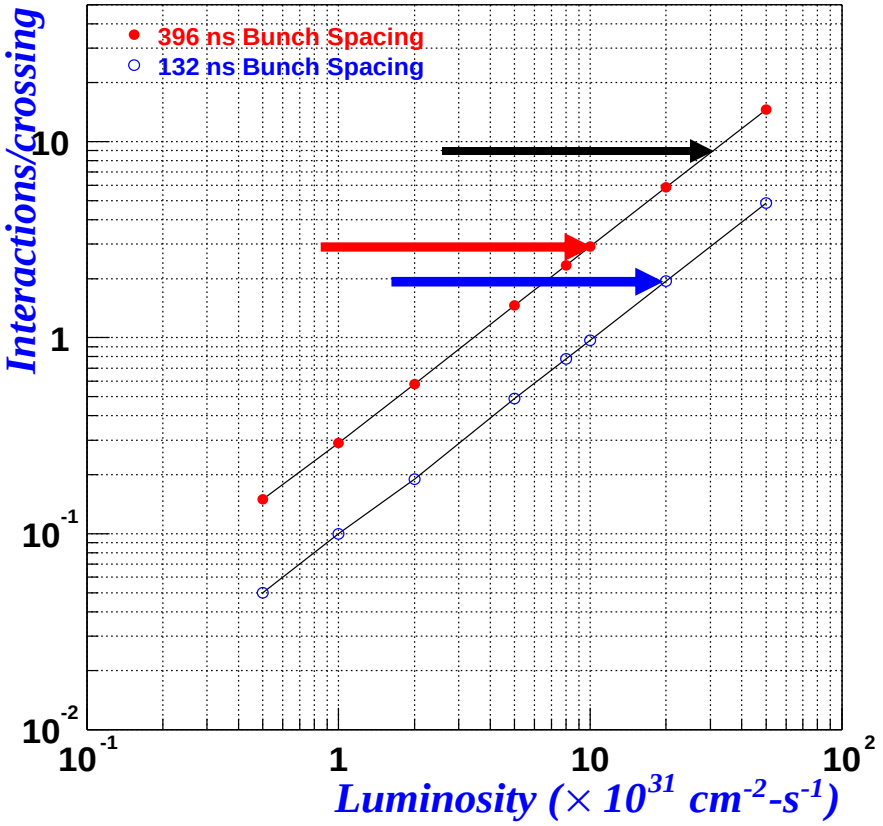


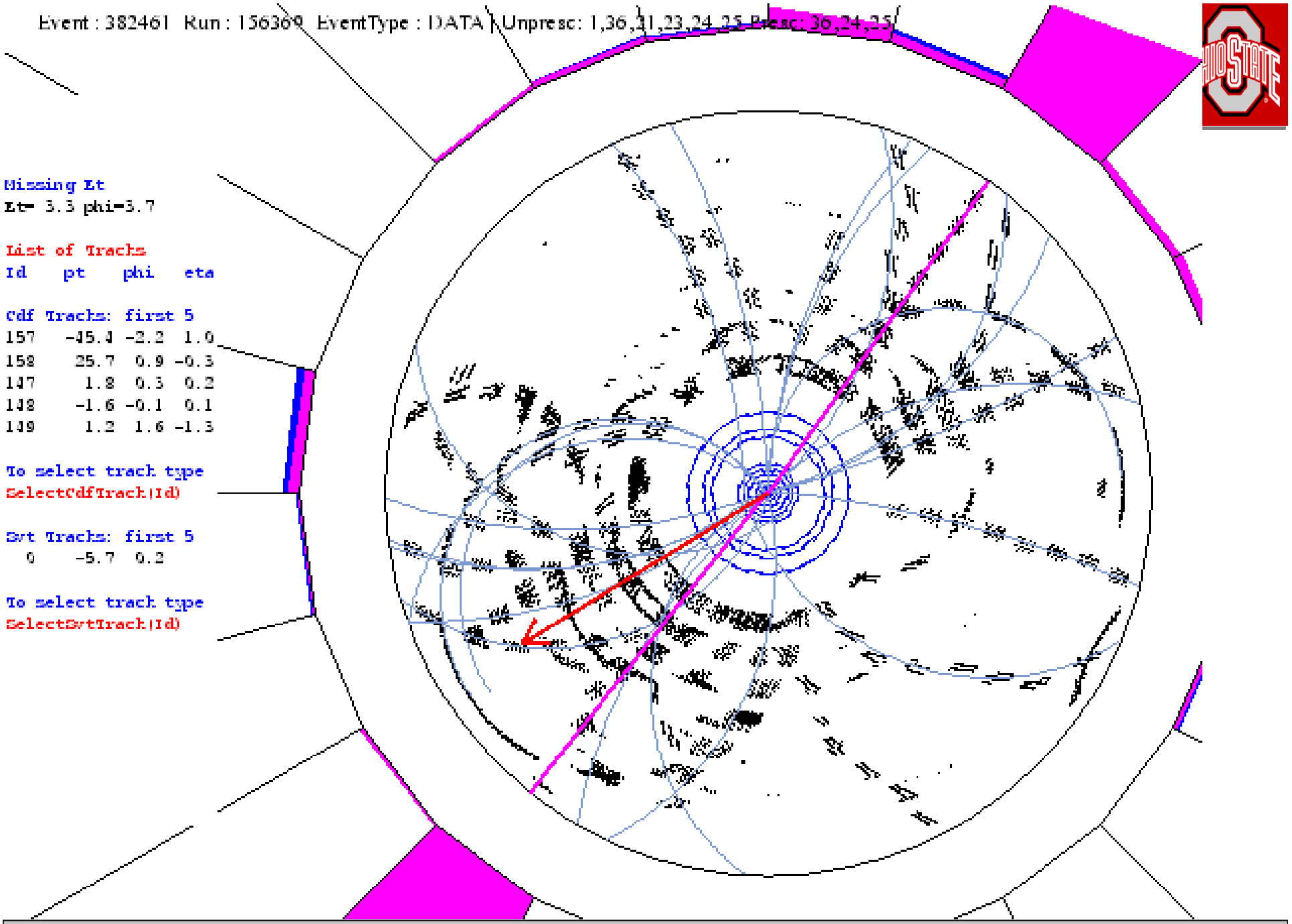




XFT Run II Upgrade

- The XFT was designed for a luminosity of:
  - $L=1x10^{32}cm^{-2}s^{-1}$ 396nsec bunch
    - <int/crossing> ~ 3
  - $L=2x10^{32}cm^{-2}s^{-1}$ 132nsec bunch
    - <int/crossing> ~ 2
- Accelerator Performance
  - Max lum attained: $5x10^{31}cm^{-2}s^{-1}$
  - Expect maximum of $L=3x10^{32}cm^{-2}s^{-1}$ 396nsec bunch
    - <int/crossing> ~ 9
    - Factor of 3-4 above design

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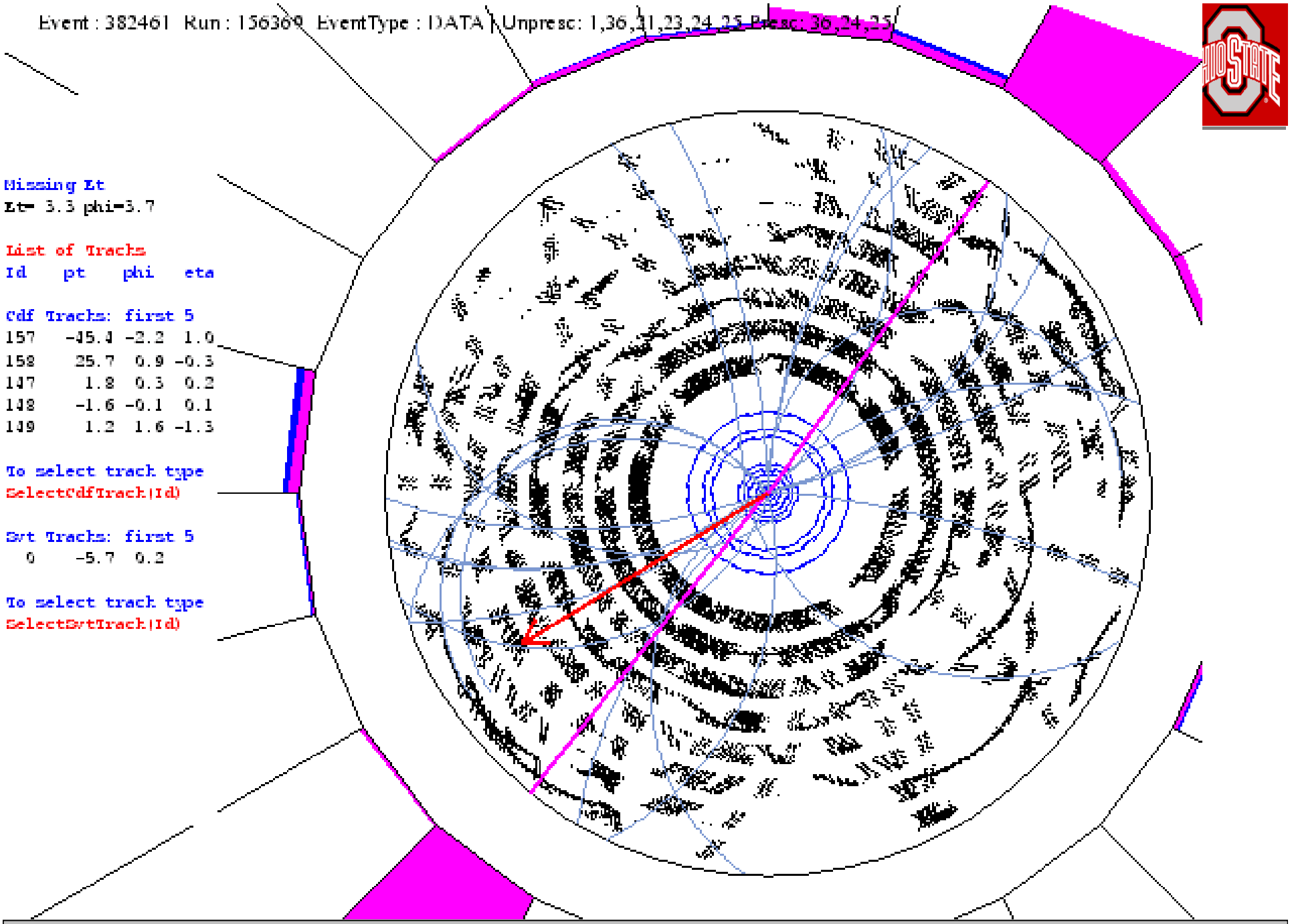
Missing Et
Et= 3.3 phi=3.7
List of Tracks
Id pt phi eta
Cdf Tracks: first 5
157 -45.4 -2.2 1.0
158 25.7 0.9 -0.3
147 1.8 0.3 0.2
148 -1.6 -0.1 0.1
149 1.2 1.6 -1.3
To select track type
SelectCdfTrack(Id)
Svt Tracks: first 5
0 -5.7 0.2
To select track type
SelectSvtTrack(Id)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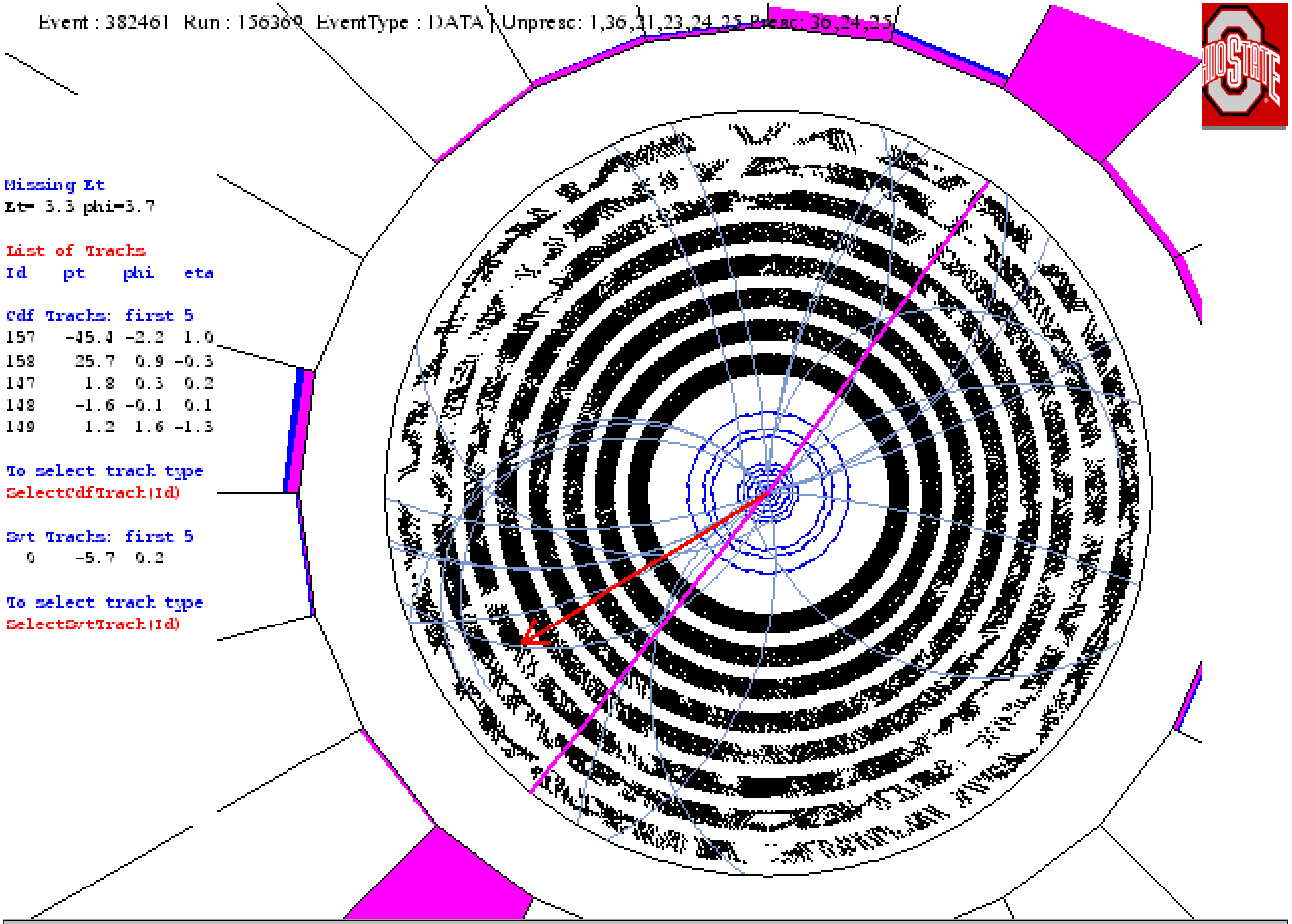
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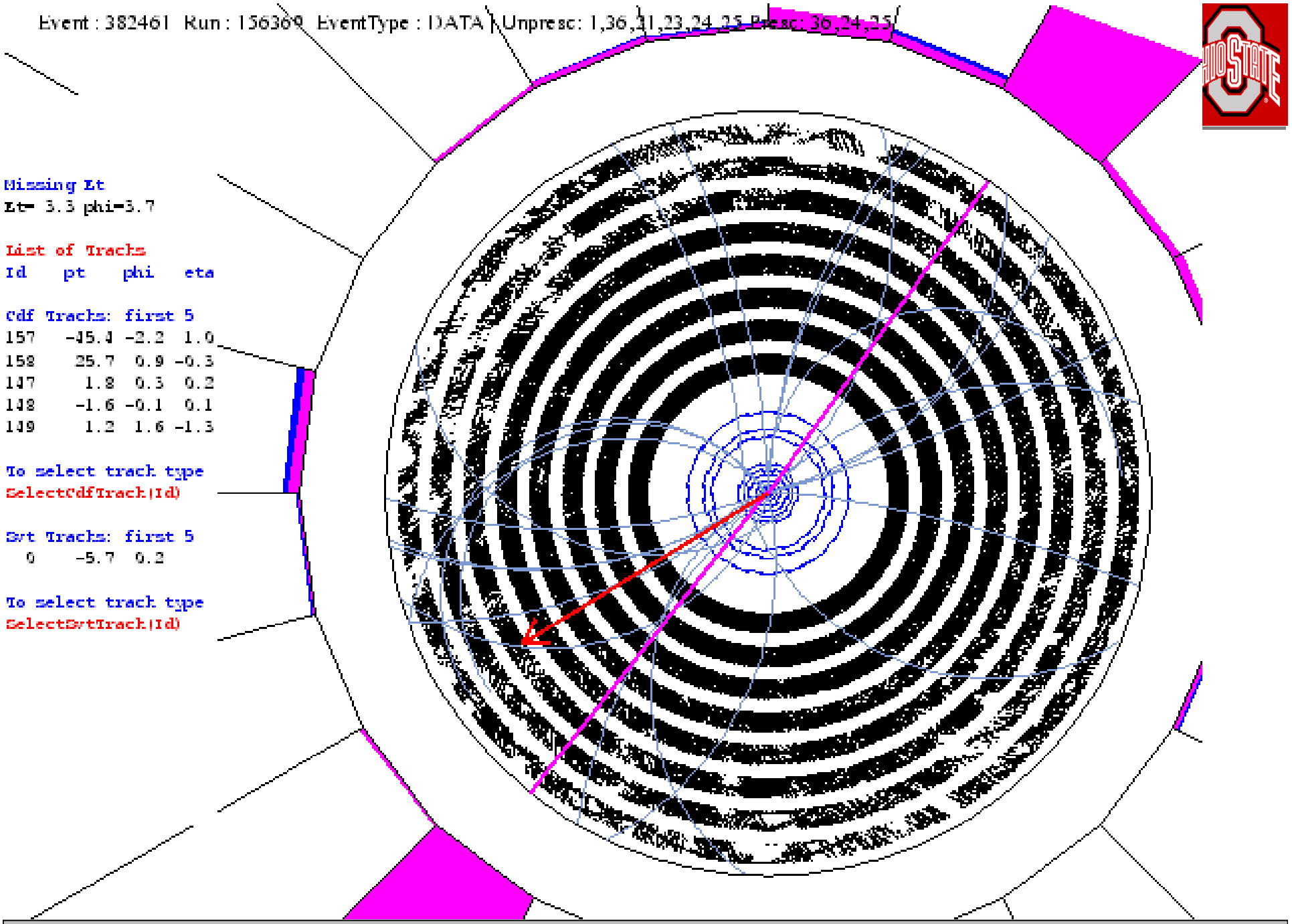
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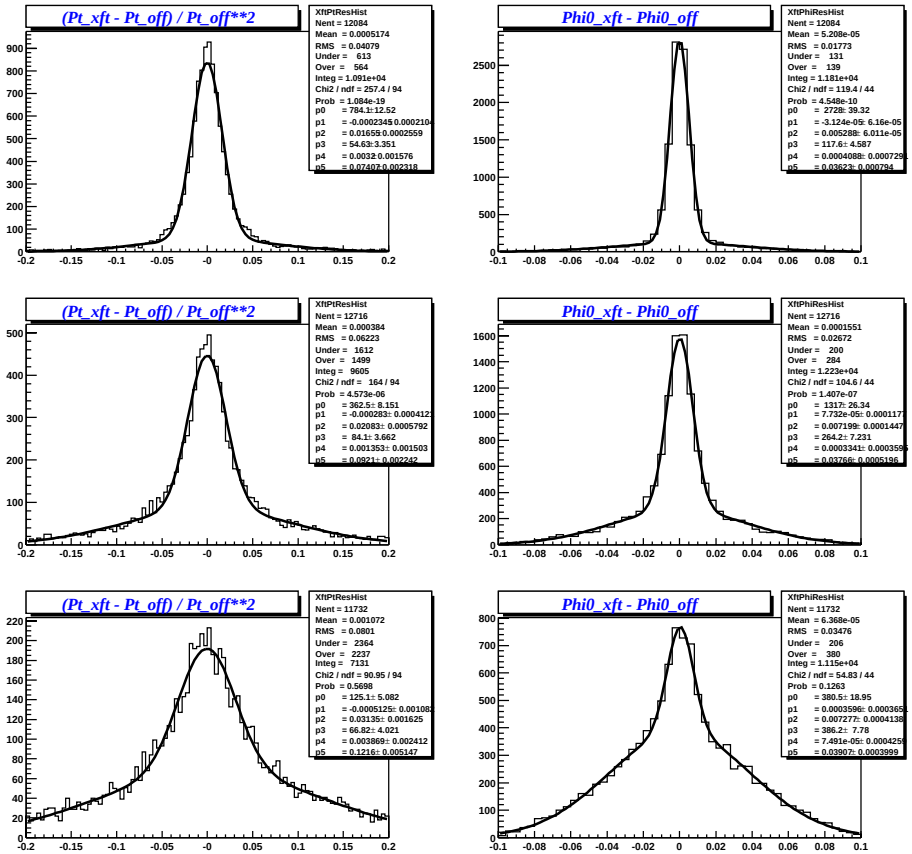
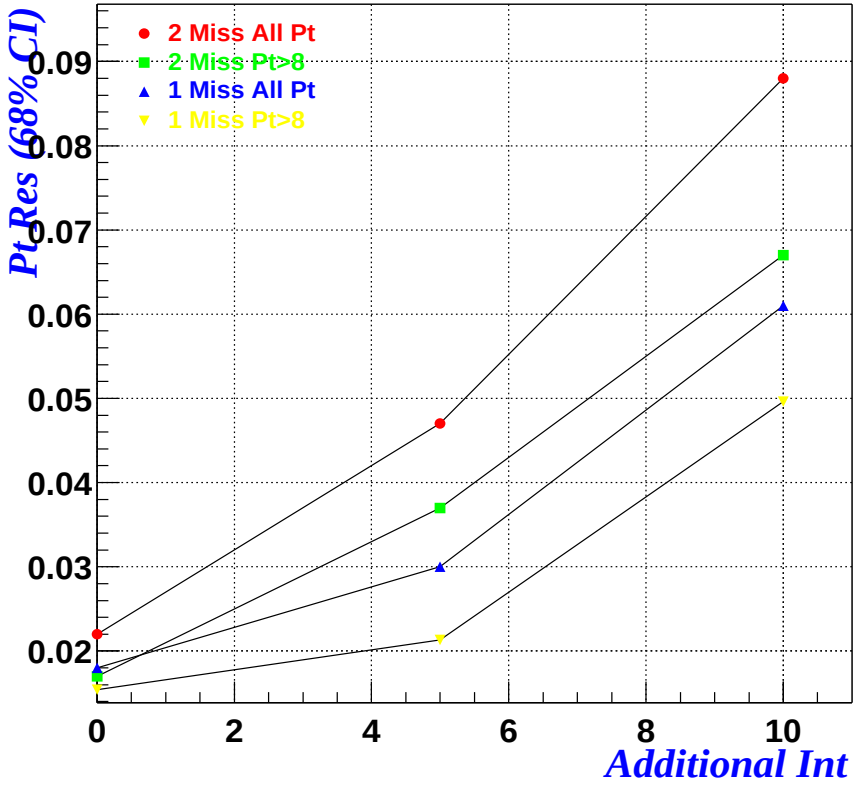
Performance at High Luminosity

Significant degradation observed as number of additional interactions exceeds 5



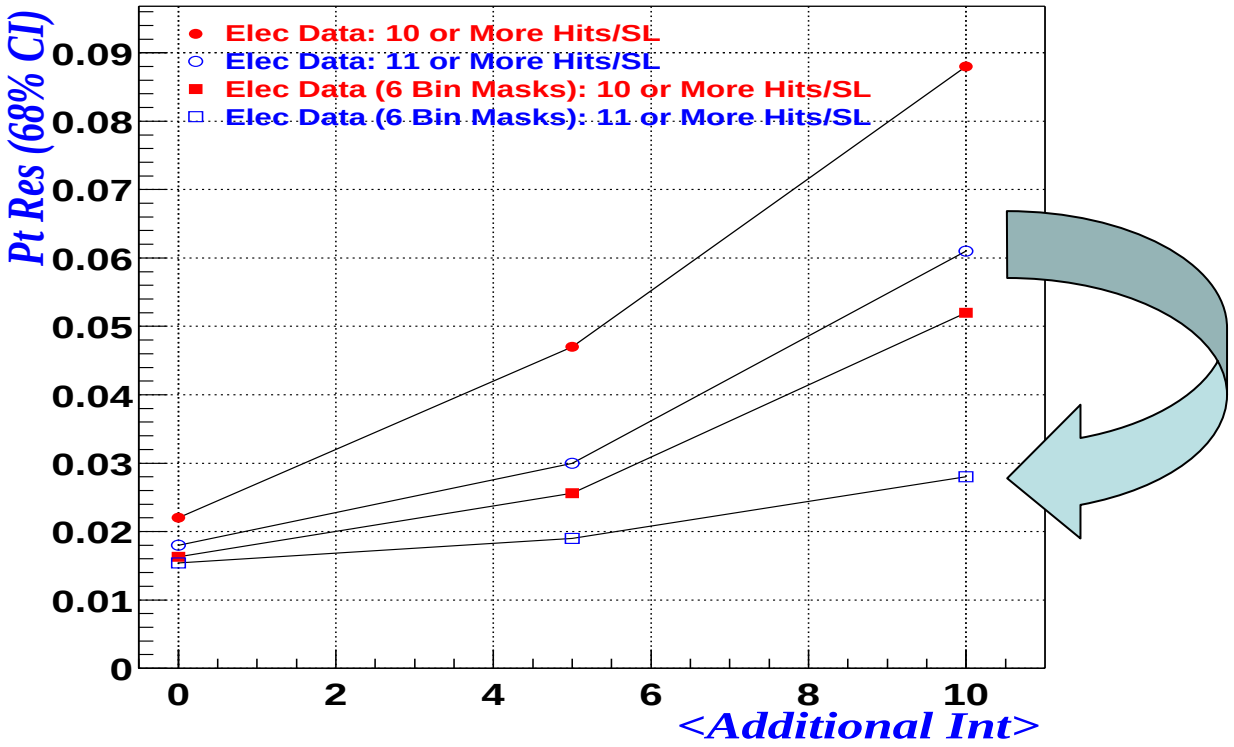


Algorithm Changes

- Hit Stage
  - Provide 6 times bins instead of the present 2
- Segment Finding Stage
  - Using 6 times bins, measure phi (pixel) position and slope at all 4 axial layers and 1 stereo layer.
  - Provide 5 slope bins at the outer two axial and outermost stereo layers, 3 slope bins at the inner two axial layers.
- Segment Linking Stage
  - Require matching slope and pixel at all 4 axial layers, instead of limited (low pt) slope requirement at the outer two layers.
  - Require stereo confirmation for high Pt tracks, stereo association for all tracks.

Simulation of Upgraded XFT

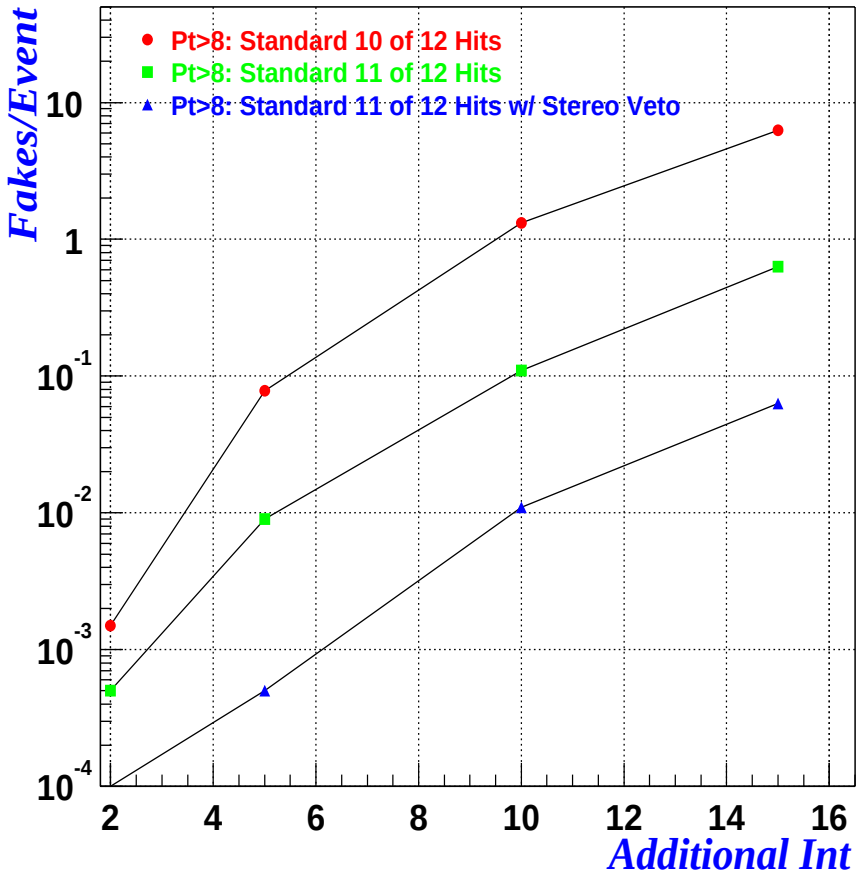
- Full simulation of RunII detector and occupancies necessary
  - Started on implementation of RunII XFT design using standard CDF environment
  - Preliminary indications of design performance

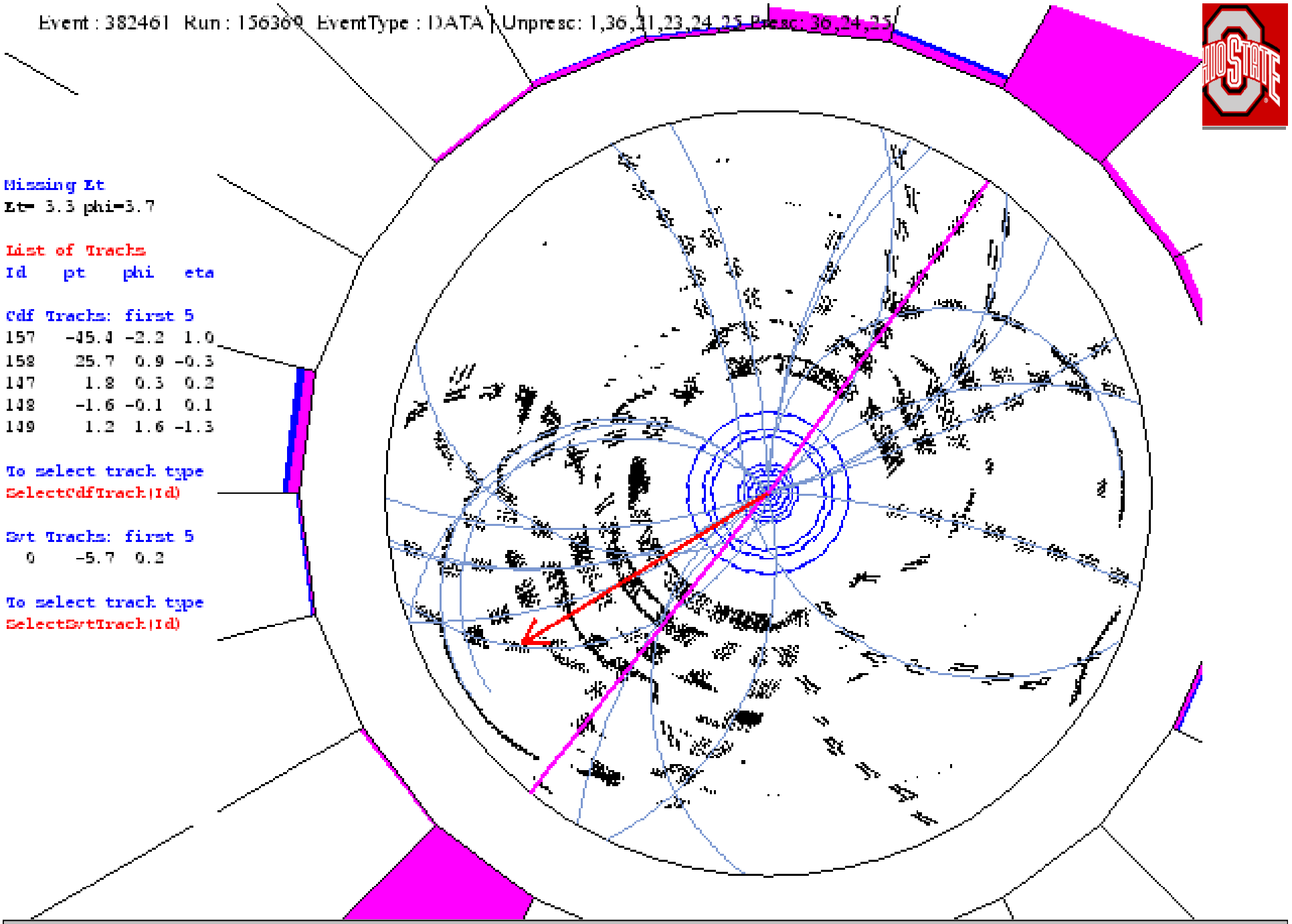


Improvement expected from upgrade

Impact of Stereo

- The stereo can have an impact in two ways:
  - Provide Z-pointing to tracks: Since EM and muon calorimeters are segmented in Z, coarse pointing can be very helpful in eliminating fakes
  - Confirmation Segment: Since often fake XFT tracks are the result of linking two unrelated low Pt segments, requiring another high Pt stereo segment in the allowed window around an axial track can be very powerful.
- Note that the stereo has no impact on phi/pt resolution.

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To select track type
SelectCdfTrack(Id)
Svt Tracks: first 5
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To select track type
SelectSvtTrack(Id)

Improving Pattern Recognition Chips

- New Finder Chips
  - Expect factor of 7 more masks
  - Need to Run about factor of 2 faster (16nsec internal clock versus 33nsec internal clock)

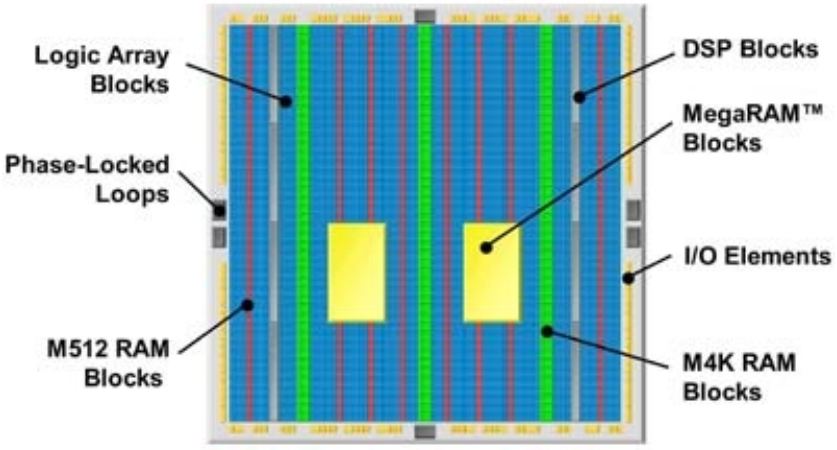
Chip	2 Time Bins, Masks	6 Time Bins, Masks
Finder Axial SL1	166	1344
Finder Axial SL2	227	1844
Finder Axial SL3	292	2056
Finder Axial SL4	345	2207

- New Linker Chips
  - Expect factor of 3.3 more roads
  - Need to run about factor of 2 faster(16nsec internal clock versus 33nsec internal clock)

Slope Bins	Roads
0,0,2,2	1200
3,3,5,5	4000

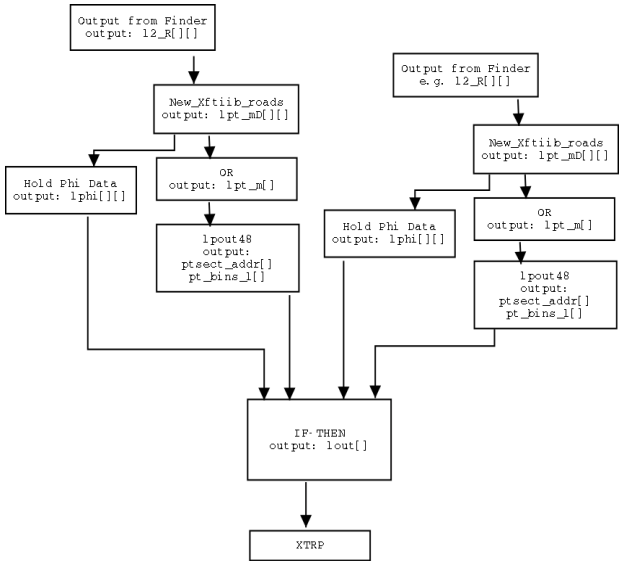
The Stratix Chip

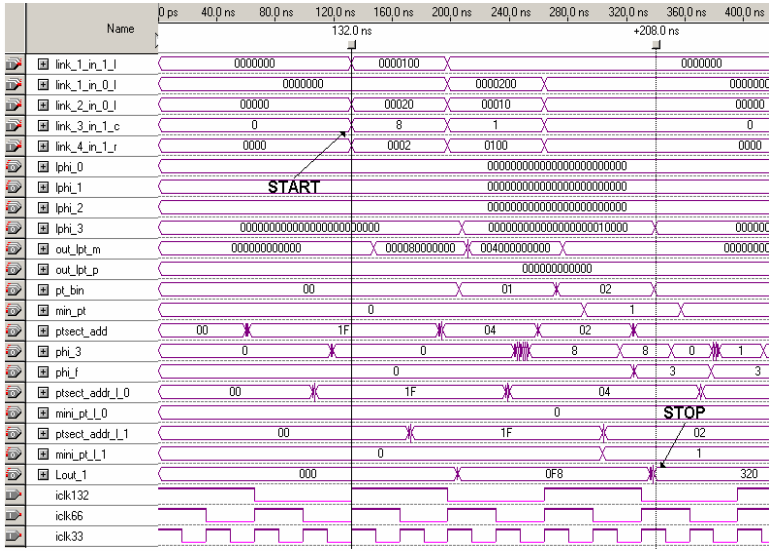
- The original XFT design utilizes Altera FLEX 10K50 chips for the Finder and Linker algorithms.
- The current Altera technology leader is Stratix:
  - Factor of >10 more logic elements
  - Factor of >100 more memory
  - Advanced I/O features
    - LVDS, SERDES
  - Factor of 4-6 faster
- Full simulation of new Linker chips using latest Altera FPGA design software tools



Implementing the Upgraded Linker Design

- Key features:
  - Design uses much more slope information from the upgraded Finder design
    - 3 slopes inner two axial layers
    - 5 slopes outer two axial layers
  - Many more roads needed per 1.25 degrees:
    - Current: 1200
    - Upgraded: 4000
- Design fully (and successfully) simulated using Altera software package (QUARTUS)



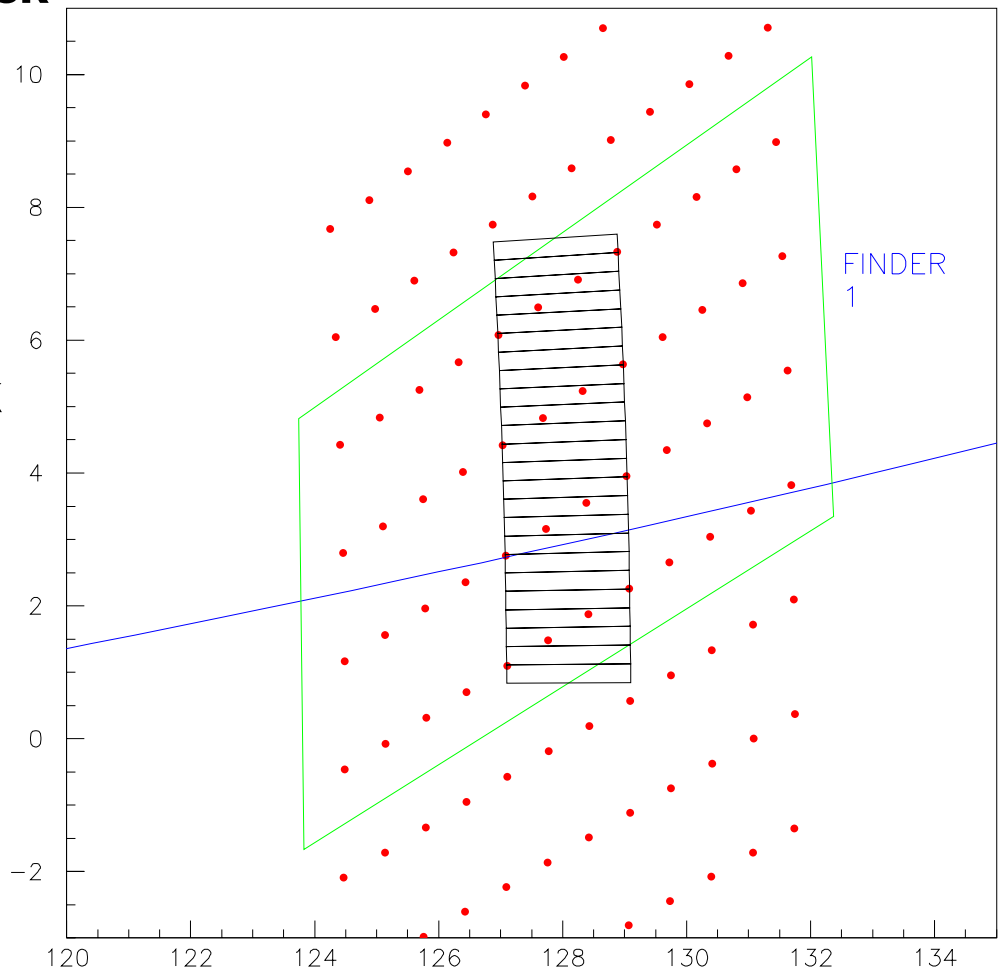


Conclusions

- The current XFT Trigger is installed and working well in the current CDF Run II trigger and DAQ system
- Fermilab's luminosity plans indicate that the current XFT will suffer from increased occupancy when the design luminosity is greatly exceeded
- A planned upgrade of the XFT will address the occuppancy problems
- The upgrade is currently in the design stage, and we are planning for installation and commissioning by summer 2005.

Finder Output

- In the **inner** two layers, each **mask** corresponds to 1 of 12 **pixel** positions in the middle of the layer.
- The **pixel** represents the **phi** position of the track.
- In the **outer** 2 layers, each **mask** corresponds to 1 of 6 **pixel** positions and 1 of 3 **slopes:** (low pt +, low pt -, high pt).
- When a **mask** is located, the corresponding **pixel** is turned on.



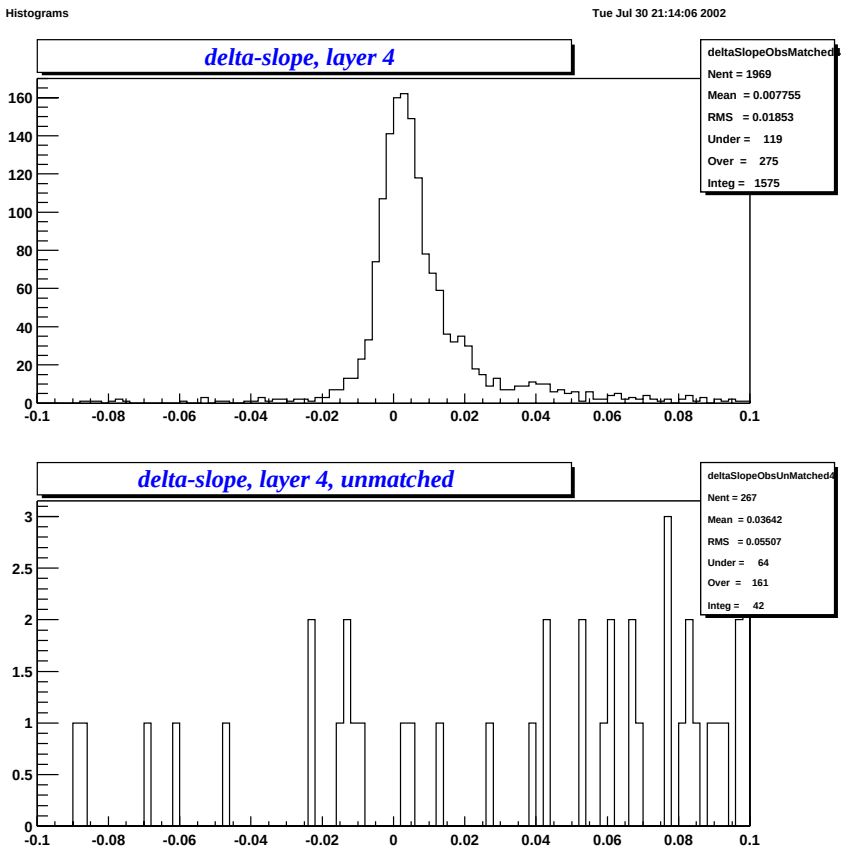
Backup Slides

Improving The XFT

- Degradation of XFT occurs in 3 areas:
  1. Transverse momentum (P_T) resolution
  2. Extrapolated ϕ_0 resolution
  3. fake track fraction
- To improve things we need:
  - Better segment finding: This will reduce the number of spurious pixels reported to the Linker.
    - Axial Finders: improve ϕ_0 and P_T resolution.
    - Stereo Finders: Reject fake tracks
  - Better segment linking: Valid segments from different low pt tracks could be mistaken for a single high Pt track. This becomes a much bigger problem at high luminosity. Using better slope information at the linking stage reduces this problem.

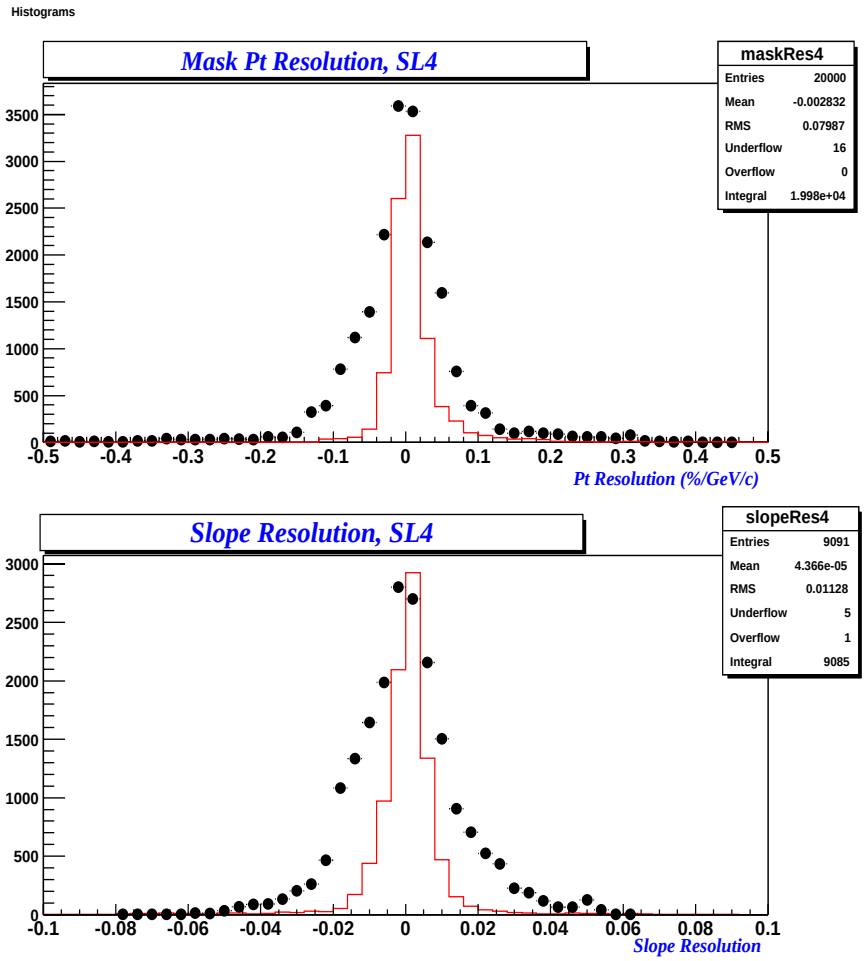
Fake Tracks

- The plots show the difference in local slope between found XFT tracks and the nearest true Monte Carlo track.
- The top plot is for “real” XFT tracks.
- The bottom plot is for “fake” (unmatched) XFT tracks.
- Conclusion: Fake tracks are due to combination of segments from ***different*** **real** tracks



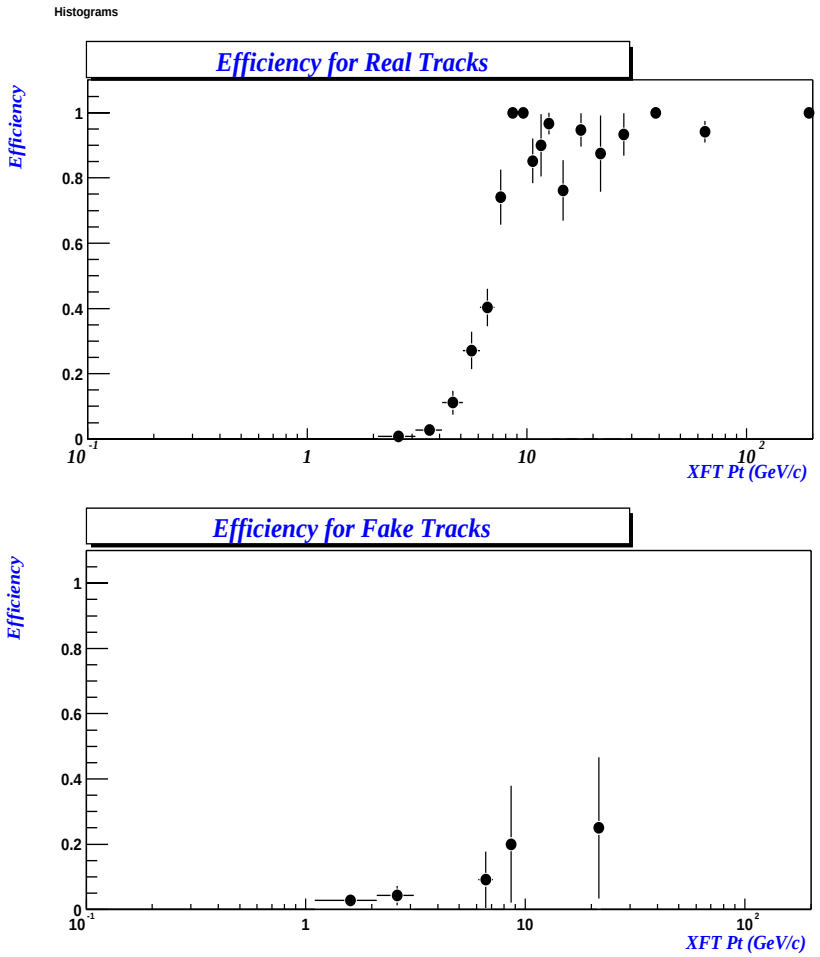
Impact of Additional Timing Information

- The additional resolution in timing at the hit level allows the Finder to measure the Pt or Slope of the segments with higfer precision.
- We have added this new timing info to our full XFT simulation, to understand the impact on resolution at the segment finding level.
- The top plot shows the improvement in slope resolution at the mask level. The solid curve uses the additional timing information.
- The bottom plot shows the same for the slope resolution at the mask level.

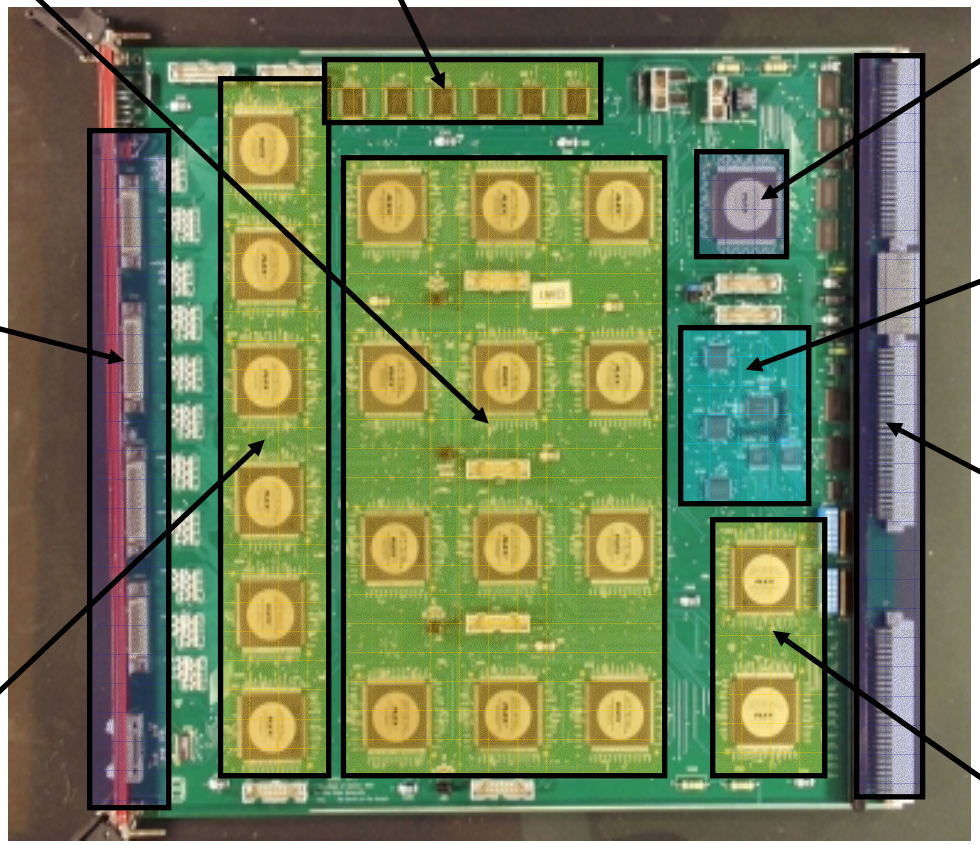


Impact on Segment Linking

- We have tested how better segment slope resolution can help reject fakes.
- In a Monte Carlo sample, we smear segments found by the expected slope resolution. We then ask if this "measured" slope is above a high Pt threshold.
- We require both segments from the outermost axial layer to have passed the high Pt threshold.
- The upper plot is the efficiency for true tracks to pass the threshold.
- The lower plot is the efficiency for fake tracks to pass the threshold.

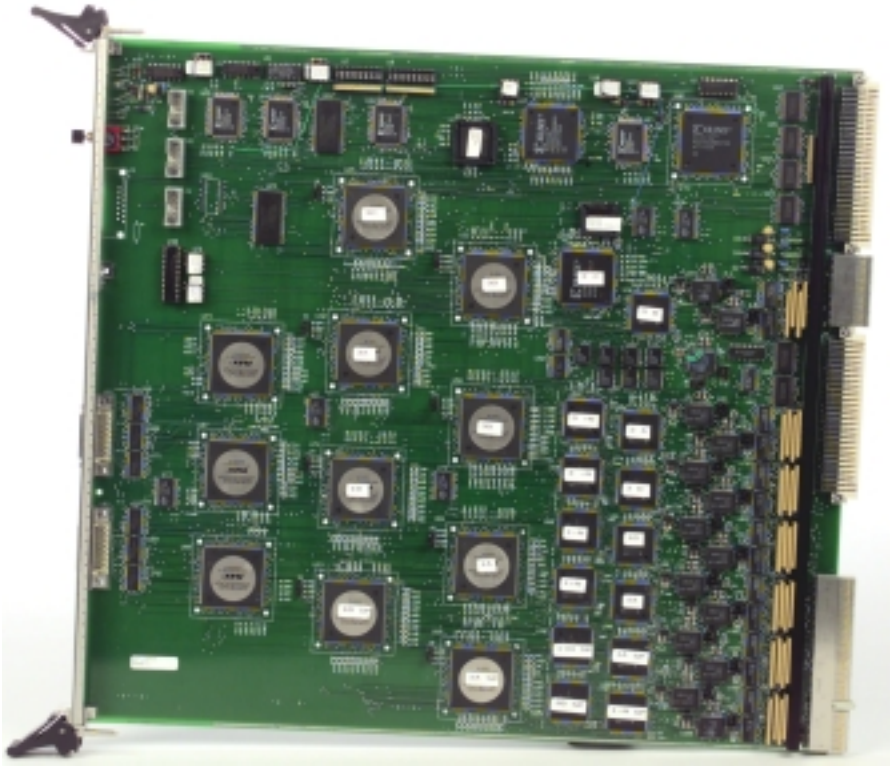


Designing a New Linker Prototype



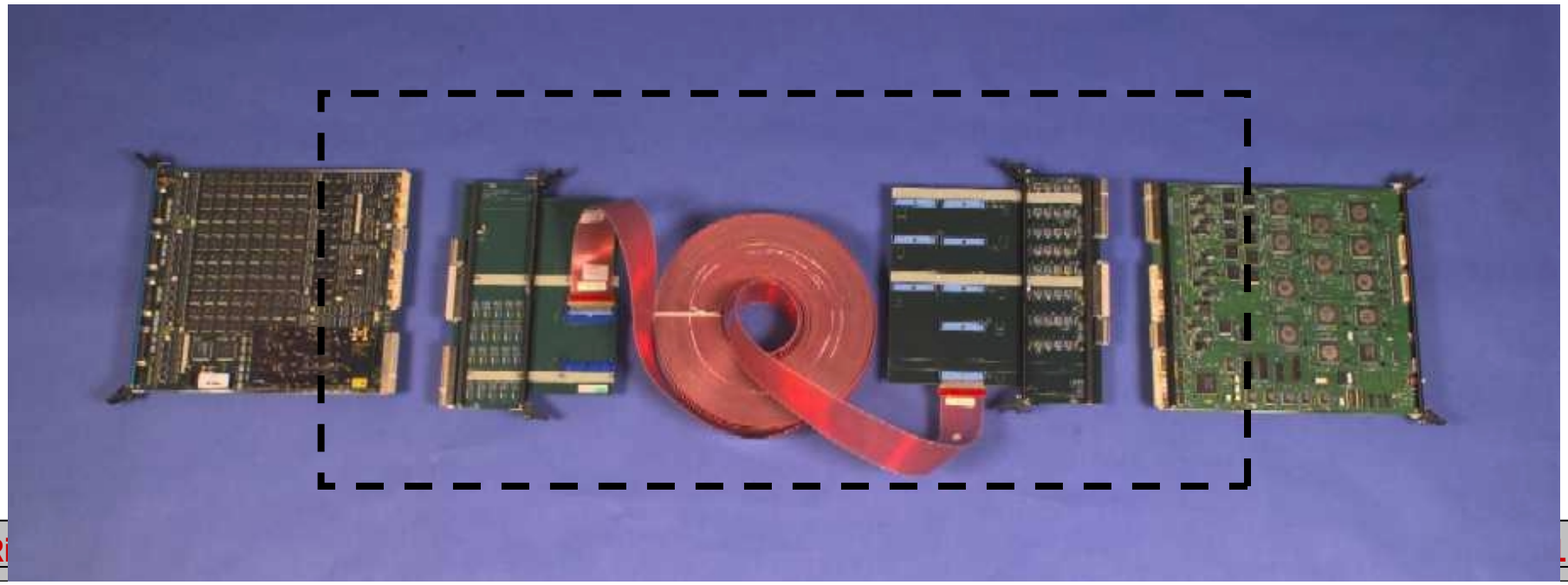
Upgraded Finder Board

- The input capture section runs at the same speed and does not change.
- The pixel driver (output) section runs at the same speed and does not change.
- The primary change is to the Finder pattern recognition chips.
  - Need more masks
  - Need to run faster since time is taken to input more data (3x more hit data)
- New board layout needed since Finder chip footprint will change



What changes:TDC to Finder

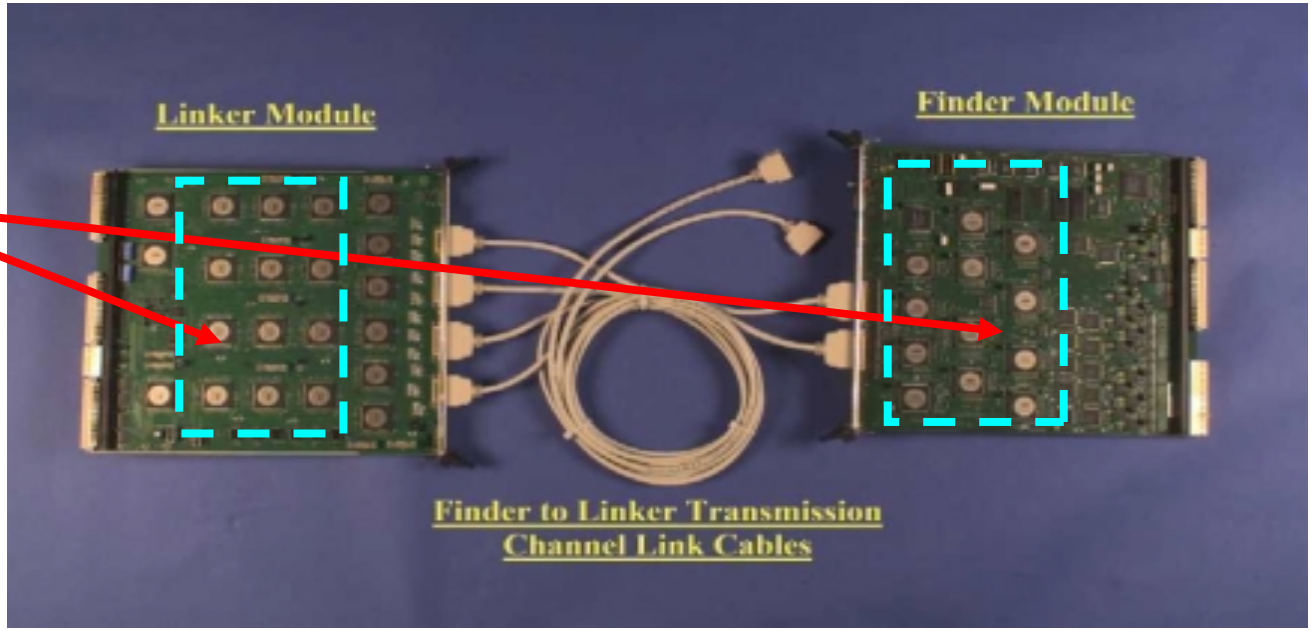
- The upgraded TDC (?) replaces the current TDC + mezzanine card to provide hit information to the Finder.
- However, the TDC transition cards, cabling, and Finder transition cards in the present system are reused.
- Data is driven up the Ansley cables at the current clock of 22nsec. Two additional CDFCLK (@132nsec) are required to send up 6 time bins/wire versus the present 2 times bins/wire



What changes: Finder to Linker

- The Finder control output, cabling, and Linker Input sections do not need to change. We use the additional 2 CDFCLKs (@132nsec) to transfer additional slope information.
- The Linker output section can also remain the same as the present system.

Algorithm chips need to be modified to handle increase in information.



Using the New FPGAs

- Current Linker chips use Altera EP10k50 devices.
- Target device for upgraded design: Altera EP1S25
- First step: Implement current algroithm in new devices, with no changes
- Design fits easily: factor of 10 less utilization; much faster (3-10x)

Device For Compilation	EP1S25	EP10K50
Total Logic Elemnts	2,404/25,660 (9%)	2515/2880 (87%)
Total Pins	160/706 (23%)	159/249 (63%)
Total ESB bits	n/a	3328/20480 (16%)
Total Memory Bits	3,328/1,.944,576 (<1%)	n/a
DSP Block 9-bit elements	0/80	n/a
PLL's	0/6	n/a
TIMING		
iclk33	T = 7.5ns	T = 25ns
iclk66	T = 10.8ns	T = 70ns
iclk132	T = 3.7ns	T = 34ns