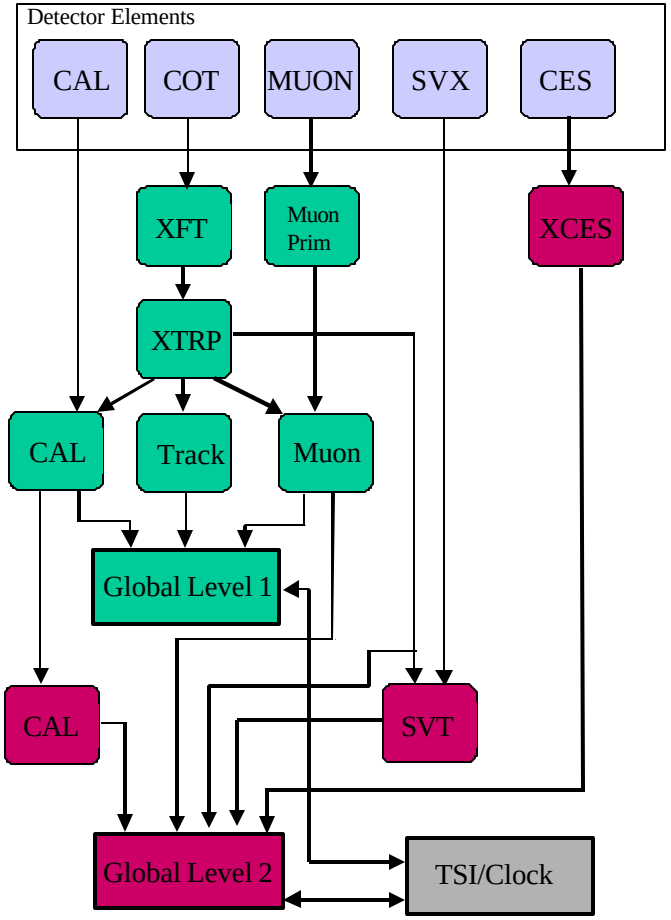
eXtremely Fast Tracker; An Overview

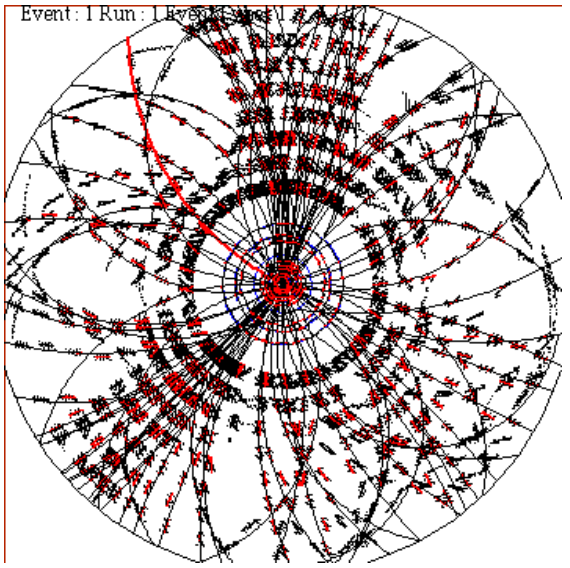
XFT = eXtremely Fast Tracker

- Role of tracking
  - Top, W/Z, Exotic Physics triggers require High momentum electron and muon **Level 1 trigger** candidates
  - Bottom Physics require low momentum tracking at the
  - **Level 1 trigger**
    - electrons
    - muons
    - hadronic tracks
- L1 Trigger Primitives
  - Electrons: XFT track + EM cluster
  - Muons: XFT track + muon stub
- L2 Trigger Tracks
  - XFT Track + Silicon Hits



Central Outer Tracker (COT)

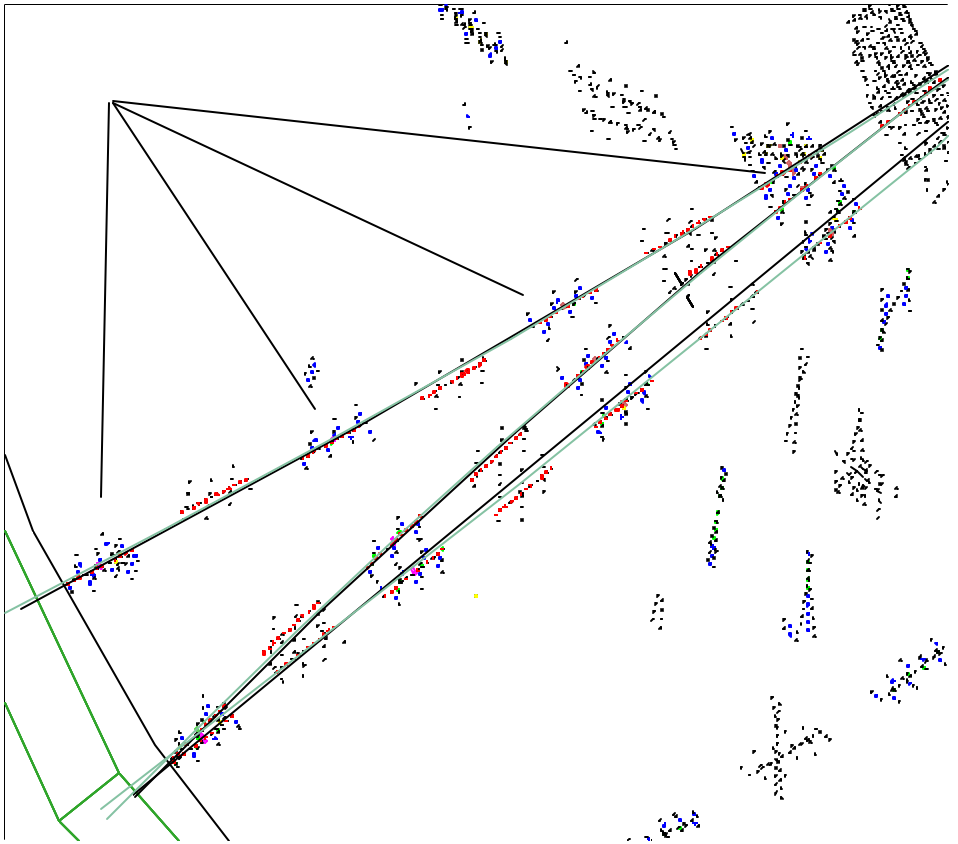
- 8 “superlayers”
  - 4 with axial wires
    - r - ??measurement
  - 4 with stereo wires
    - z measurement
- Small Cells
  - 0.88 cm drift (avg.)
  - Max drift time ~220 ns
  - 12 sense wires/cell: 96 possible measurements
  - 2540 cells, 30240 channels total
  - 1344 cells, 16128 channels axial only



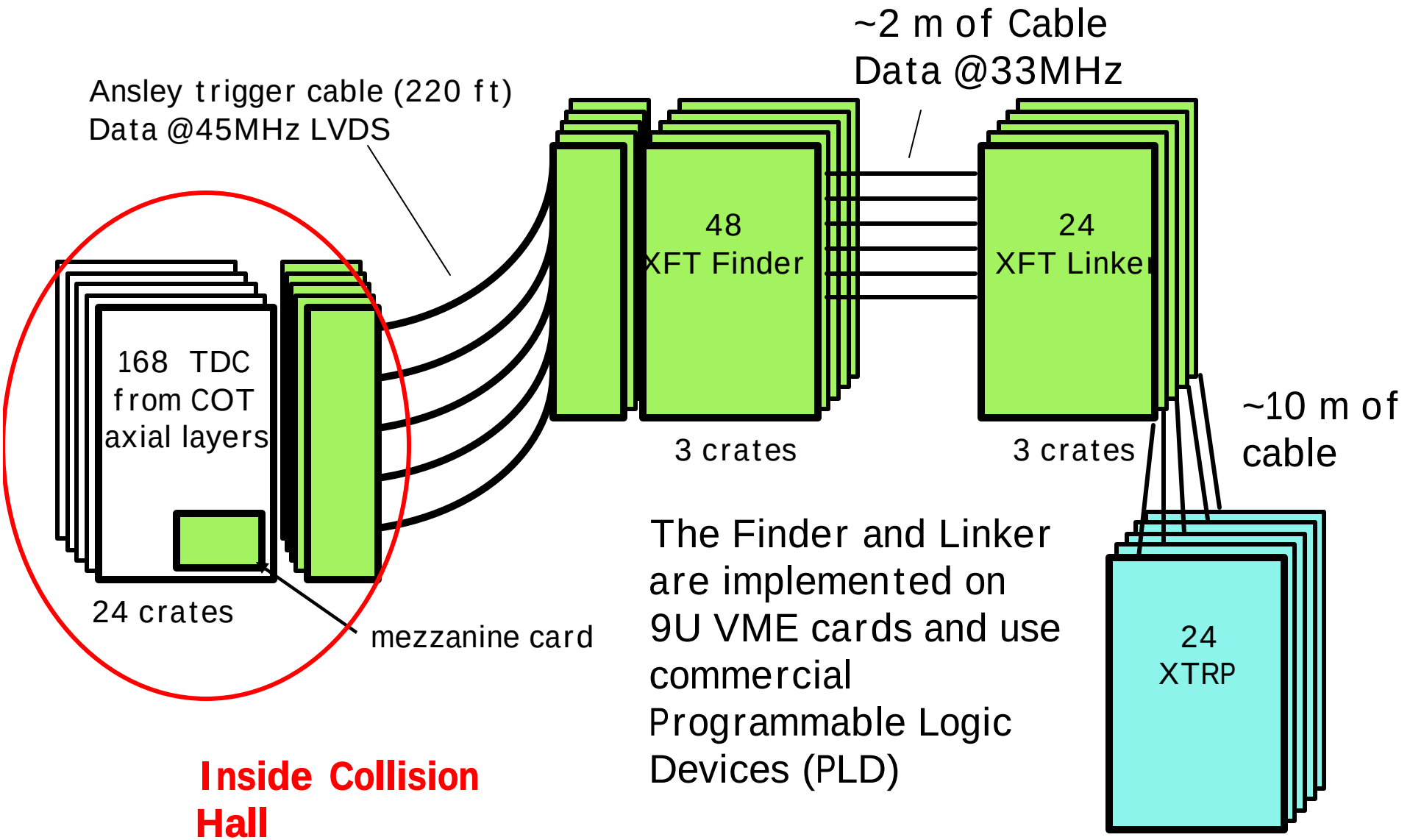
Charged Track Finding

- Hit Finding: Mezzanine Card
  - Hits are classified as prompt or delayed
- Segment Finding
  - In the axial layers, search for patterns of prompt/delayed hits consistent with High Pt tracks
  - Each segment found is assigned a pixel (phi, all layers) and possibly a slope (outer 2 axial layers only)
- Track Finding
  - Looking across 3 or 4 axial layers, search for patterns of segments consistent with Pt>1.5 GeV/c
  - Resultant Pt and Phi of all 1.5 GeV/c tracks sent on to XTRP
  - Maximum of 288 tracks reported
- New Tracks reported every 132nsec!

Good hit patterns are identified as segment, then segments are linked as tracks

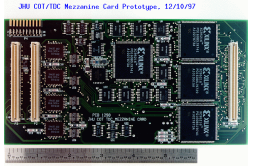


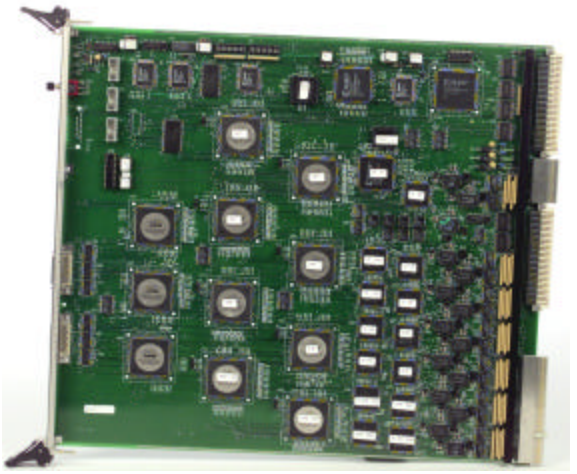
XFT Tracking Trigger

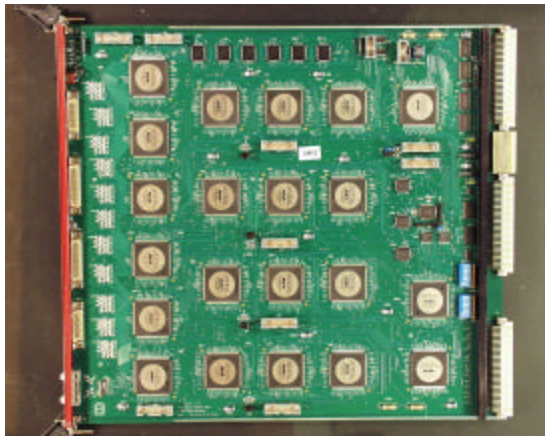


XFT System

- Mezzanine Cards
  - 168 cards
  - Classifies hits as prompt/delayed
- Final Finder system
  - 24 SL1-3 boards
  - 24 SL2-4 boards
  - Heavy reliance on PLDs
    - Allows for some redesign: new patterns for number of misses, wire sag, faster gas, etc
- Final Linker System
  - 24 Linker boards
  - Heavy reliance on PLDs
    - Allows for new road set based on new beam positions
    - Have already developed 5(?) new roads sets due to accelerator changes.

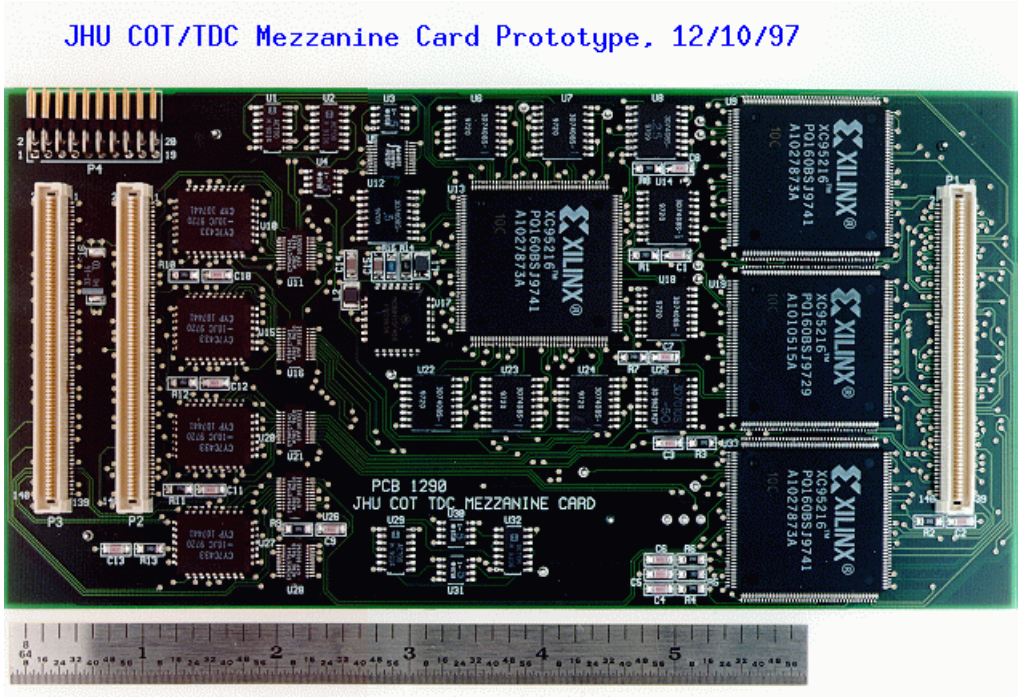






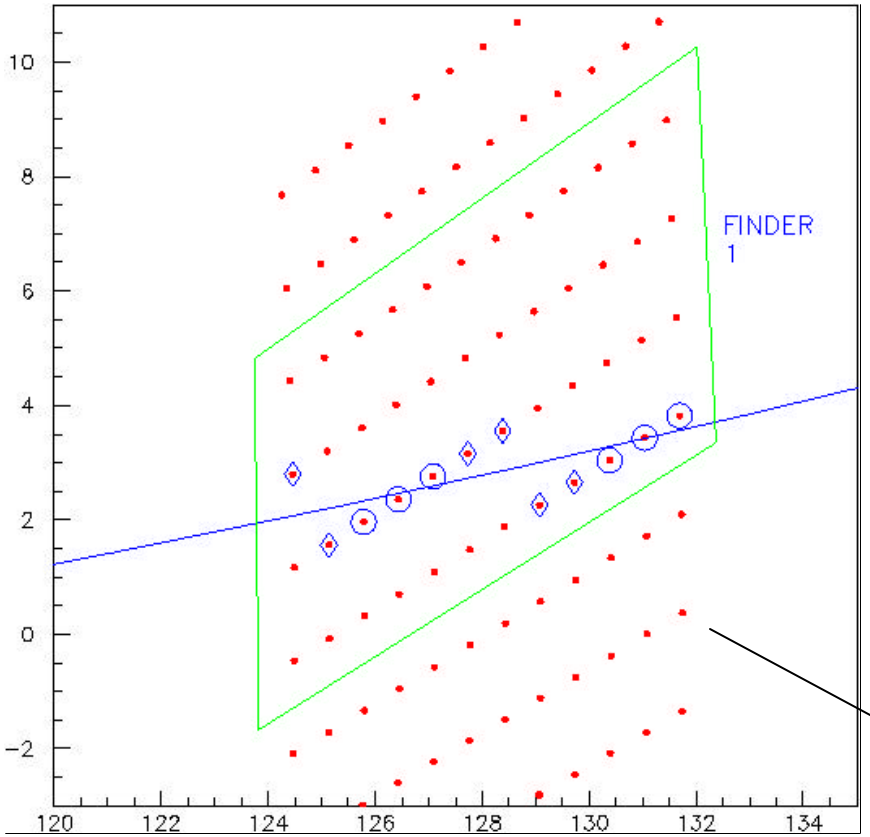
TDC Mezzanine Card

- Developed at University of Michigan
- Resides on axial TDC's
- Classifies all hits as prompt and/or delayed



TDC Mezzanine Card (XTC)

As tracks pass through each layer of the COT, they generate "hits" at each of the 12 wire-layers within a superlayer.



The mezzanine card is responsible for classifying each hit on a wire as either

- **Prompt: Drift time from 0-66 nsec**
- **Delayed: Drift time from 66-210 nsec**

"Prompt" hit

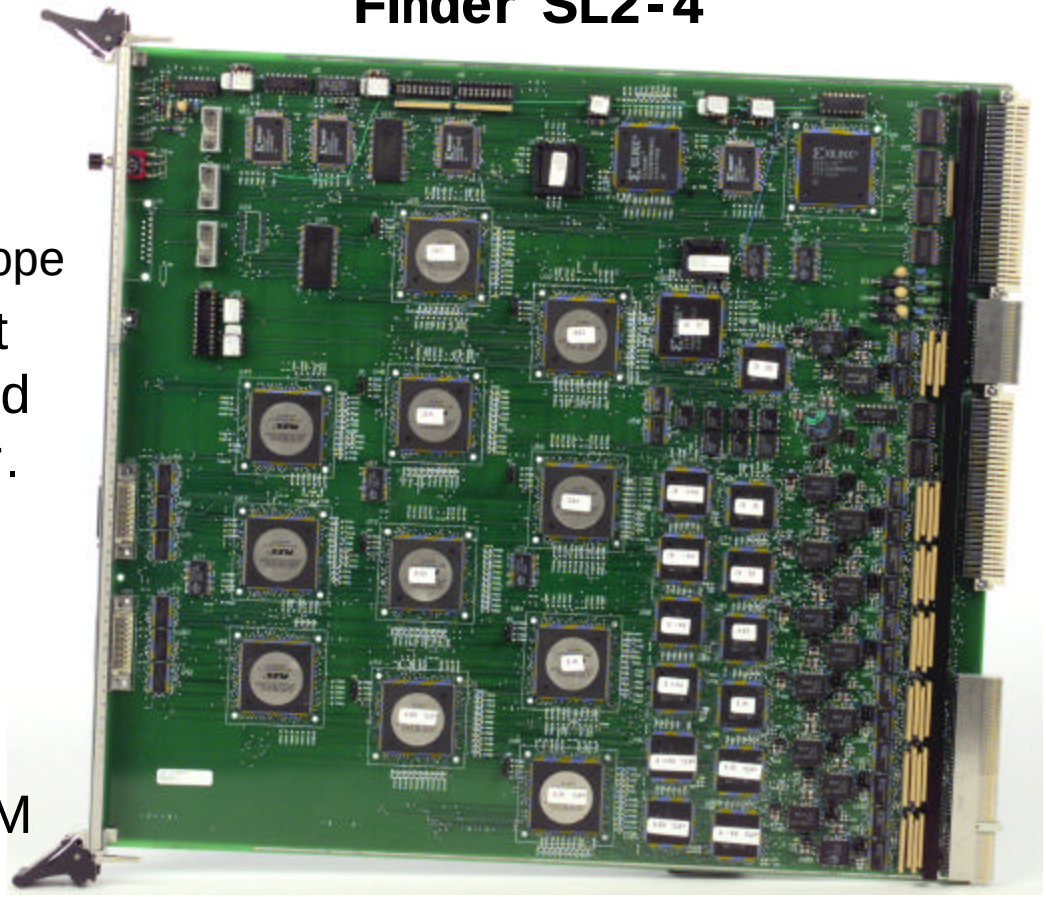
"Delayed" hit

Single COT Superlayer

Finder Board

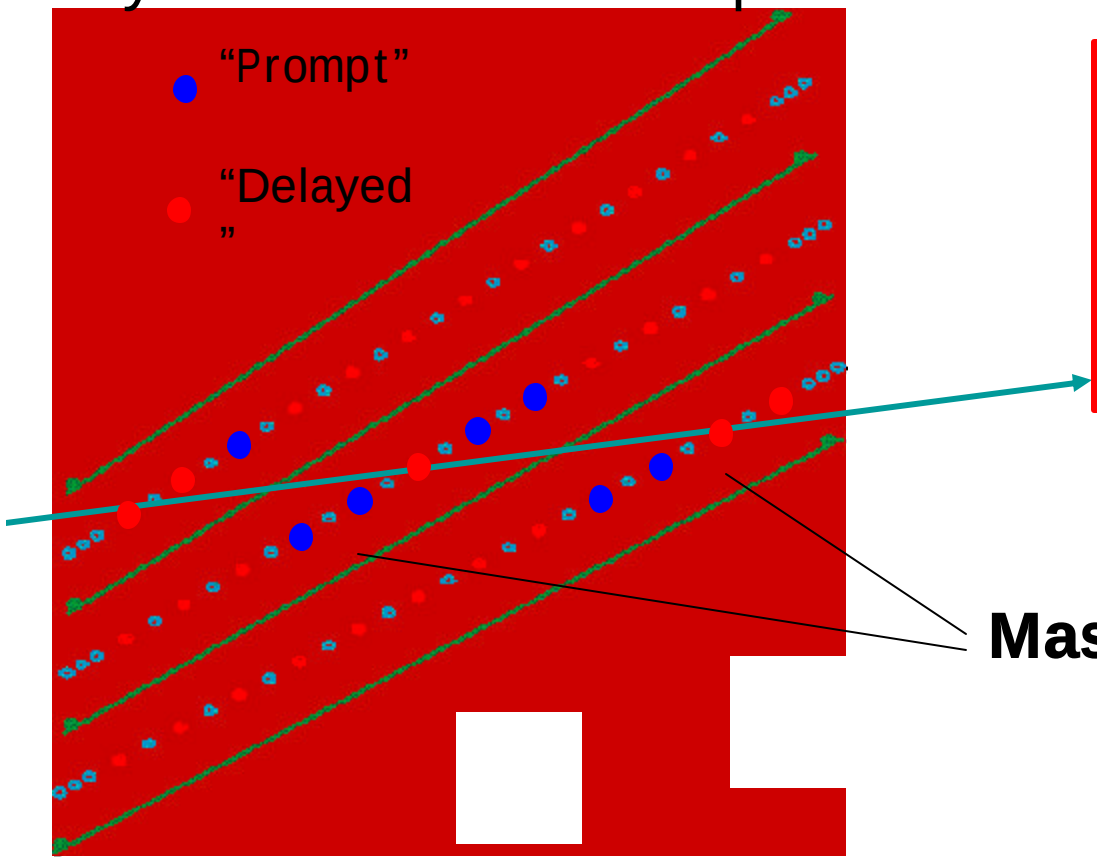
- Developed at FNAL.
- Each Finder PLD contains all the masks needed to find segments with Pt > 1.5 GeV/c.
- For SL 1, 2, 3, 4:
  - Masks: 170, 230, 270, 310
  - Pixels: 12, 12, 6 & slope, 6 & slope
- Each chip processes 4 adjacent COT cells, and outputs pixel and slope information to the Linker.
- 48 Finder Boards (2 Flavors)
  - 24 SL1-3 Boards
  - 24 SL2-4 Boards
- 336 total Finder chips Board programs are stored in EEPROM and Flash Ram

Finder SL2-4



The Finder

Track segments are found by comparing hit patterns in a given layer to a list of valid patterns or "**masks**".

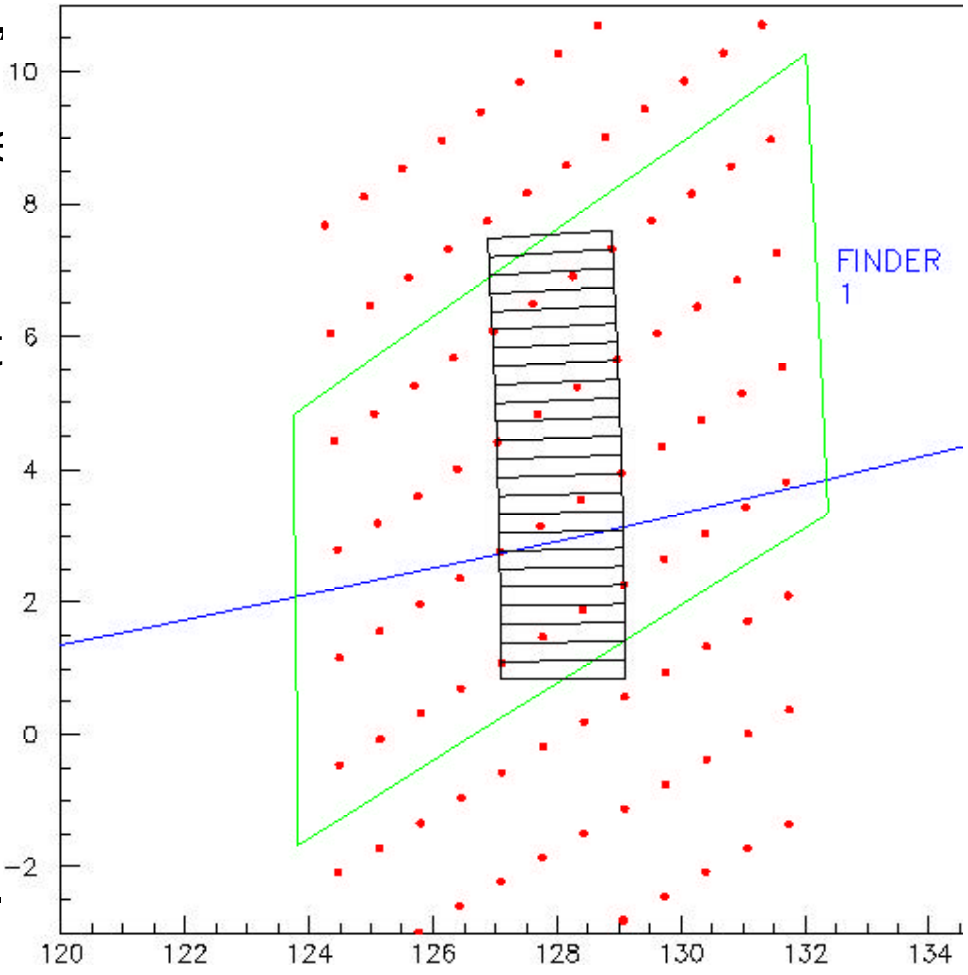


Up to 3 missed hits are allowed. The number of misses is programmable depending on the COT efficiency.

Mask : A specific pattern of prompt and delayed hits on the 12 wires of an axial COT layer

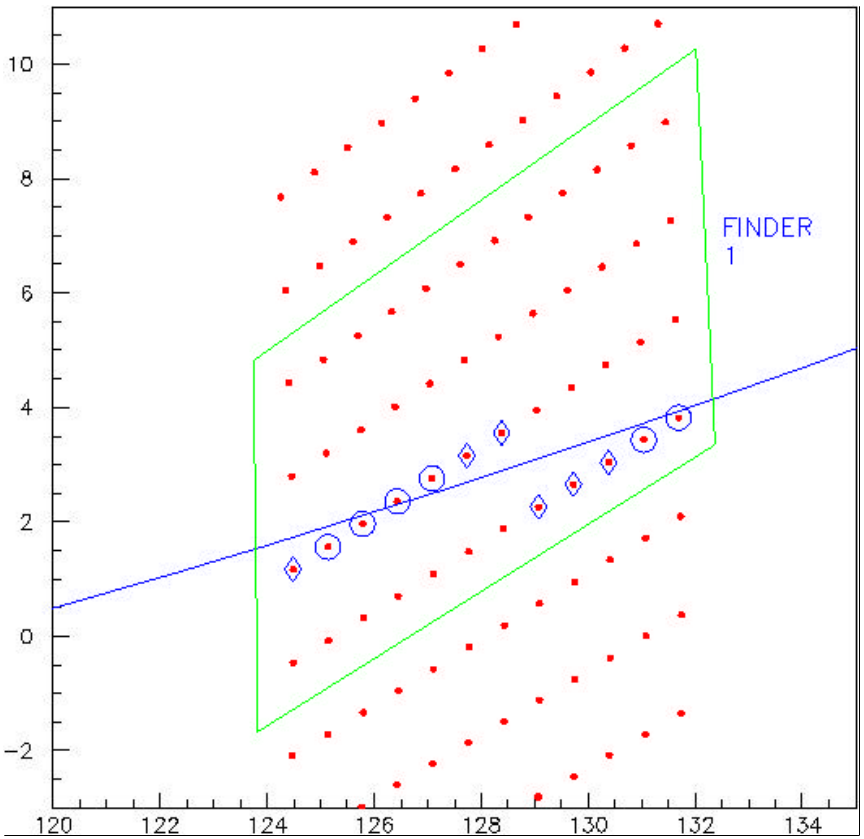
Finder Output

- In the **inner** two axial superlayers, each **mask** is assigned to 1 of 12 **pixel** positions in the middle of the layer.
- The **pixel** represents the **phi** position of a valid segment at that superlayer.
- In the **outer** 2 axial superlayers, each **mask** corresponds to 1 of 6 **phi pixel** positions and 1 of 3 **slopes:** (low pt +, low pt -, high pt).
- When a **mask** is found, the corresponding **pixel** is "turned on".
- More than one mask (& pixel) may be found within a COT cell.

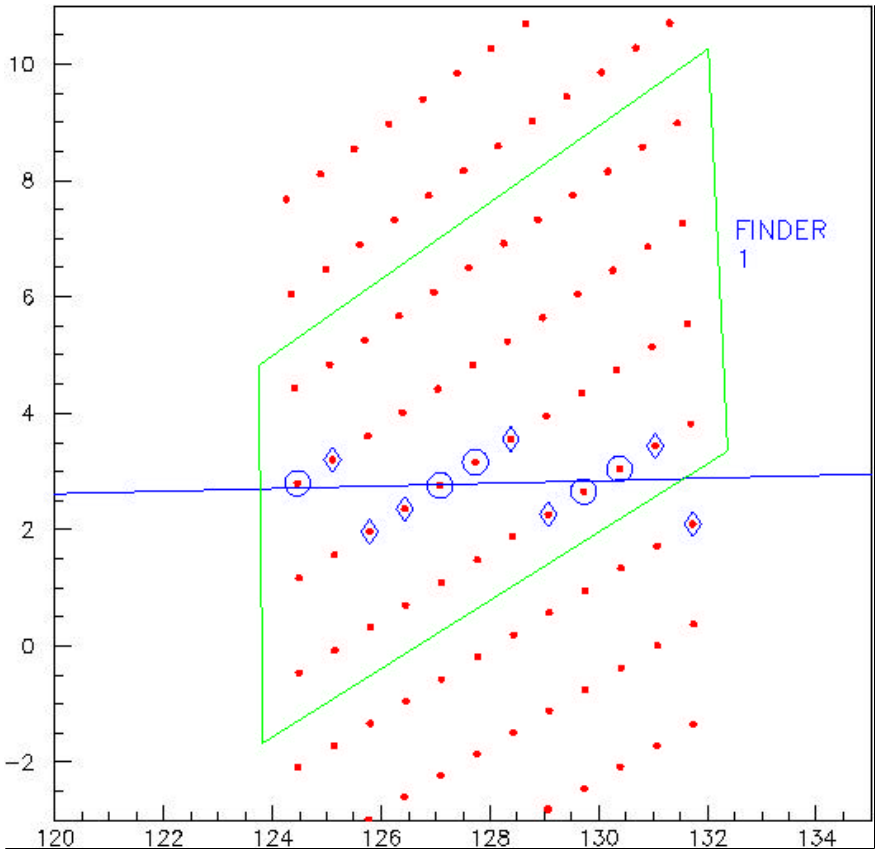


Example Finder Masks

Track with P_T = 1.0 GeV/c
(not a valid mask)

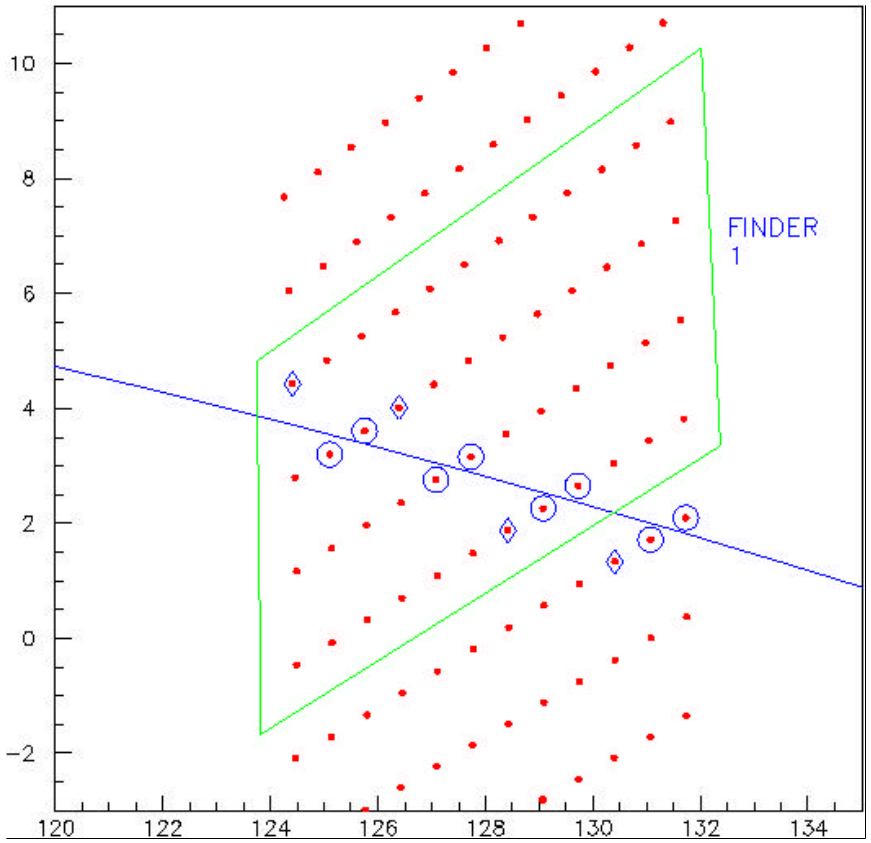


Track with P_T = 100 GeV/c
(a valid mask)

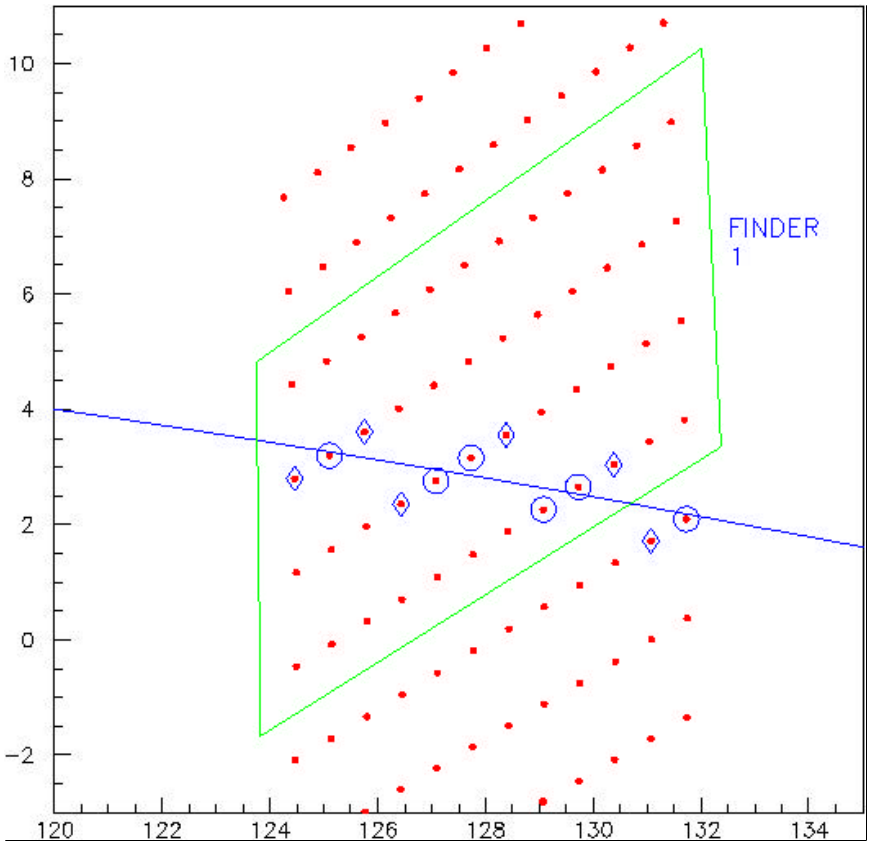


Example Finder Masks

Track with P_T = -1.0 GeV/c
(not a valid mask)

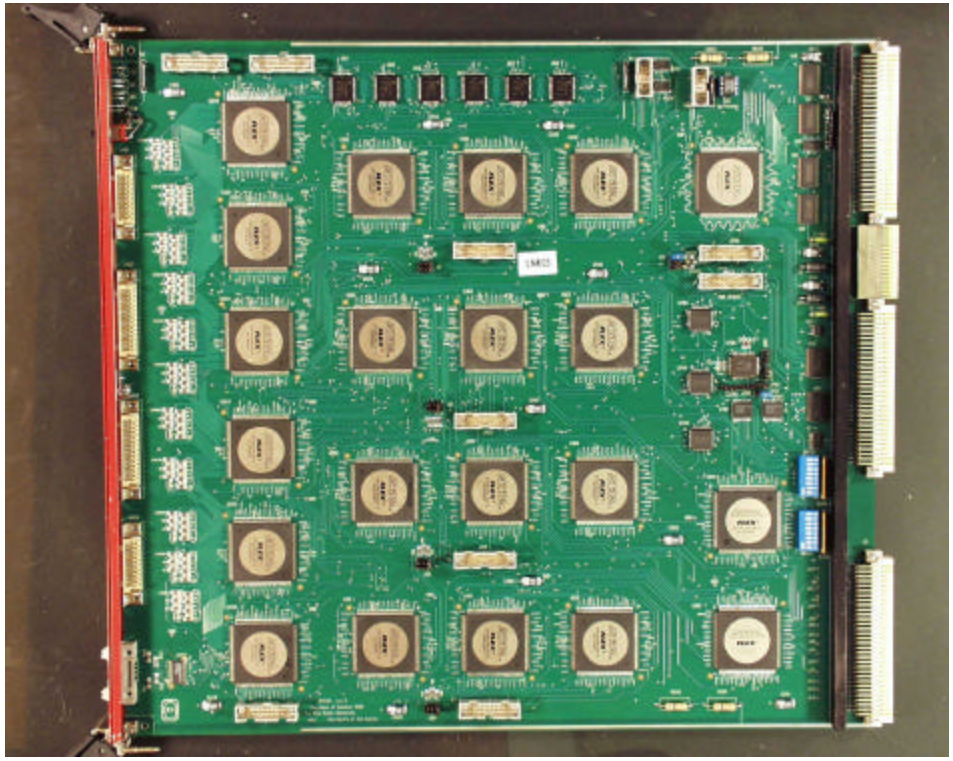


Track with P_T = -1.5 GeV/c
(a valid mask)



Linker Board

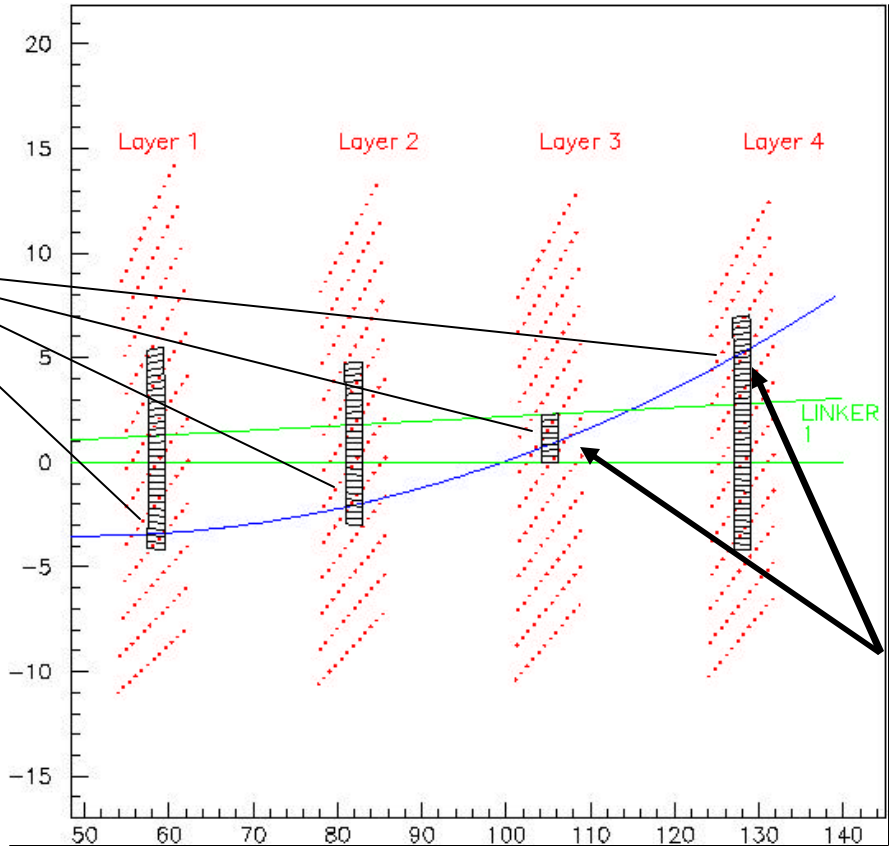
- Developed at OSU.
- Each linker chip contains all the roads needed to find tracks with transverse momentum > 1.5 GeV/c
- Each chip processes 1.25° of the chamber, and outputs the best found track in that phi-slice to the next stage in the trigger.
- There are twenty-four identical Linker Boards required for the full system. Each covers 15 deg. of the COT.
- 288 total Linker chips, 504 total PLDS
- Board programs are stored in EEPROM and Flash Ram



The Linker

Tracks are found by comparing fired **pixels** in all 4 axial superlayers to a list of valid **pixel** patterns or "**roads**".

Pixels must match



The Linker system divides the COT into 288 slices. Track linking is performed simultaneously in these slices.

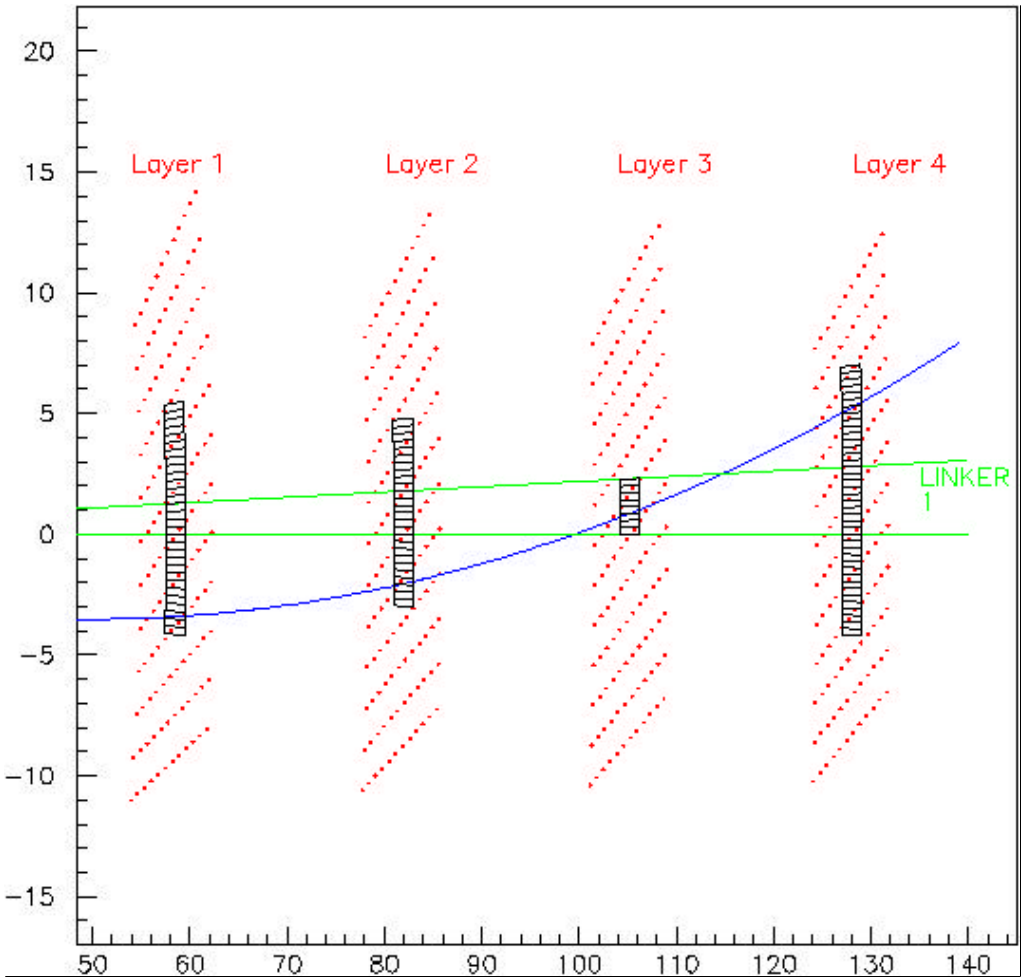
Slopes must match

The Linker

- Each Linker Chip reports the best track that passes through a 1.25° phi-slice located at the 3rd axial layer.
- Since tracks can curve in the magnetic field, this means that pixels outside of the 1. 25° phi-slice are needed

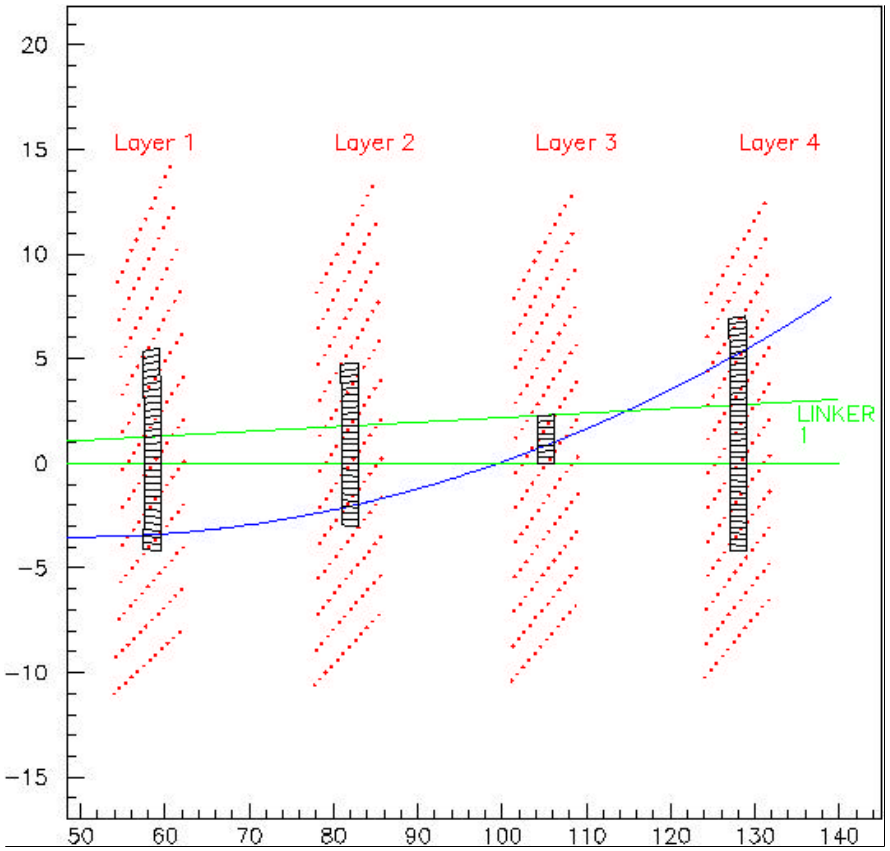
The total number of roads needed to find all tracks with P_T > 1.5 GeV/c in a linker is **2400**.

The number of roads grows as 1/Pt(min)

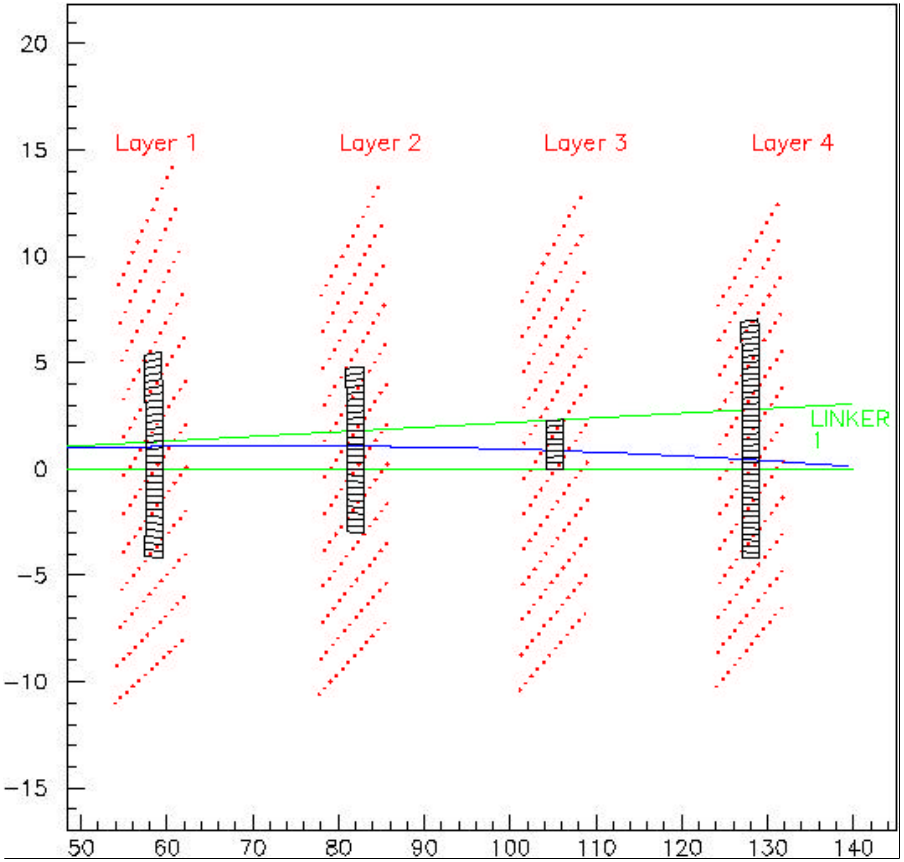


Example Linker Roads

Track with P_T = +1.5 GeV/c
(a valid road)



Track with P_T = -10 GeV/c
(a valid road)



Some Numbers

- How fast?
  - Capable of producing new track list every 132nsec
  - Time to produce a track from collision = 1.9?sec (~15 x 132nsec clock ticks)
    - XTC + Ansely Cable time(315nsec) + Finder(560nsec) + Linker(730nsec) + XTRP CableTime(90nsec)
  - Time for L1 decision: 5.5?sec
- Data at each stage
  - Input to Mezzanine: 16138 axial wires
  - Input to Finder: 32256 bits (prompt/delayed at each axial wire)
  - Input to Linker: (1344 cells)x(12pixels/cell)=16128 bits
  - Input to XTRP: (288 Linkers)x(12 bits)=3456 bits