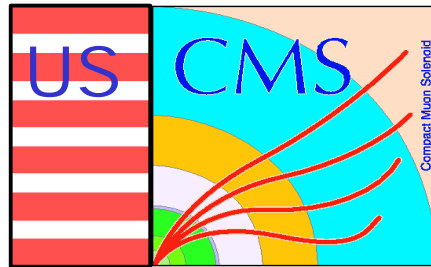


EMU Structured Beam Test Preparation



J. Gilmore
EMU Meeting
Gainesville, March 2003



Current Plans for CERN Test

- **Structured Beam Date at CERN**
 - May 23 – June 2: 50% muons, 50% pions (per Tracker request)
 - Begin setup May 15 at X5A, date confirmed
 - Followed by ~10 days of normal beam time, through June 12
 - X5A reserved by CMOS experiment, sharing arrangements made
- **Primary goal: validate crate electronics for ESR & production**
 - Test LHC synchronization scheme
 - Trigger performance tests with high-rate muons
 - Test 2 CSCs, TTC, DDU: multiple peripheral crates if possible
- **Other goals**
 - Include Sector Processor as L1 source if possible
 - All necessary equipment provided by trigger group
 - Test Slice DAQ as time & capability permit
 - Test in parallel readout path, Slice DAQ provides PC & software
- **Use CSCs from ISR storage**
 - Support stands shipped & assembled at CERN



Infrastructure at X5A

- **Needs for X5A test area**
 - Space for 2 CSCs on support stands & 2-3 VME crates
 - Gas supply & plumbing for 2 CSCs
 - Electricity outlets, space for HV racks, LV supplies
 - Scintillator paddles w/support stand (or similar) for triggering, plus associated electronics (NIM)
- **Needs for X5A control barracks**
 - Space & electricity for 2-3 PCs and 2 VME crates
 - Ethernet access, TTC input signals from beam
- **Cable distance from test area**
 - Cable/Fiber length for HV, LV and readout?
- **GIF inspired safety issues: still in progress**
 - Use only halogen-free cables
 - All cables/tubing must be clearly labeled
 - e.g. include “CMS-CSC” and name of responsible person



Equipment Needs (1)

Institution responsible for each of the following:

digital oscilloscope with probes	CMU
pulse generator for test trigger	CERN pool?
BNC/Lemo cables, tees, terminators and BNC-Lemo adapters	UCR storage?
scintillator trigger system & support stand	UCR storage?
2 CSCs and gas system	Levtchenko/Lanaro
HV supplies and cables, control	UF
cooling and tubing	not needed

Instrumentation for 2 CSCs (plus spare): most already on-chamber at ISR

AFEBS & cables to ALCT	(on CSCs)
10 CFEBs	(on CSCs)
10 CFEB-DMB cables (skew clear)	ISR
3 DDU-capable DMBs	OSU
3 TMBs with updated firmware	UCLA
10 CFEB-TMB cables (skew clear)	ISR
2 ALCTs with updated firmware	(on CSCs)
4 ALCT-TMB cables (skew clear)	ISR
2 LVDBs	(on CSCs)
power & cables to LVDB	UW (Lanaro)
2 LVMBs w/cables to DMB	UCD



Equipment Needs (2)

Crate equipment:

2 VME peripheral crates		OSU
1 full and 2 partial VME backplanes	UF	
2 Dynatam (slow control VME computers)	OSU	
1 10-base-T switch, cables/Tees/terminators	OSU	
3 CCBs		2 RICE/1 OSU
1 DDU with fiber spools for DAQ readout		OSU
1 Linux PC with gigabit/S-Link to readout DDU (1-2 fast hard drives, dual CPU with 64-bit/66MHz PCI)	OSU	
TTCvi/vx and support, for 2 CCBs	Rice	
NIM crates & Modules (delays, logic, etc)	CERN pool/UCR storage?	
CAMAC crate & controller, TDCs, etc		not needed
signal cables, short and long (Lemo/BNC)	CERN pool/UCR storage?	
Trigger/Test Control Board (TCB)	OSU	

Software:

Interim DAQ/Slow Control	OSU
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Beam Test Responsibilities (1)

- **Tasks and Equipment**
 - **A. Lanaro (at CERN)**
 - LV supplies and cables to LVDB (halogen-free)
 - Gas plumbing (from GIF area racks) and supply tanks
 - CERN liaison for X5A area, related logistics and other CERN red-tape
 - **P. Levtchenko (at CERN) plus V. Andreev, S. Otwinowski, B. Lisowski**
 - CERN transport issues (trucks, cranes, etc.)
 - 2 CSCs and Skew Clear cables from ISR
 - 2 CSC test stands (1 at ISR + 1 in transit from UCLA)
 - **J. Gilmore (OSU)**
 - 3 DMBs, 1 DDU, 2 crates, 2 Dynatems, 1 CCB, TCB and network hub
 - DAQ PC, all fiber for DAQ readout, DAQ software
 - **J. Hauser (UCLA)**
 - 3 modified TMBs for DMB-DDU readout
 - **A. Korytov (UF)**
 - 2 HV supplies for CSCs, plus a spare
 - Halogen-free HV cables for 2 CSCs [A. Madorsky]
 - 1 full and 2 partial custom backplanes
 - **P. Padley (Rice)**
 - 2 CCBs, 2 MPCs, TTC system + support (crate, PC, fiber)



Beam Test Responsibilities (2)

- **More equipment**
 - D. Zer-Zion (UCR): NIM equipment & misc. cables from UCR storage
 - A. Golyash (CMU): LeCroy LT364 Digital scope + probes
 - M. Tripathi (UCD): LVMB-DMB cables
 - P. Murray (UCD): Slice Test DAQ system needs
 - D. Acosta (UF): all Sector Processor system needs
 - TBD (CERN pool/UCR): NIM + misc. cables, scintillator trigger system
- **Manpower (~20 people needed)**
 - CERN/ISR: P. Levtchenko, others? (transport expert, CERN liaison)
 - CMU: N. Bondar, I. Vorobiev, A. Golyash (anode ADB expert)
 - OSU: J. Gilmore + 1 (DAQ + CFEB/DMB experts)
 - Rice: ? (CCB/TTC + MPC experts) [M. Matveev, S. J. Lee, G. Pawloski?]
 - UCD: R. Breedon, P. Murray (Slice DAQ expert)
 - UCLA: ? (ALCT + TMB expert) [M. von der Mey, B. Mohr?]
 - UCR: R. Clare, D. Zer-Zion, D. Futyan
 - UF: A. Drozdetski, Bobby? (CSC HV expert)
 - UW: A. Lanaro (gas and LV expert, CERN liaison)
 - Who else can commit time at CERN for beam test? Purdue?



Logistics

- **CERN shipment deadline**

- **Air shipments from U.S. by May 1 at latest!**

- **Ship to Peter Levchenko at CERN address**

- Petr Levchenko
CERN, EP Division
2 route de Meyrin
CH-1211, Geneve 23
Switzerland
Phone: 4179 201 0537

- **Inside CERN**

- Site Meyrin, Bat. 375, Entrance I-3
Phone: 160537

- **Finalize plans this week**

- **Approve equipment and responsables list, contact persons**
 - **Specific manpower needs and availability, names**
 - **Define preparation and shipping schedule**
 - **Additions/modifications to test plans**



Near Term Plans

- **Hardware Tests at UCLA (currently ongoing)**
 - Full TMB firmware is finally ready (last week)
 - Previous test proved TTC, DDU and DAQ software capability
 - Tests to perform now through end of April
 1. **Single CSC DAQ & Trigger tests at high rate**
 - Regular & random sources: anode, cathode, scintillator, ext. pulser
 - Verify that event & bunch sync are maintained with no bit errors
 2. **Multi-CSC tests & multi-crate tests**
 - Requires some software modifications
 - Repeat test modes above
- **Above testing includes**
 - **Peripheral crate electronics/firmware testing**
 - **Integration and performance shakedown**
 - Prove overall hardware/firmware/software capability for all modes
 - **Tune & test control/DAQ software**
 - Prepare operation routines for CERN tests
 - TTC & MPC implementation tests
 - **Test implementation of multi-CSC Event Display**