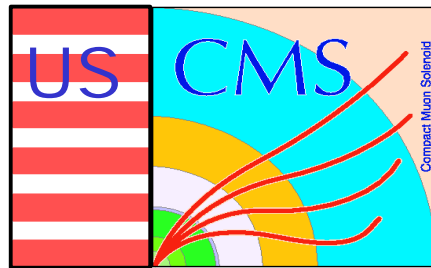


# ***EMU Beam Tests 2003: Technical Details***



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*EMU Meeting, FNAL*  
*October, 2002*



# ***EMU Test Goals: Review***

- **Goals before spring 2003**
  - **Simultaneous operation of multiple CSCs (2-3)**
    - **Production versions of on-chamber electronics**
    - **Common gas, cooling, HV, LV, Slow Control and DAQ systems**
      - **Implement TTC and DDU, Slow Control compatibility for Slice test?**
  - **Synchronization, calibrations, continuous slow control monitoring**
  - **Two crate operation modes**
    - **All CSCs readout on one full backplane**
    - **CSCs readout on 2-3 individual small backplanes**
      - **Simulates multi-crate operation; tests TTC and Slow Control (Dynatem)**
  - **Final pre-production versions of crate electronics**
  - **Trigger and DAQ: rate/performance analysis**
- **Test categories**
  - **Hardware performance tests: trigger and DAQ rate capability**
  - **Integration tests: timing, slow control, DAQ/trigger/run control**



## *Integration Tests*

- **Assume basic operations completed**
  - Multiple CSCs with gas, cooling, HV, etc.
  - Cosmic/scintillator and calibration pulse timing ready
- **Slow Control, configuration and monitoring**
  - Use what is available now, implement DCS later...
  - Board initialization
    - Hard/soft resets, load constants (DAC, masks, etc)
    - Boards ready-to-go after reset! (No Slow Control initialization req'd)
  - Calibration setup and pulse generation
  - LVDB power on/off control
    - Add crate and HV power control later
  - Status monitoring: board errors & temperature/voltage/current
- **DAQ/Trigger/Run Control**
  - Trigger control (TTC and/or OSU Test Control Board)
  - Event readout (via DDU), storage, display: on/off-line processing
  - Communicate with Slow Control: later, when DCS is ready



## Performance Tests

- **What can be done at FAST sites?**
  - **Calibration tests**
    - Trigger/Readout rate capabilities, DAQ volume limitations
    - Regular and Random triggering at high rate (OSU Test Control Board)
  - **Pulse pattern generation for trigger testing**
    - Trigger efficiency/performance
  - **Cosmic ray testing**
    - Scintillator trigger mode (LCT & L1A, synched by OSU TCB?)
    - Self-trigger LCT mode, use scintillator L1A or LCT == L1A?
    - A/CLCT trigger threshold/efficiency tests
      - ALCT.and.CLCT & ALCT.or.CLCT operation tests
    - ALCT/CLCT/TDC BX timing variance
    - DAC & HV threshold effects on efficiency?
    - Position resolution studies?
  - **Continuous Slow Control monitoring**
    - Includes FMM functionality too (via VME for now)



## Testing Plan: Phase I

- **Phase I Testing: hardware rate tests, one CSC first**
  - Requires LHC-realistic firmware capabilities for FULL EMU system
    - Multi-event buffering for Anode & Cathode DAQ data (~10 events?)
    - Minimal readout of Anode & Cathode DAQ data (localized in space and time)
      - Full/extended dump is prescaled or on demand only!
    - Full pattern finding capability: prove it fits (and works) in the FPGA
  - DAQ Tests: Random LCT and L1A with known average rates
    - Realistic event volume at LHC rates, readout via DDU
      - Random LCT (with Calibration Pulse?) from OSU TCB via CCB front panel
      - Randomized active CFEB triggers **from TMB firmware**, coordinated with Anode LCT generation; Random L1A from TTC or TCB via CCB
    - No DAQ analysis software needed?
      - Event display may be useful, online or offline, to verify settings and functionality
      - Monitor DDU status for errors and buffer overflows/warnings
  - Trigger Tests: how to generate correlated A/CLCT at high rates?
    - Source(s) centered on A/CFEB and/or at boundaries between FEBs?
    - Random Buckeye pulse patterns at high rate? What about anodes?
      - Include cosmics with the above options? Self LCT or Forced LCT?



## Testing Plan: Phases II & III

- **Phase II Testing: multi-CSC tests**
  - Repeat Phase I rate tests with 2 CSCs in one crate
  - Perform “low rate” tests with cosmics
    - Gives correlated Anode & Cathode triggers in all CSCs
    - Collect multi-CSC cosmic data for analysis & reconstruction tests
  - May need improved event display/reconstruction capability
    - How to display a muon passing through multiple CSCs?
    - Histogram booking, etc. for multiple CSCs
- **Phase III Testing: multi-crate tests**
  - Similar to Phase II tests
  - Requires multi-CCB communication w/coordinated fast control
    - TTC and/or OSU TCB board
      - TTC support from Rice: 6U crate, TTCvi/vx, and PC with software
  - Requires multi-Dynatem communication for slow control
    - Current “CFEB Control” software is sufficient basically as-is



# Equipment Needs (1)

Institution responsible for each of the following:

digital oscilloscope with probes		FAST
pulse generator for random trigger		FAST
BNC/Lemo cables, tees, terminators and BNC-Lemo adapters		FAST
scintillator trigger system		FAST
3 CSCs and gas system	FAST	
HV supplies and cables	FAST	
cooling and tubing	FAST	

Instrumentation for 3 CSCs\*\*: already at FAST sites, CSCs & electronics available

AFEBs	CMU
AFEB-ALCT cables	CMU
15 CFEBs	OSU
15 CFEB-DMB cables	OSU
3 DMBs	OSU
3 TMBs	UCLA
15 CFEB-TMB cables	UCLA
3 ALCTs	UCLA
ALCT-TMB cables	UCLA
3 LVDBs	UW
power cables to LVDB	UW
power cables from LVDB	UW
LV power (400 Hz source?)	UW
3 LVMBs	UCD



## Equipment Needs (2)

### Crate equipment\*\*:

VME peripheral crate(s)	FAST
full and 3 partial VME backplanes	FAST
Dynatem (slow control VME computers)	OSU/FAST
1 10-base-T switch, cables/Tees/terminators	FAST
3 CCBs	RICE
1 DDU with fiber spools for DMB readout	OSU
1 Linux PC with gigabit/S-Link to readout DDU (1-2 fast hard drives, dual CPU with 64-bit/66MHz PCI)	OSU
TTCvi/vx and support, for 3 CCBs	Rice
NIM crates & Modules (delays, logic, etc)	FAST
CAMAC crate & controller, TDCs, etc	FAST
signal cables, short and long (Lemo/BNC)	FAST
Trigger/Test Control Board (TCB)	OSU

### Software:

DCS Slow Control (Dynatem/VME/JTAG routines)	UCR
Temporary Slow Control (Dynatem/VME/JTAG routines)	FAST/OSU
Trigger/Run Control	FAST/OSU
DAQ (CAMAC/VME/G-bit readout & storage)	FAST/OSU

**\*\*Some equipment may already be present at FAST sites.**



## ***Proposed Schedule (1)***

- **Phase I & II Hardware Tests at UCLA (January 2003)**
  - **First perform 1 CSC DAQ/Trigger rate tests**
    - **Multi-CSC tests follow immediately**
    - **Immediately followed by Phase III multi-crate tests if time allows**
  - **DAQ: calibration pulses, randomize active A/CFEB LCTs at TMB**
    - **Average 1.5 CFEBs hit per CLCT**
    - **Localized AFEB readout, use Cathode Calibration L1A as LCT**
  - **Trigger: Use cosmics/source(s)?**
    - **Can this give high-rate triggers (anode & cathode, multi-CSC)?**
- **Multi-Crate operation, UF/UCLA (February 2003)**
  - **Concurrent with Multi-CSC testing if possible**



## ***Proposed Schedule (2)***

- **Maintain operational testing capability afterward**
  - **Functional for few weeks to allow add-on upgrades**
    - **Allows additional time for Structured Beam and SLICE test prep.**
    - **Slow control improvements, DAQ/Trigger/TTC tuning, etc.**
      - TTC and local run control integration tests?
      - UCD DAQ/reconstruction software tests? With multiple PCs using XDAQ?
      - Test Dynatem (or replacement G-Bit to VME) with UDP protocol?
    - **Integrate new L1 Trigger hardware: date?**
- **LHC Structured Beam Test at CERN (May 19, 2003)**
  - **GIF or H2 test area? How many CSCs?**
    - **Synchronization tests with structured beam at H2 (1 week)**
      - Preceded by ~1 week setup
    - **GIF later (with standard beam) for rate tests with background?**
      - Few days for transfer/setup and ~1 week for testing
- **Slice test at CERN SX5 (2004)**