

D741C

CMS CSC Front End Card FPGA

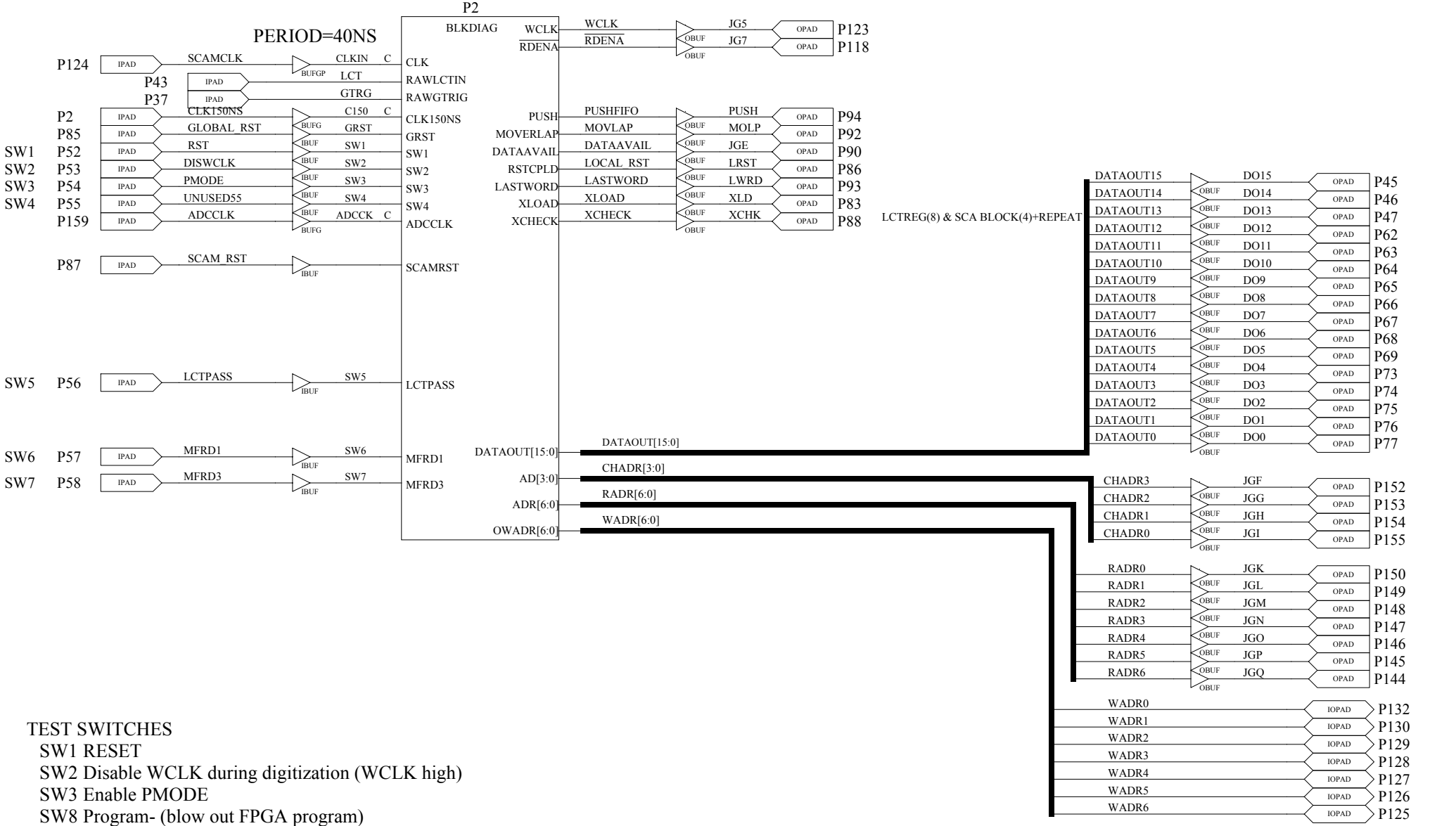
SCA Master Controller

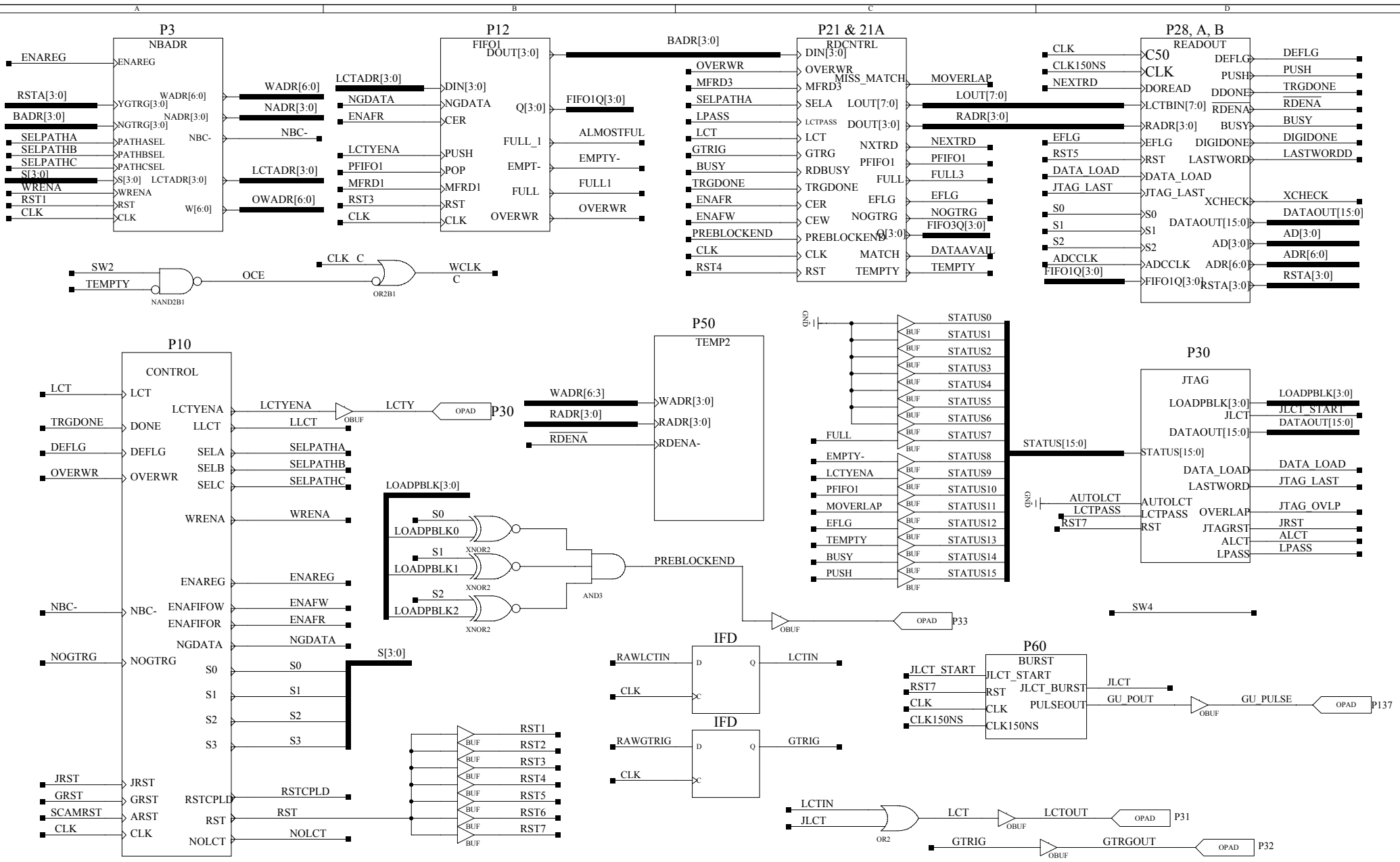
FEBRDCA

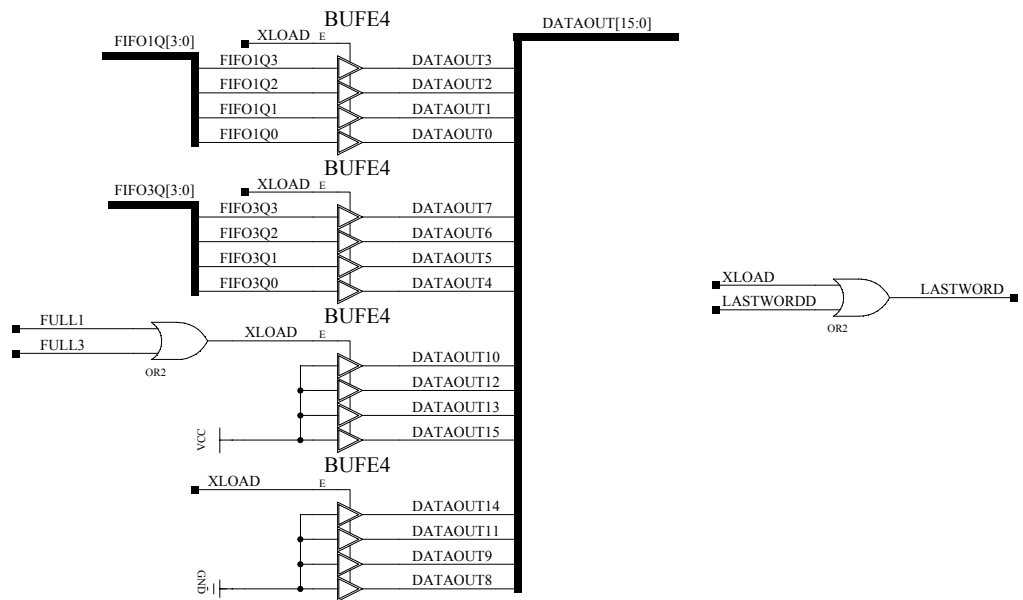
ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

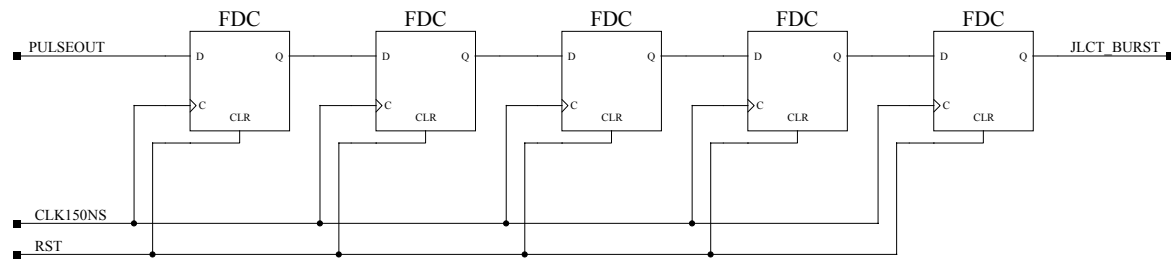
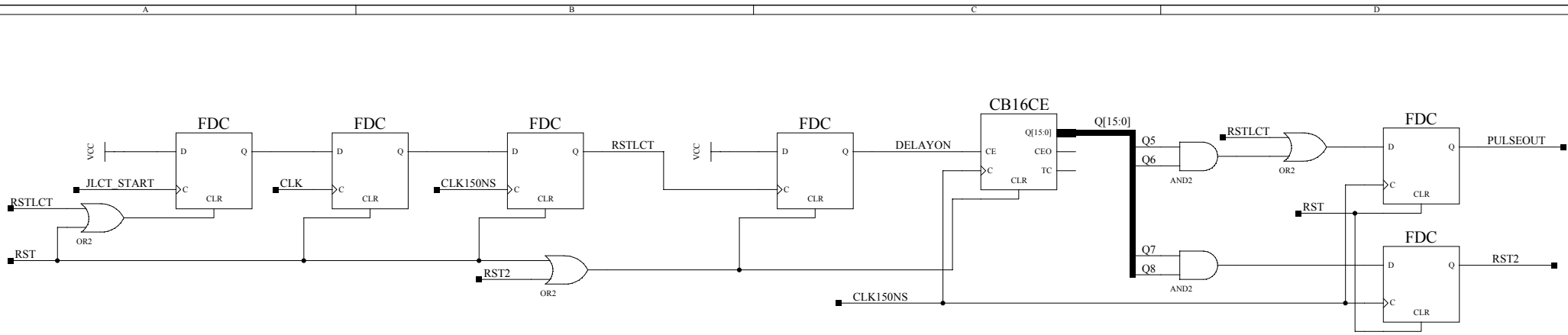
Device XC4010E3-PQ160

See M:\WV\D741C\SCAM\SCAM.UCF for special pin and timing constraints.



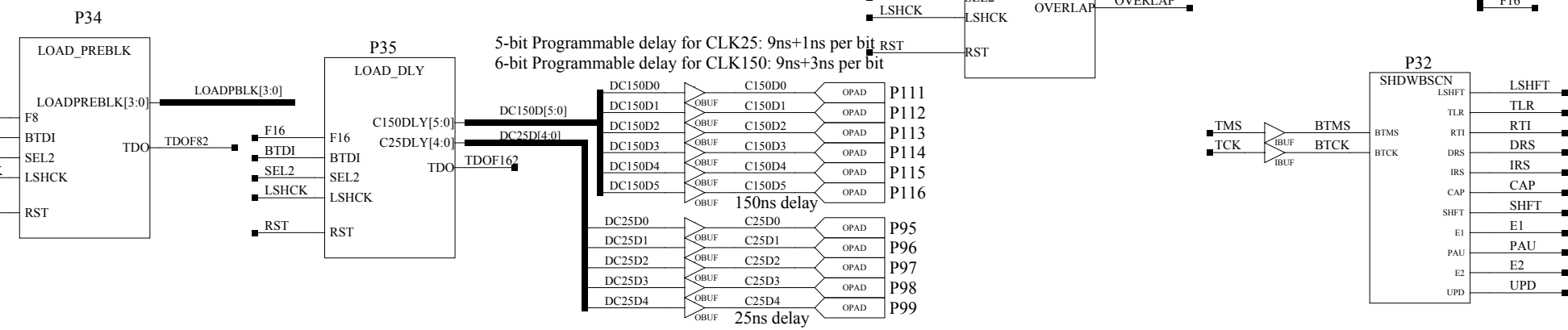
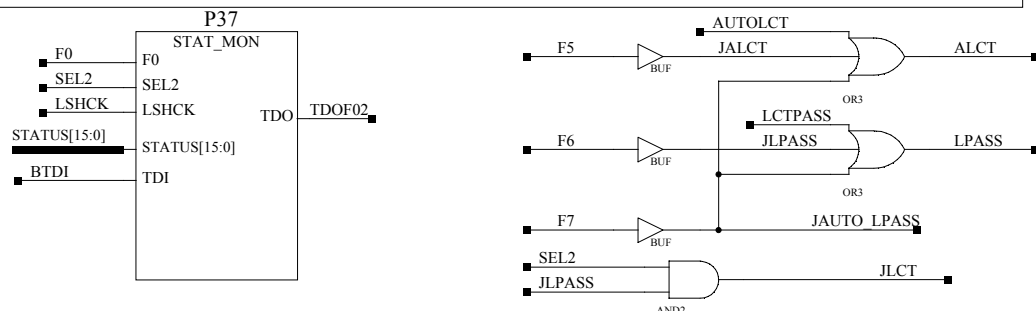
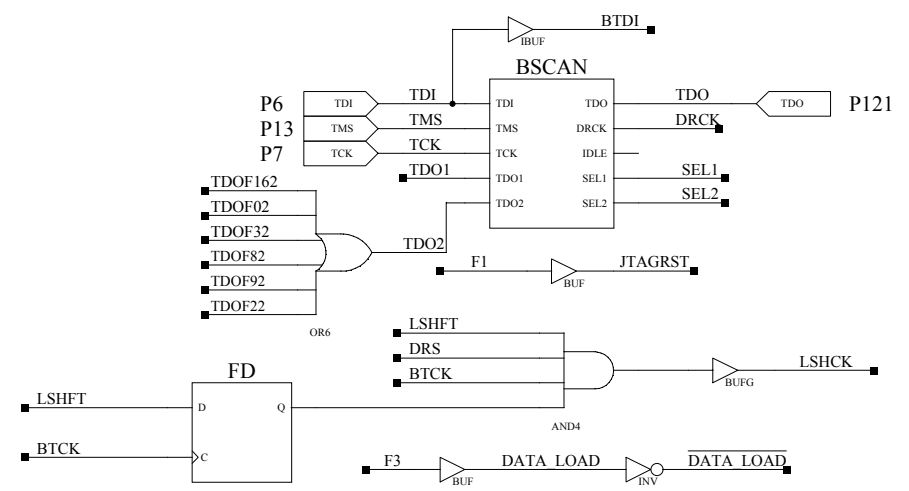


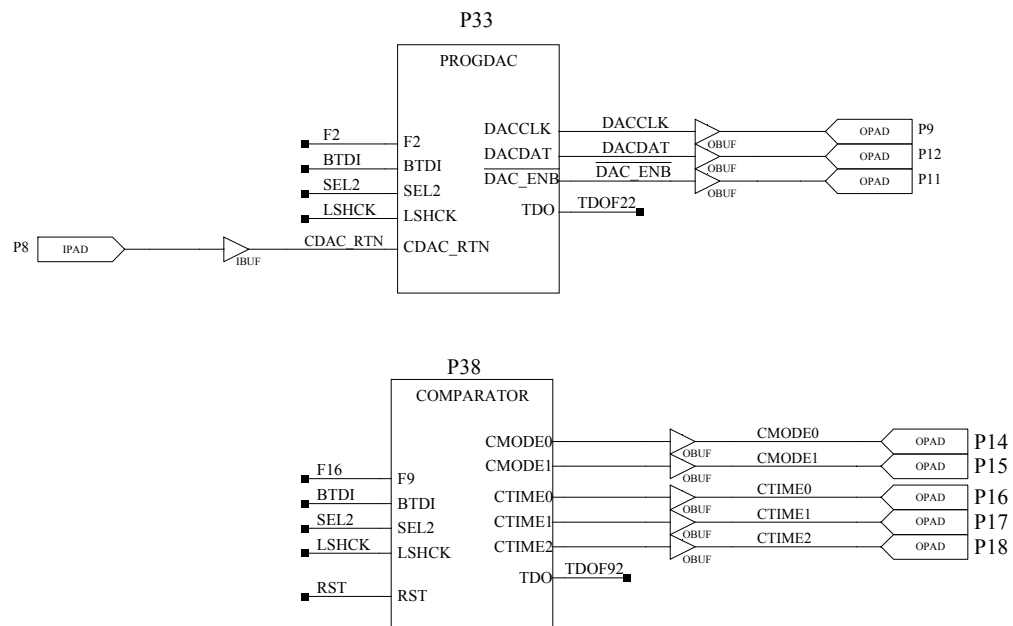


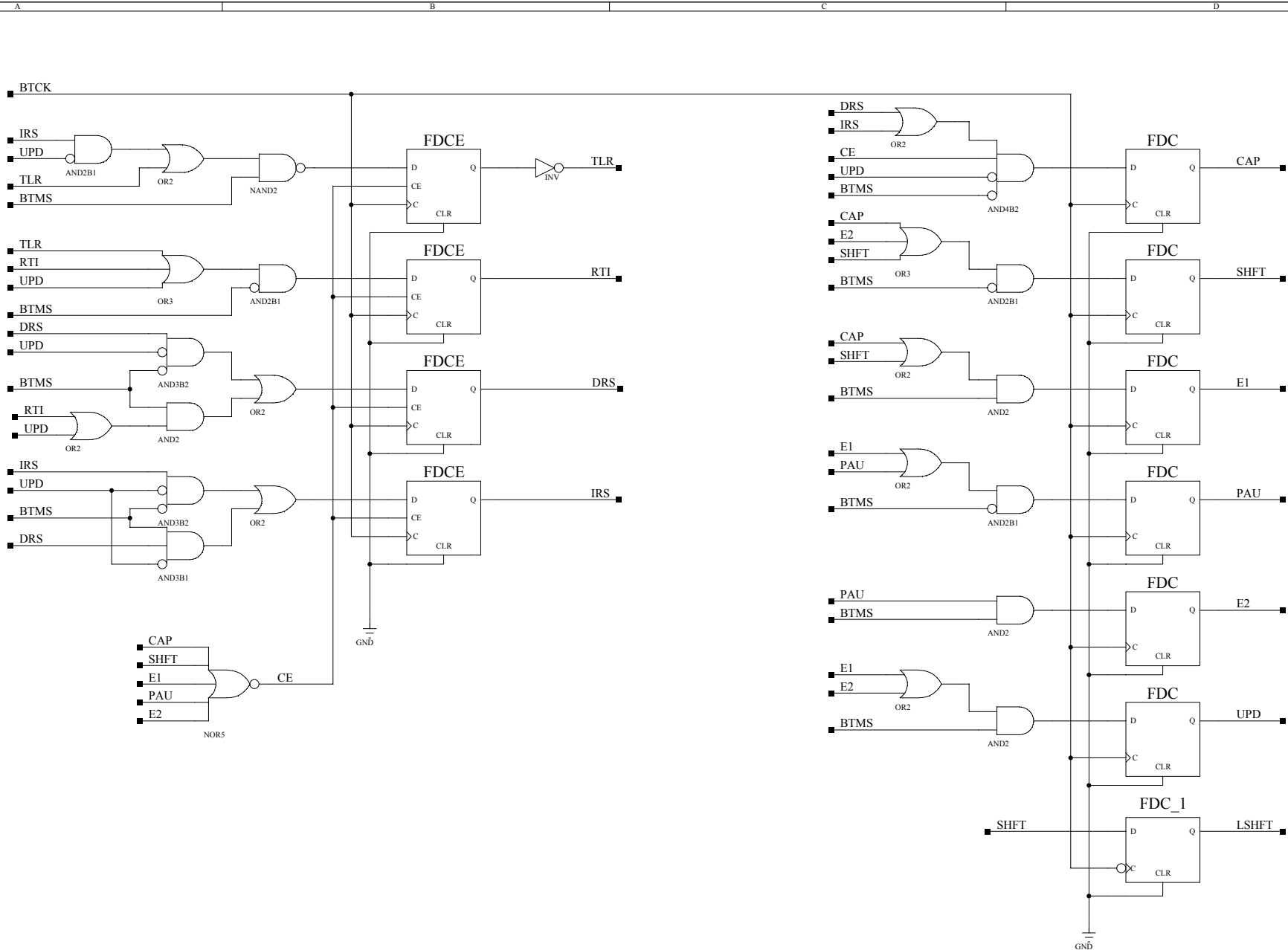


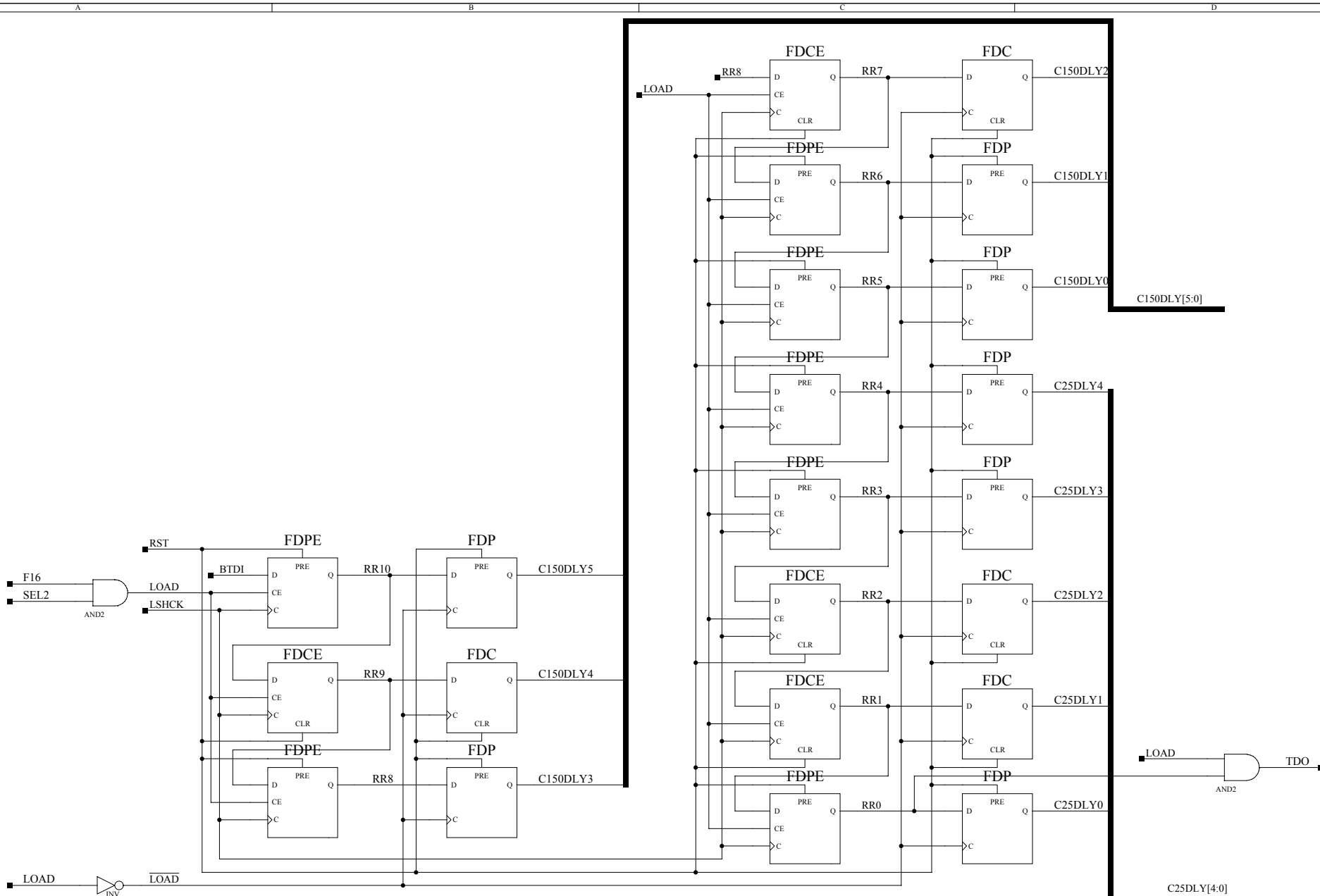
JTAG Instruction Decode

OpCode	Function [OpName]
0	Check FEB Status [CHECK_FSTAT]
7	1 SCAM Reset []
	2 Program Comparator DAC []
	3 Load Data & Send to Mbrd []
1	4 Load Shankar's comparator settings (5-bits)
4	5 Auto LCT []
5	6 LCT Pass (SEL2 is LCT) []
6	7 Auto LCT & LCT Pass []
	8 Load PRE_BLOCK_END
	9 Load COMPARTOR mode and time
16	Load Clock Delays (11-bits)

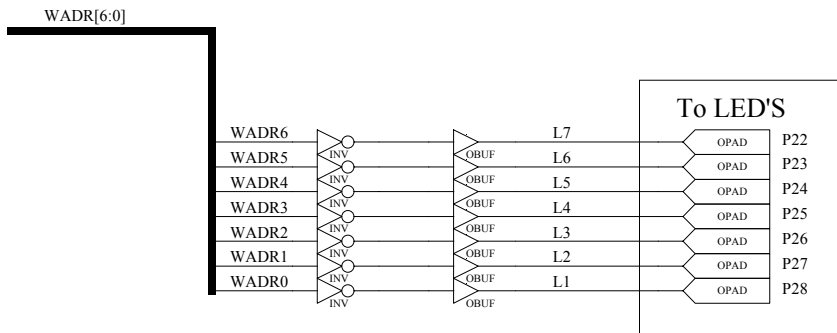
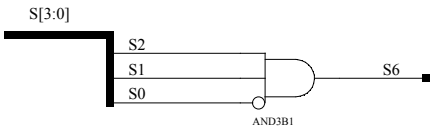
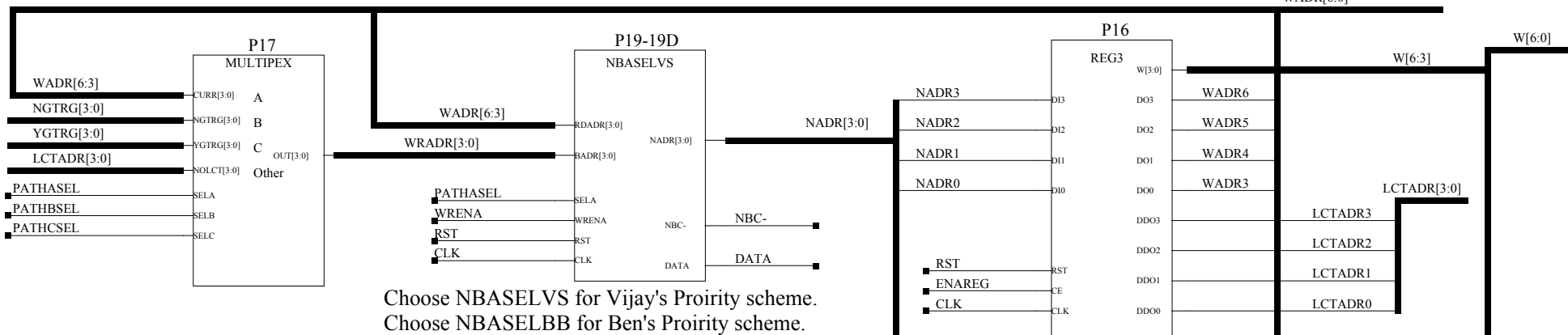


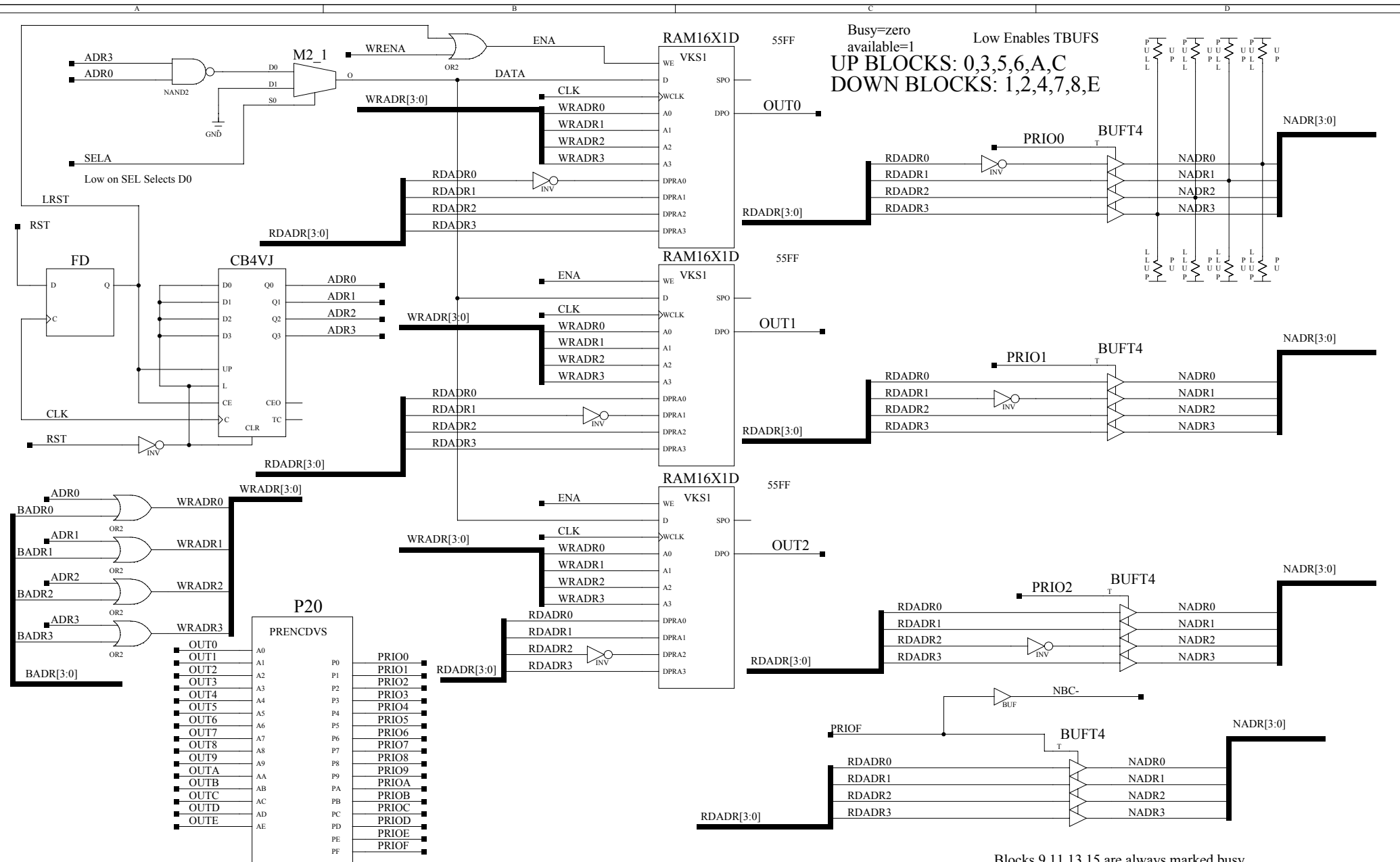






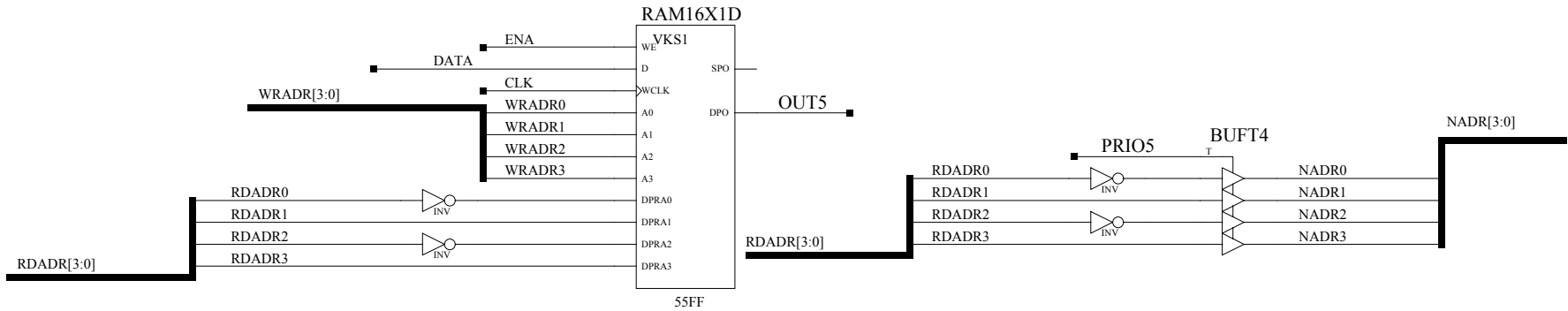
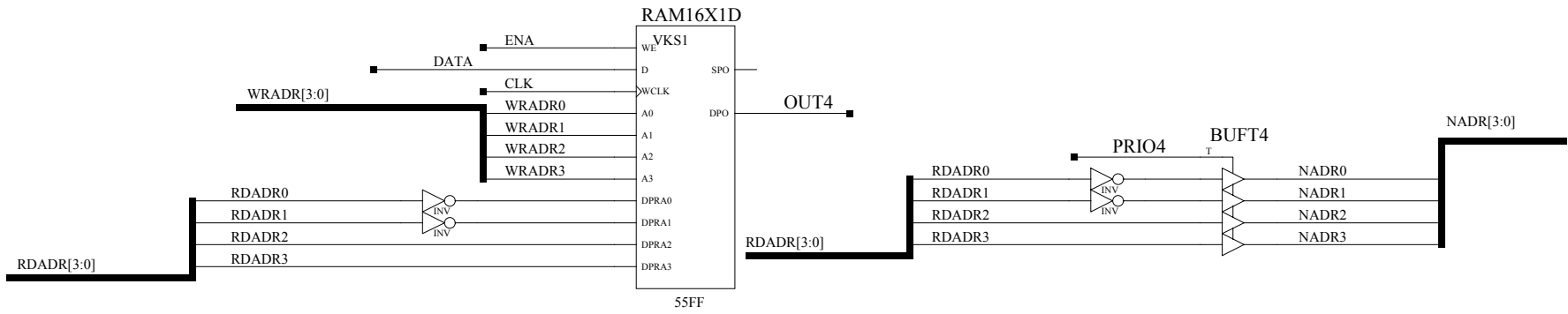
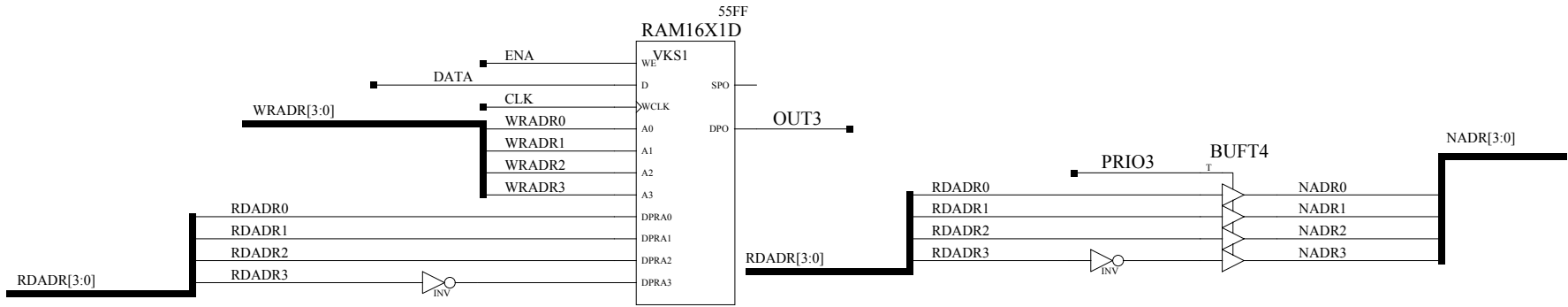
Current Block Address

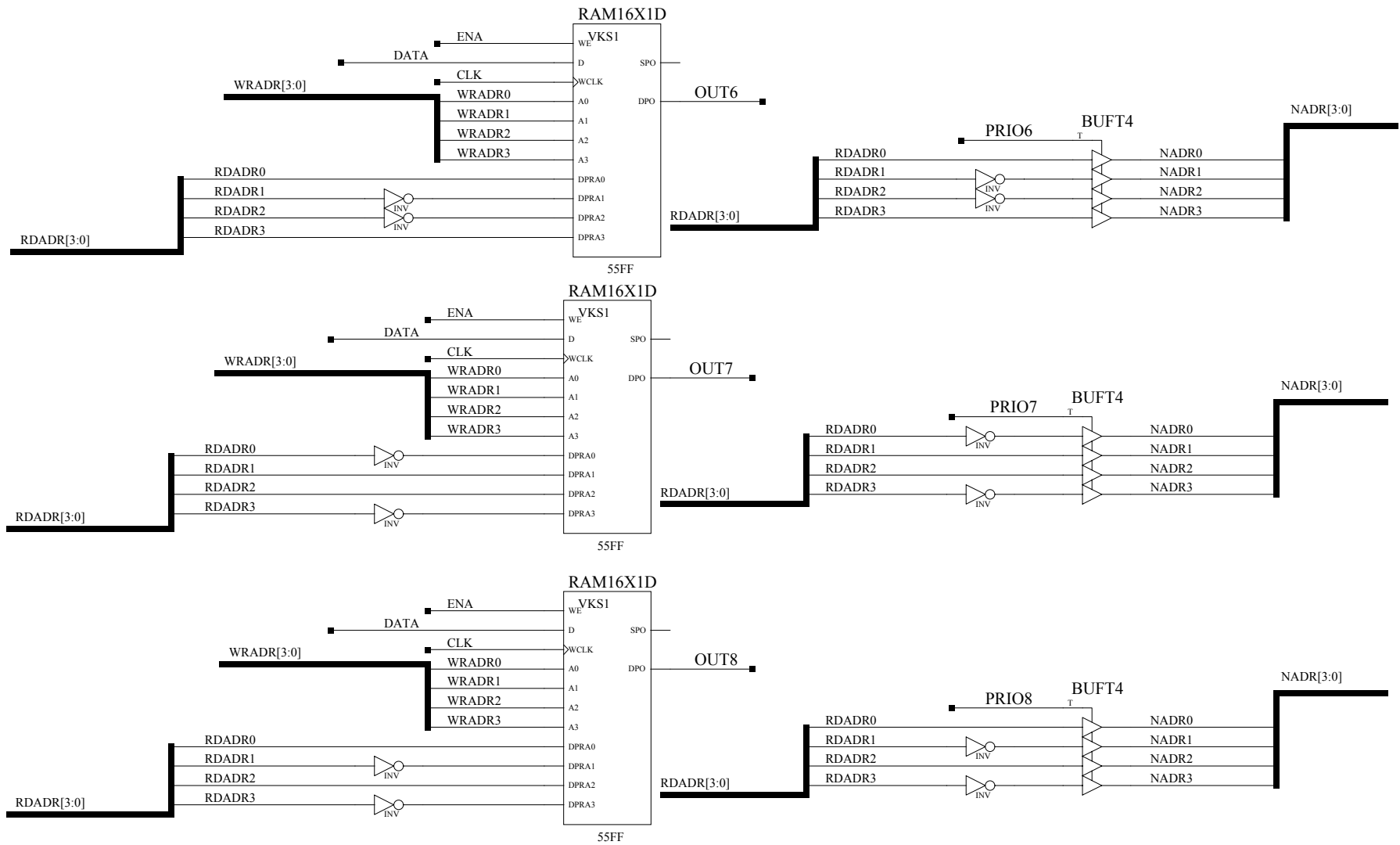


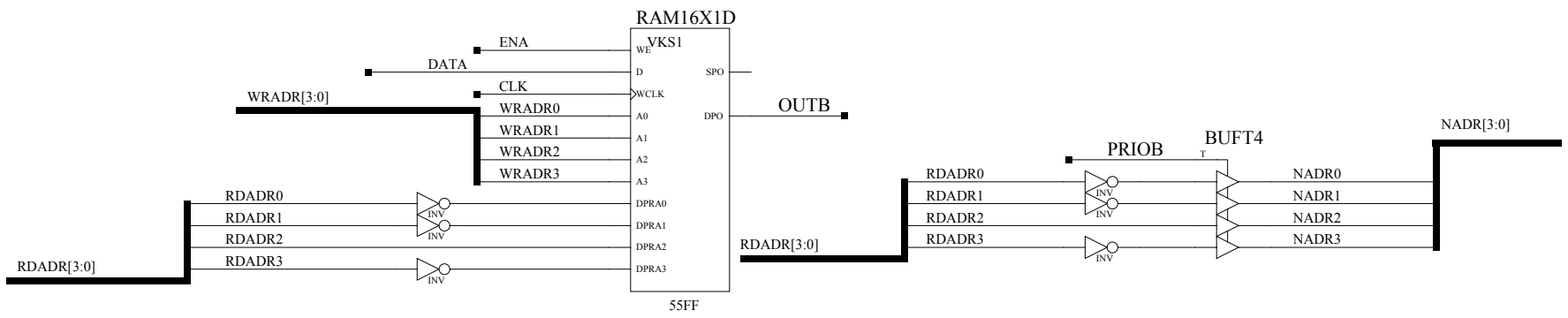
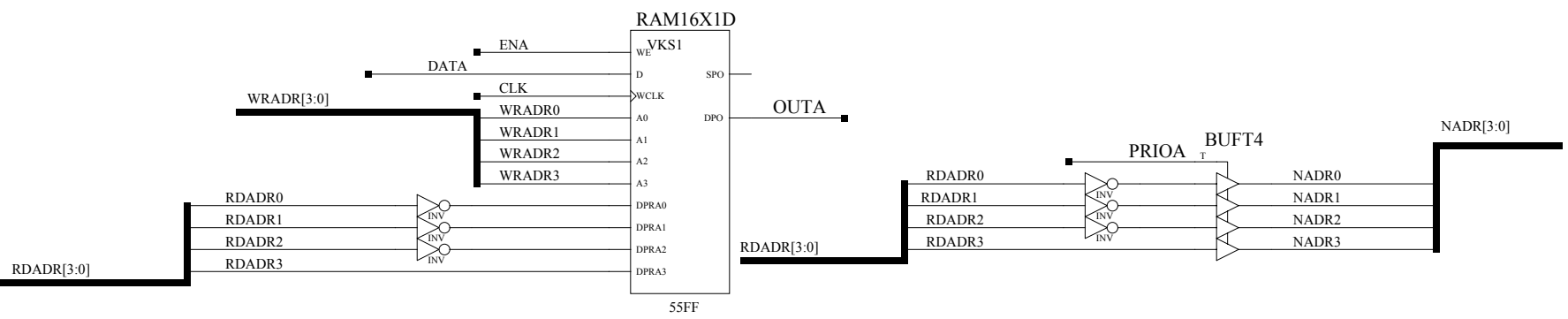
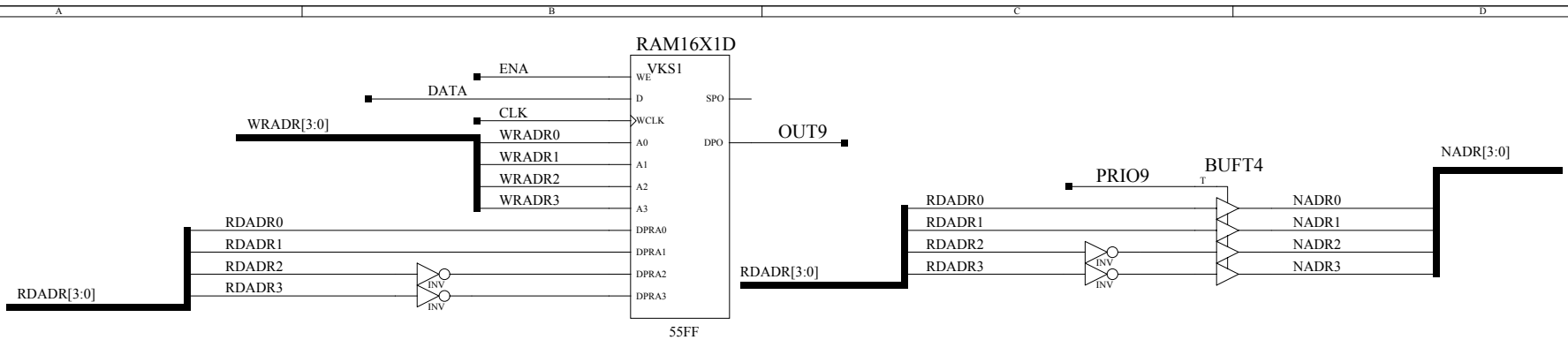


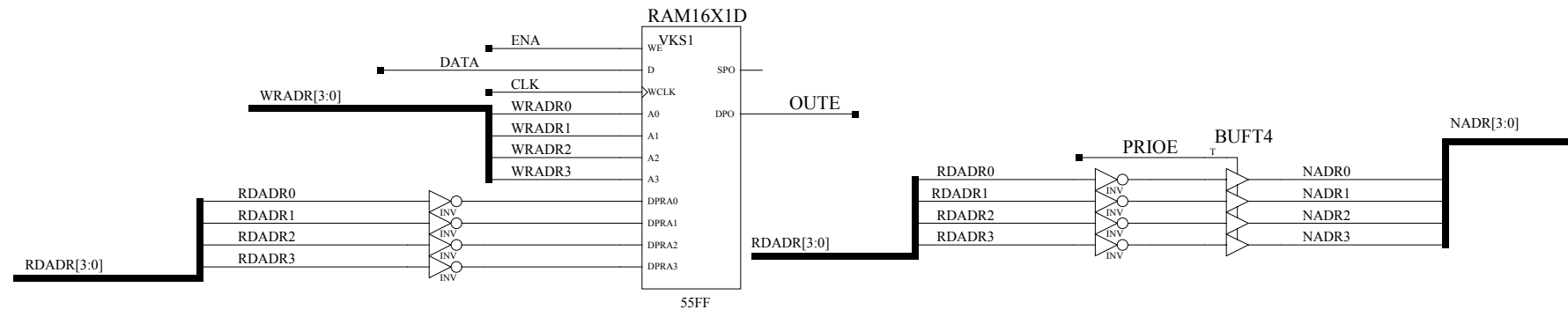
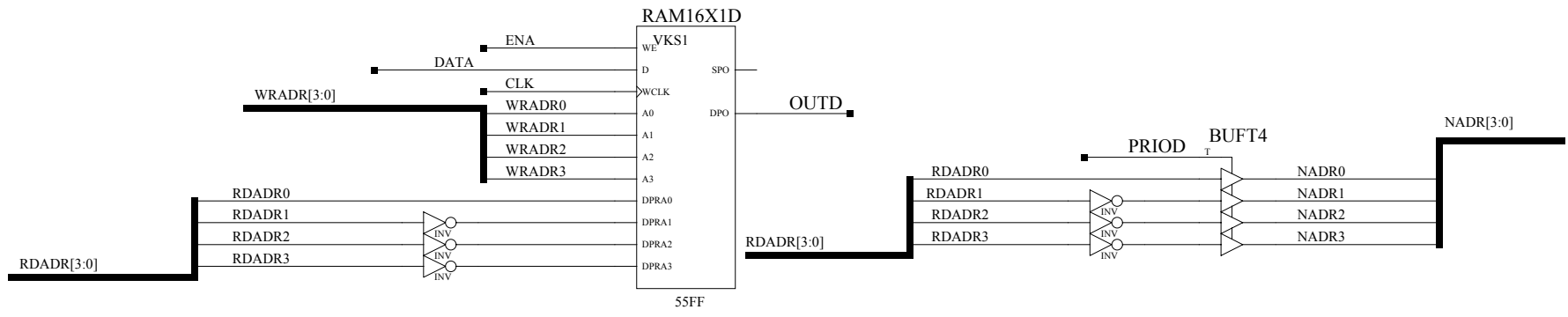
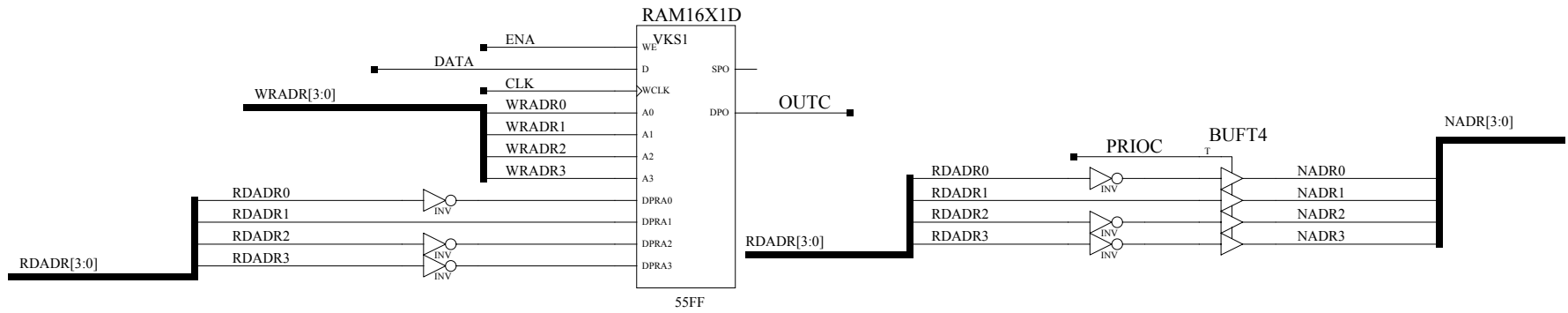
Busy=zero
available=1
UP BLOCKS: 0,3,5,6,A,C
DOWN BLOCKS: 1,2,4,7,8,E

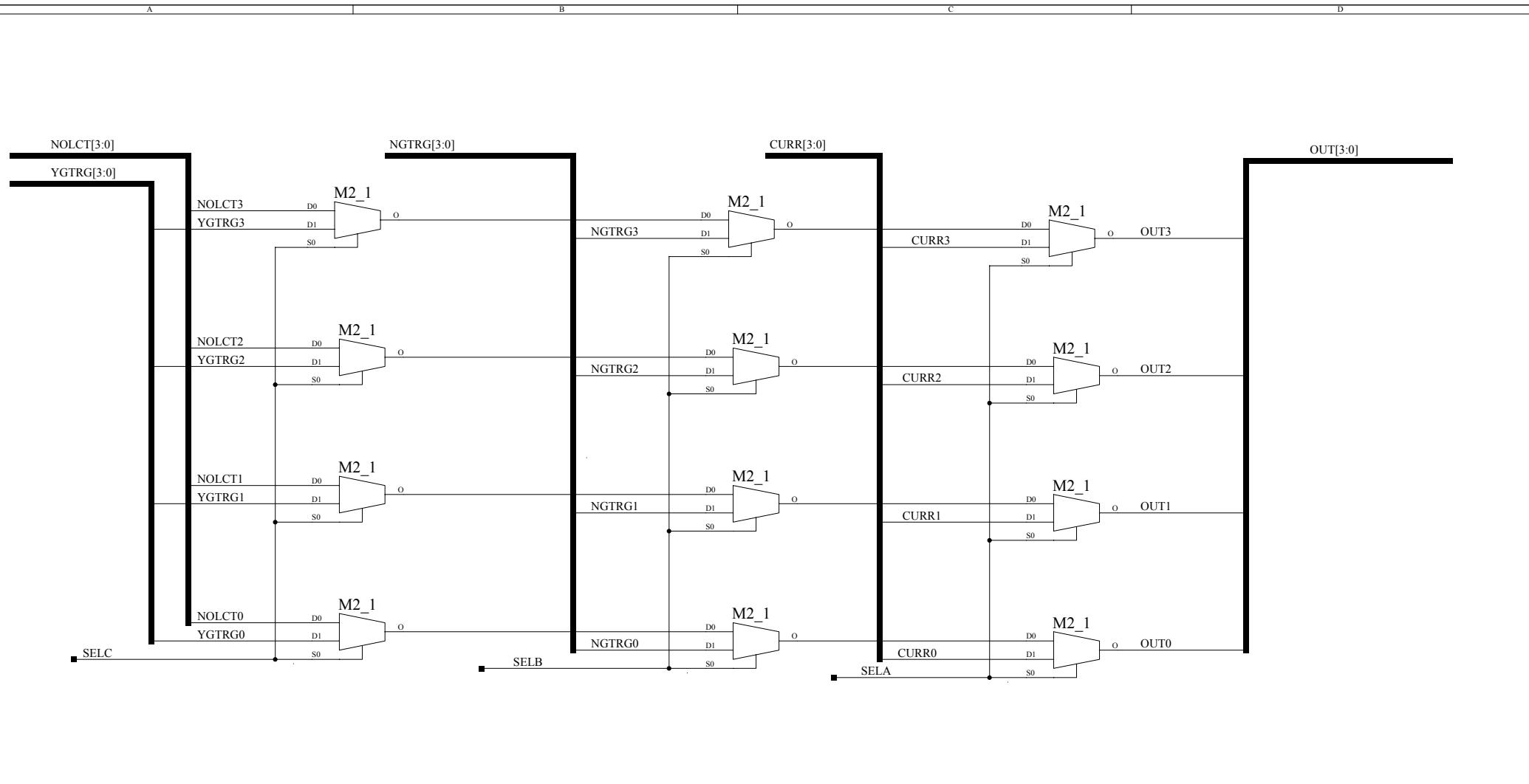
Blocks 9,11,13,15 are always marked busy.



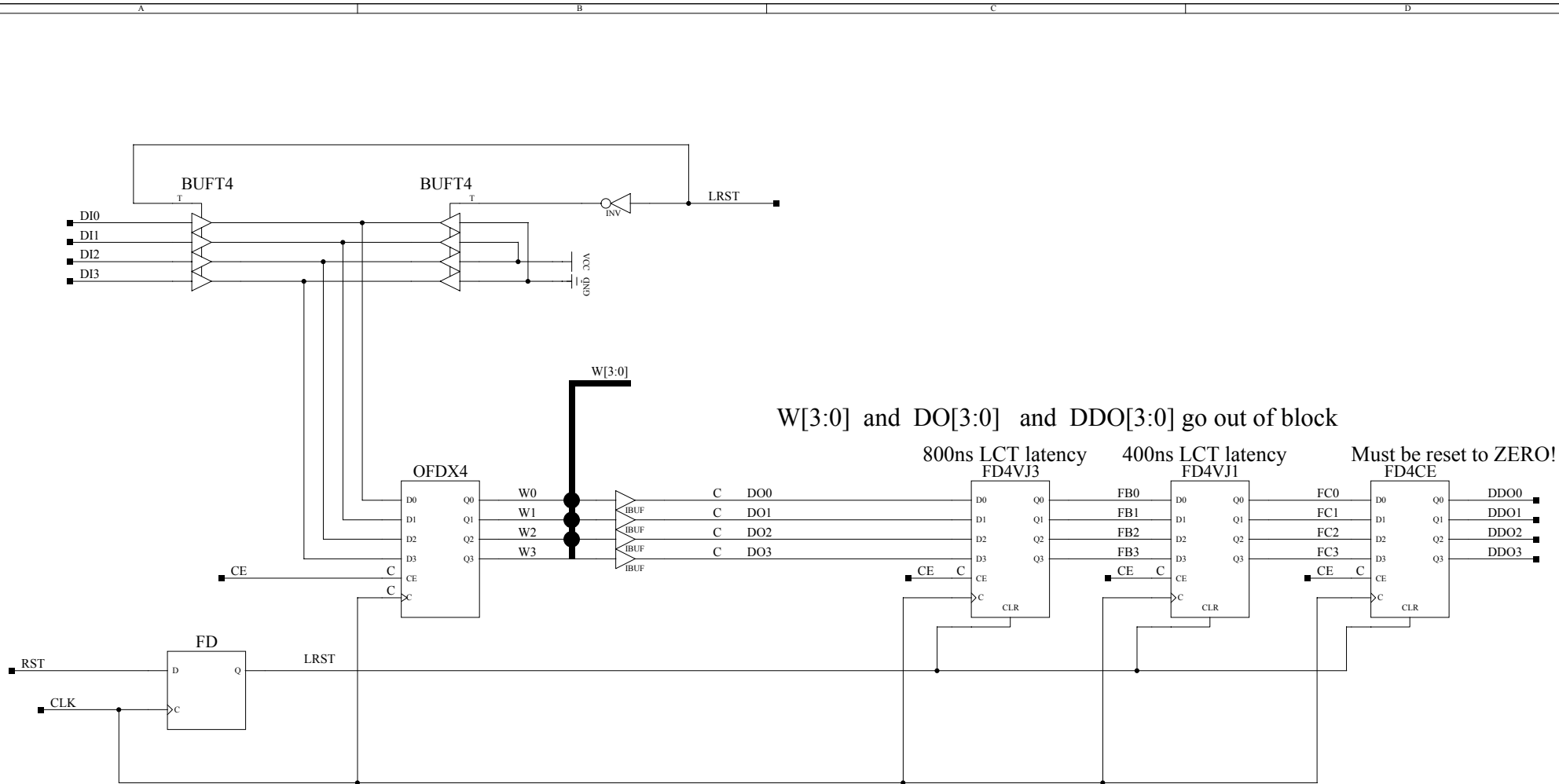


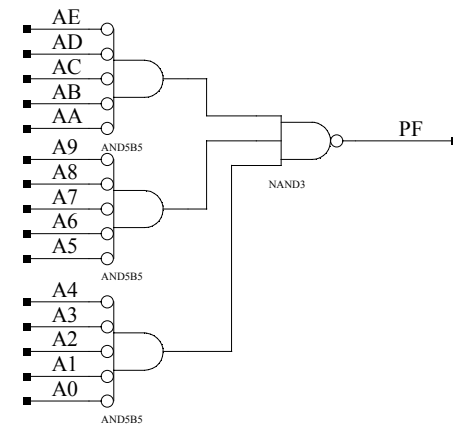
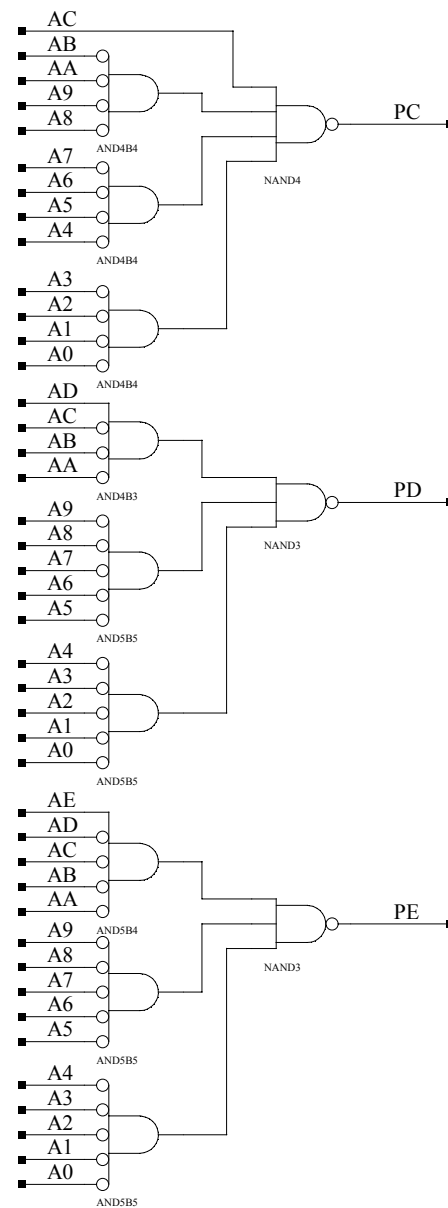
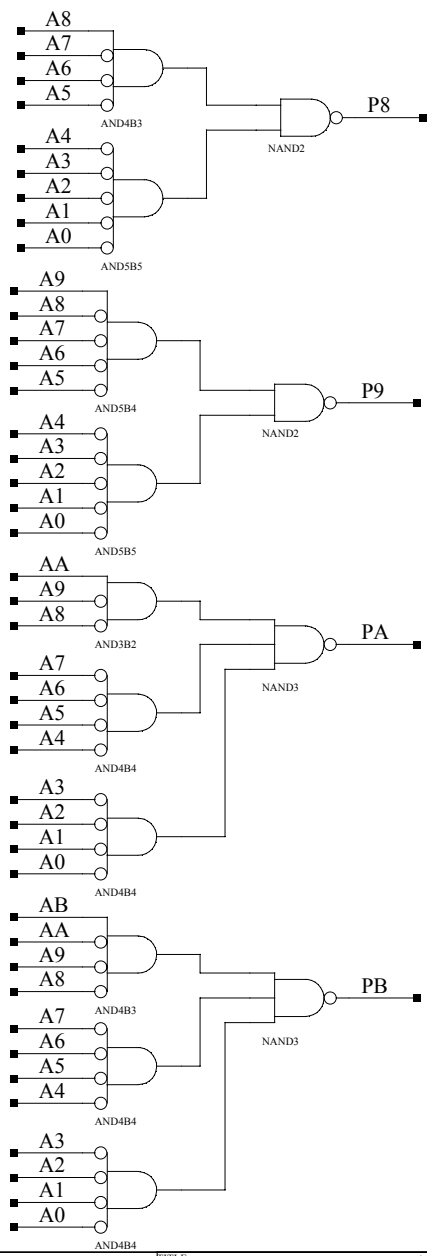
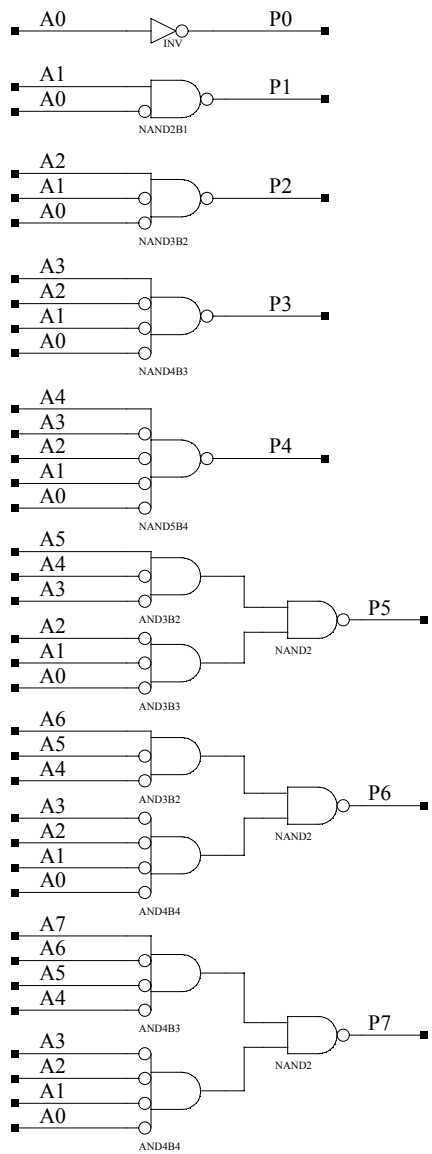




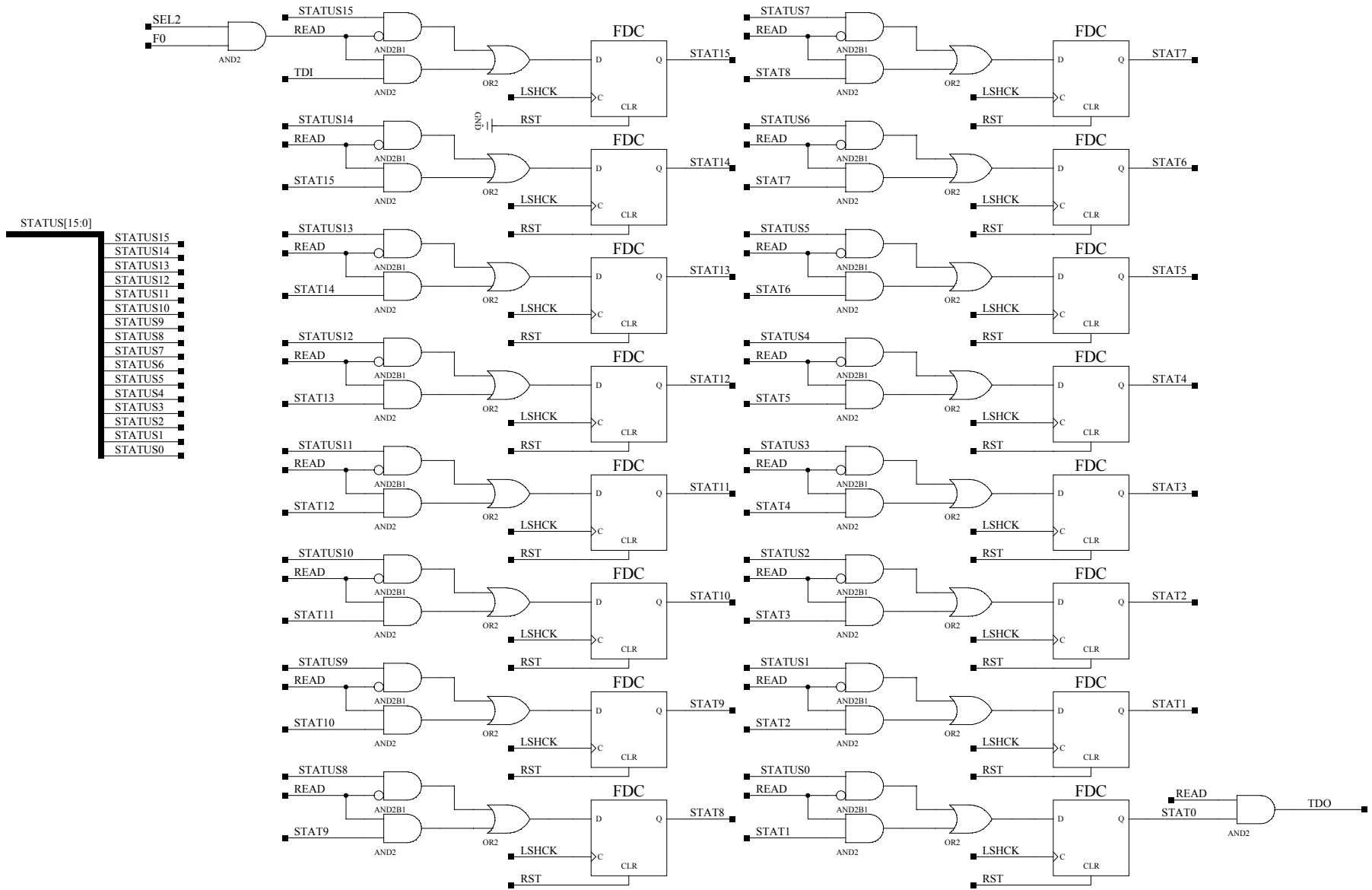


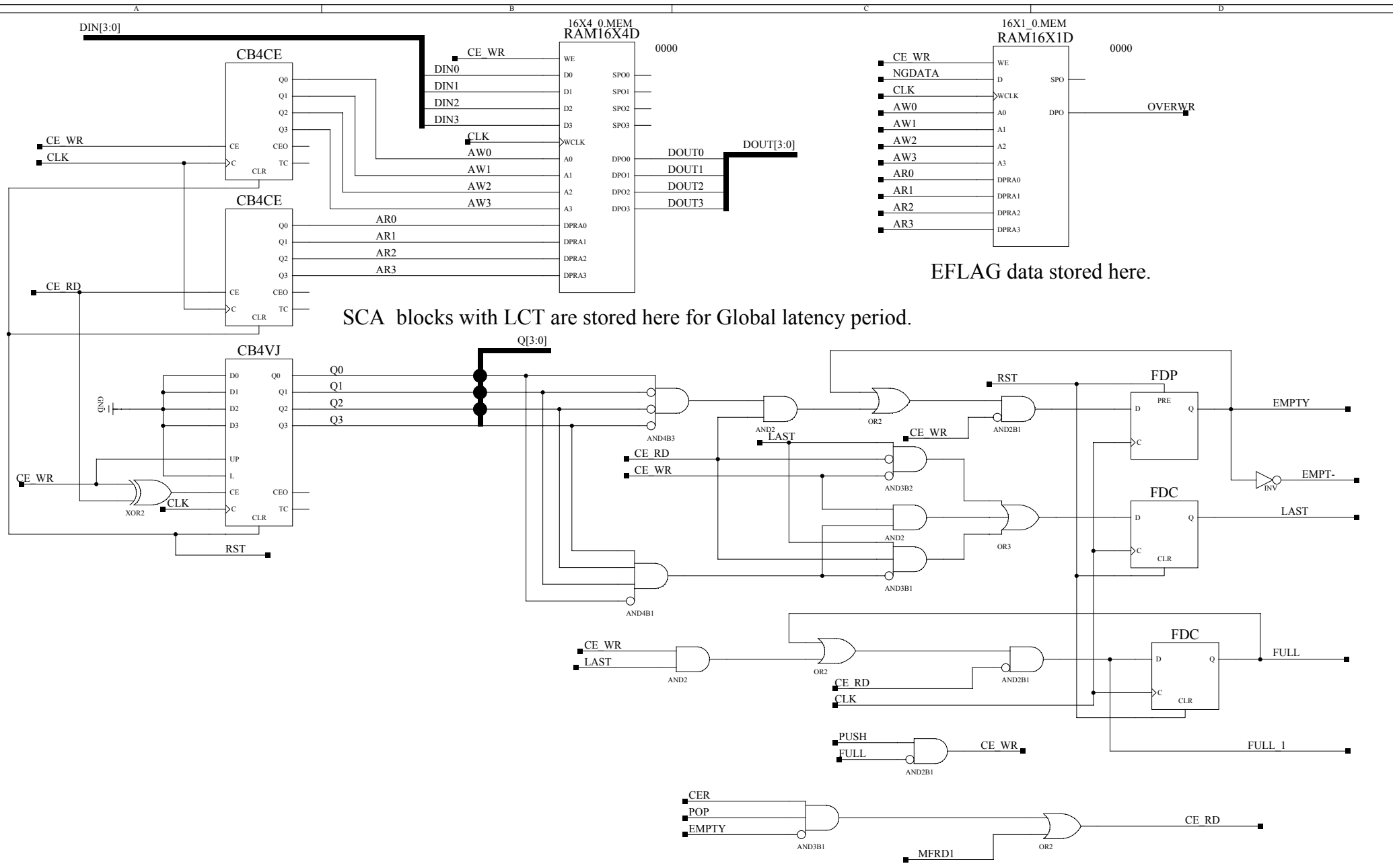
NOTE: LOW ON SEL WILL PASS THROUGH D0





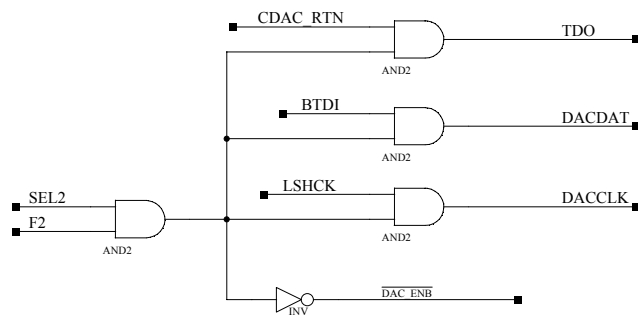
Check Status LOGIC (F0)



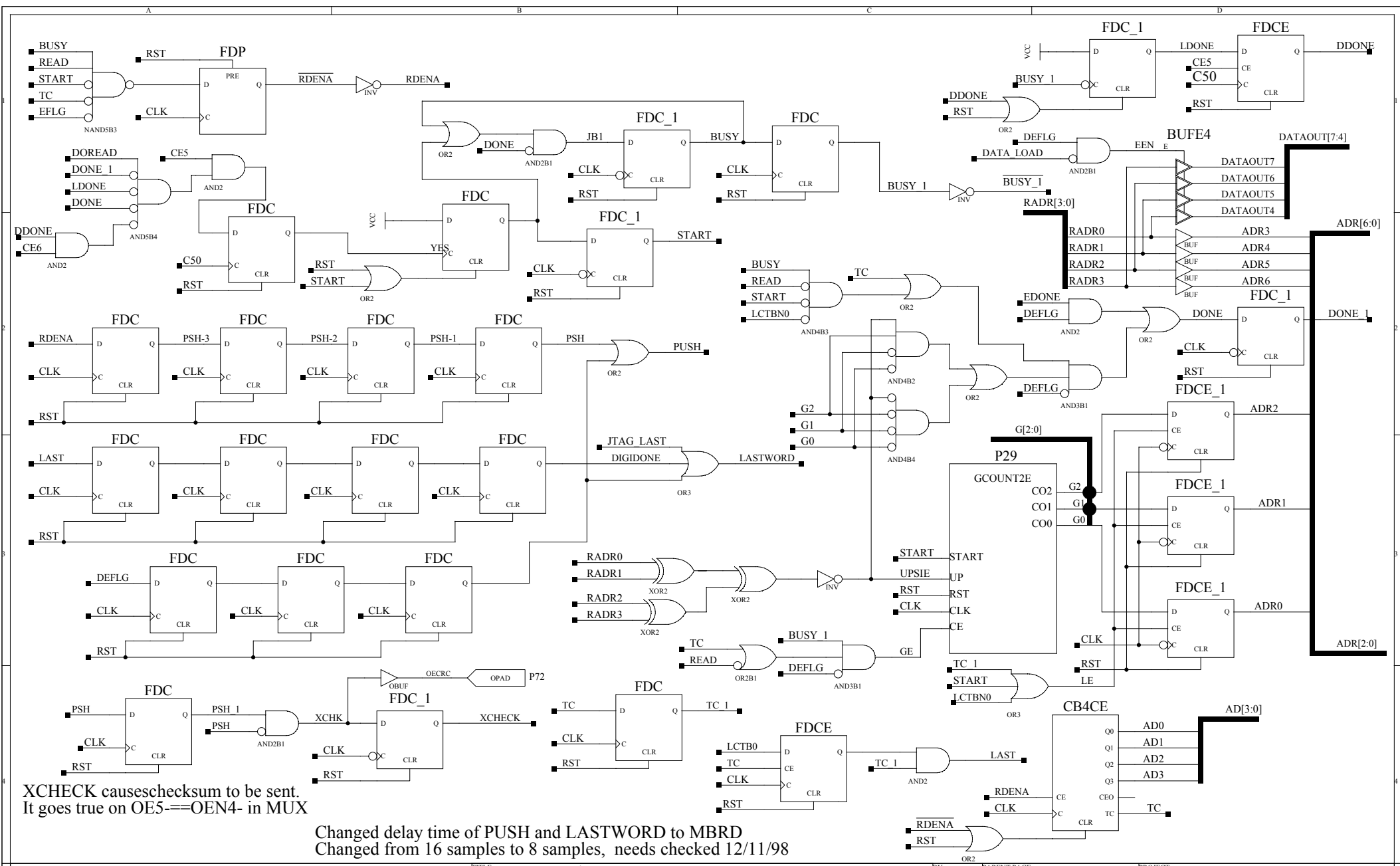


SCA blocks with LCT are stored here for Global latency period.

EFLAG data stored here.



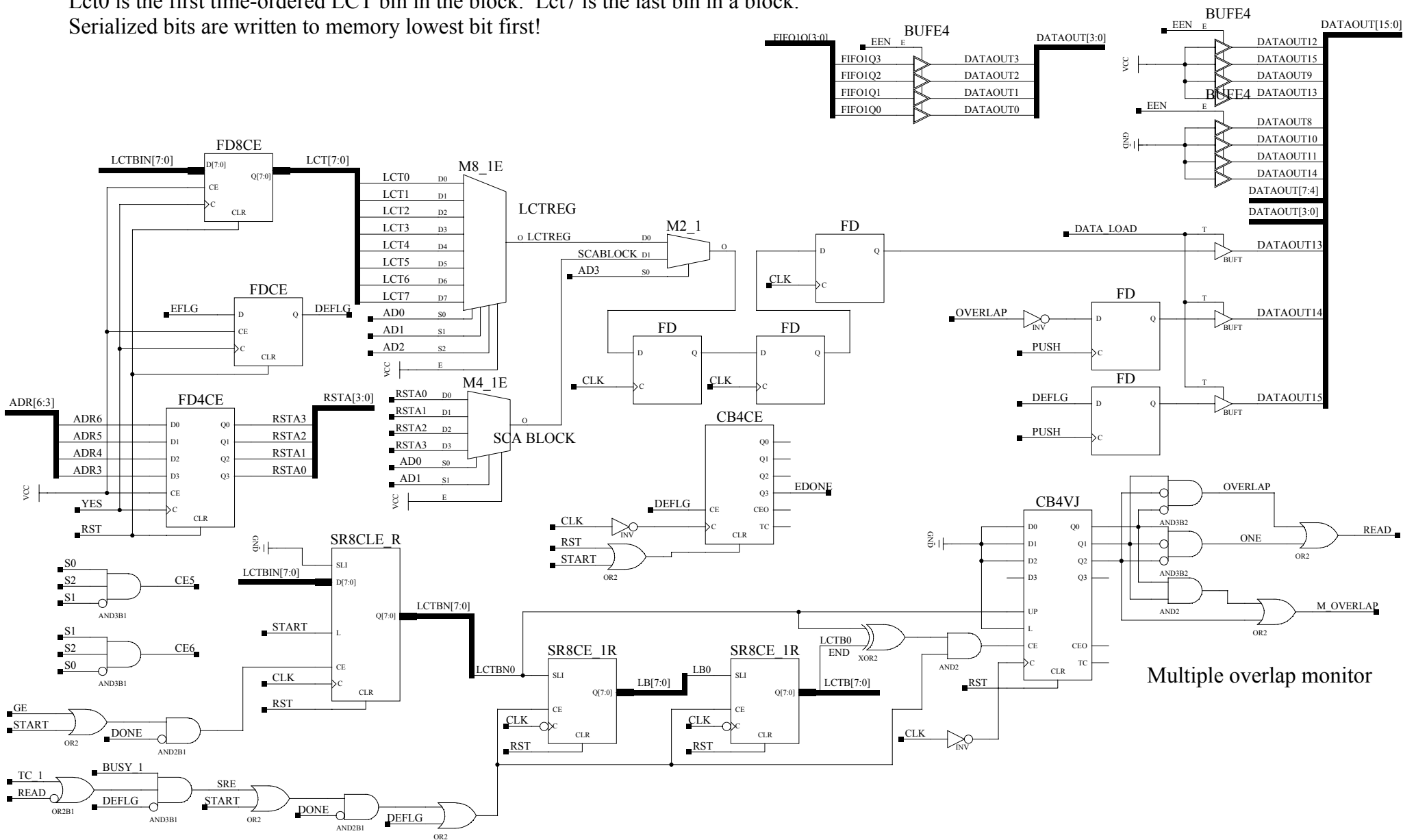
"DAC"



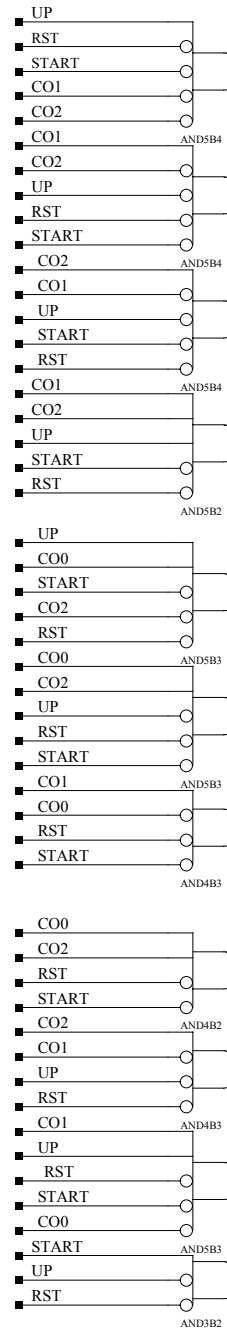
XCHECK causes checksum to be sent.
It goes true on OE5==OEN4- in MUX

Changed delay time of PUSH and LASTWORD to MBRD
Changed from 16 samples to 8 samples, needs checked 12/11/98

Lct0 is the first time-ordered LCT bin in the block. Lct7 is the last bin in a block.
Serialized bits are written to memory lowest bit first!

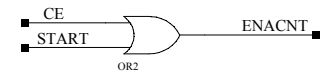


Multiple overlap monitor

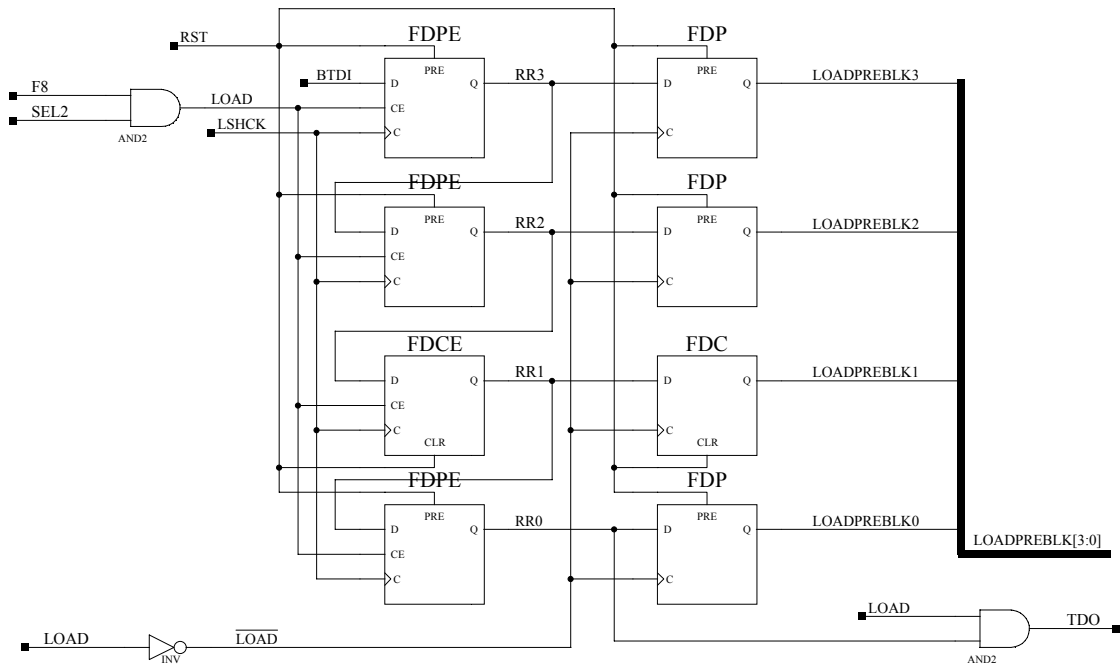


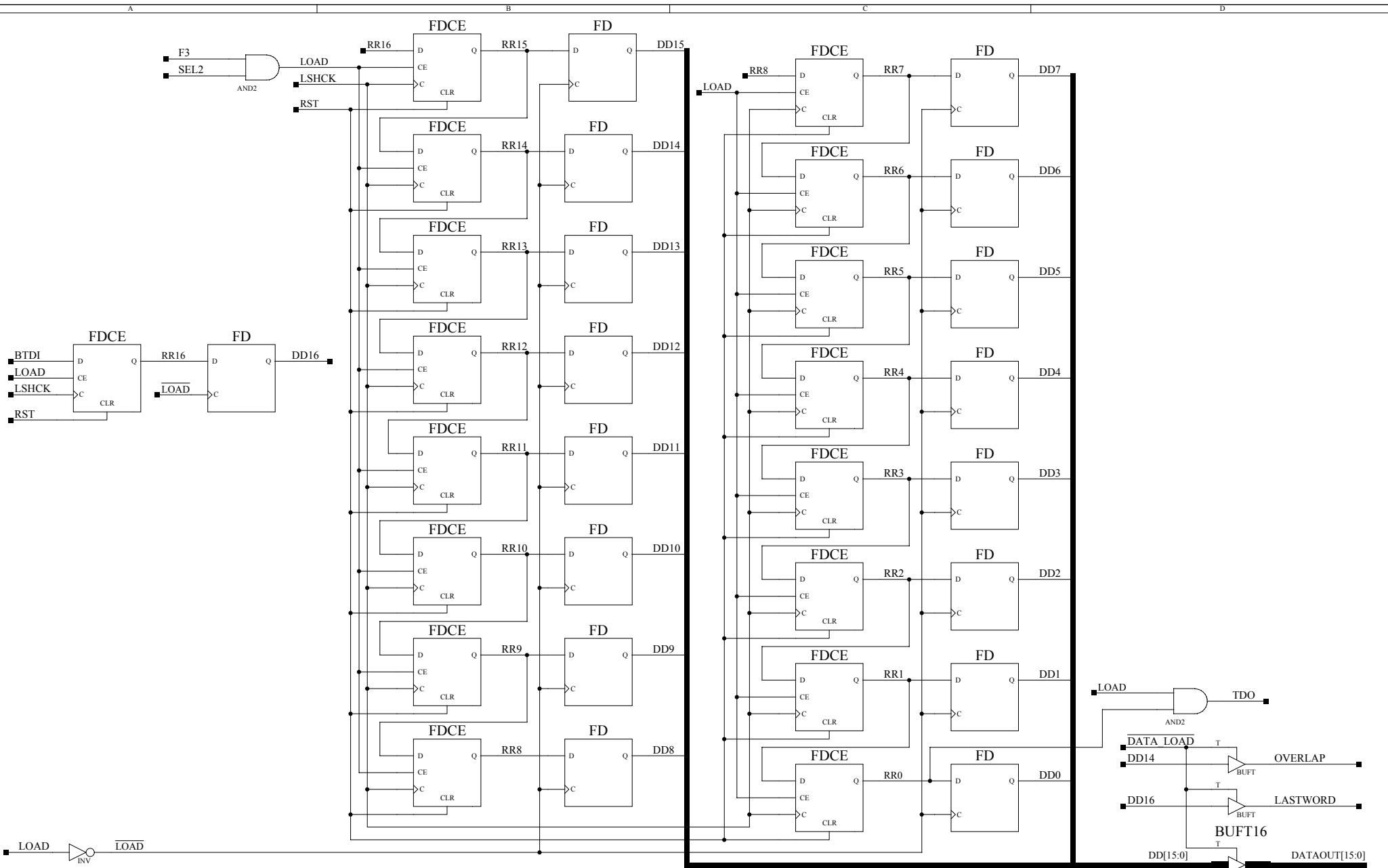
Will count 0 1 3 2 6 7 5 4
 Will count 4 5 7 6 2 3 1 0 when up is low

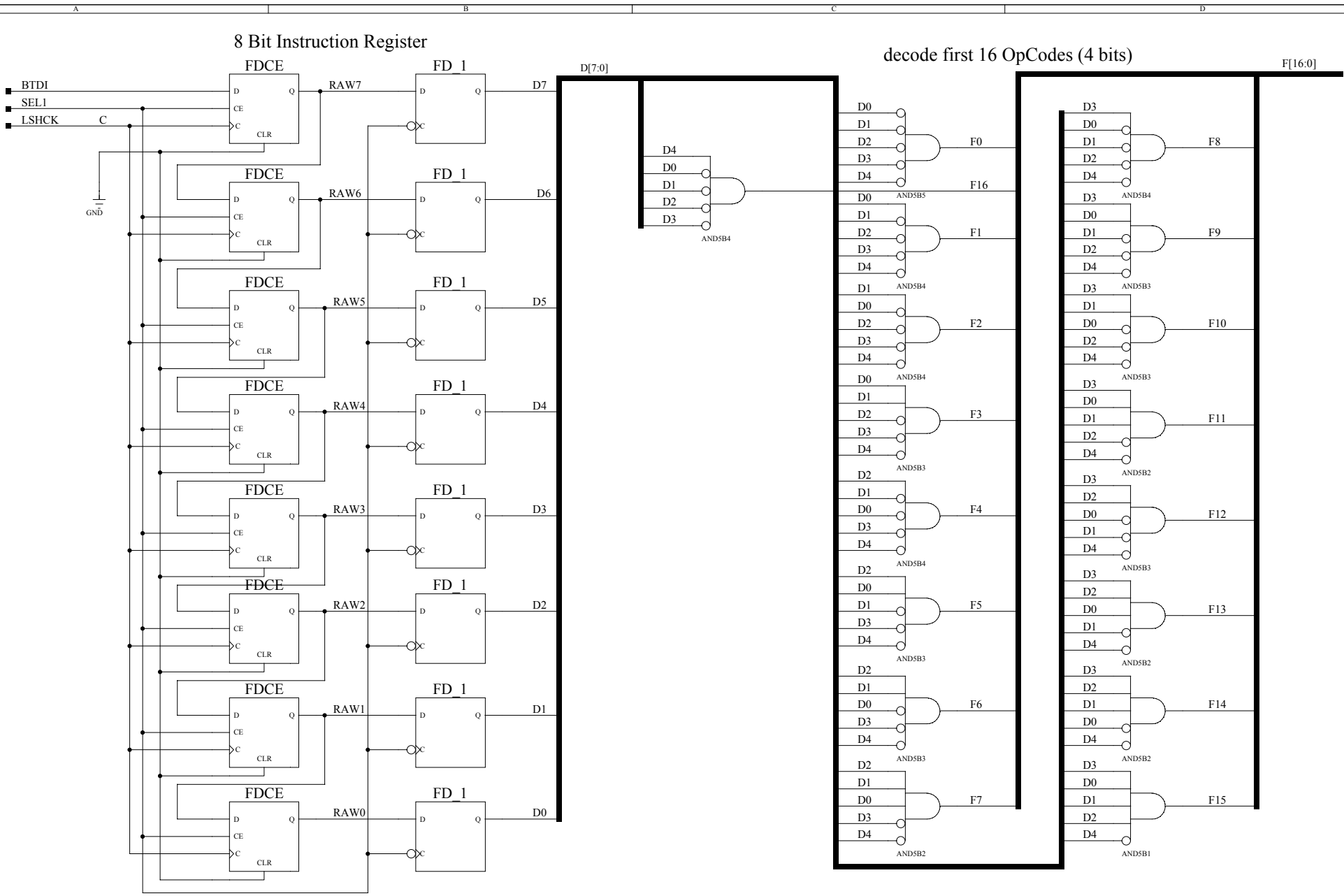
CO[2:0]

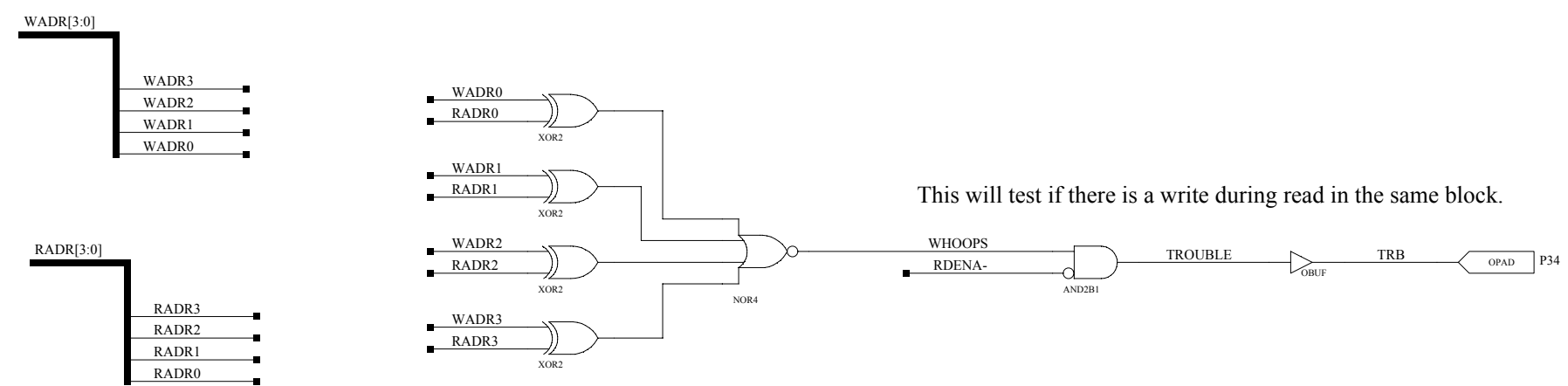


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE., COLUMBUS OH 43210			
TITLE GREY COUNTER SCA Controller CMS CSC Electronics			
PARENT PAGE	28	PROJECT	D741C
BY VKS	DATE 9-9-1998 15:59	FILE	GCOUNT2E. 1
			PAGE 29

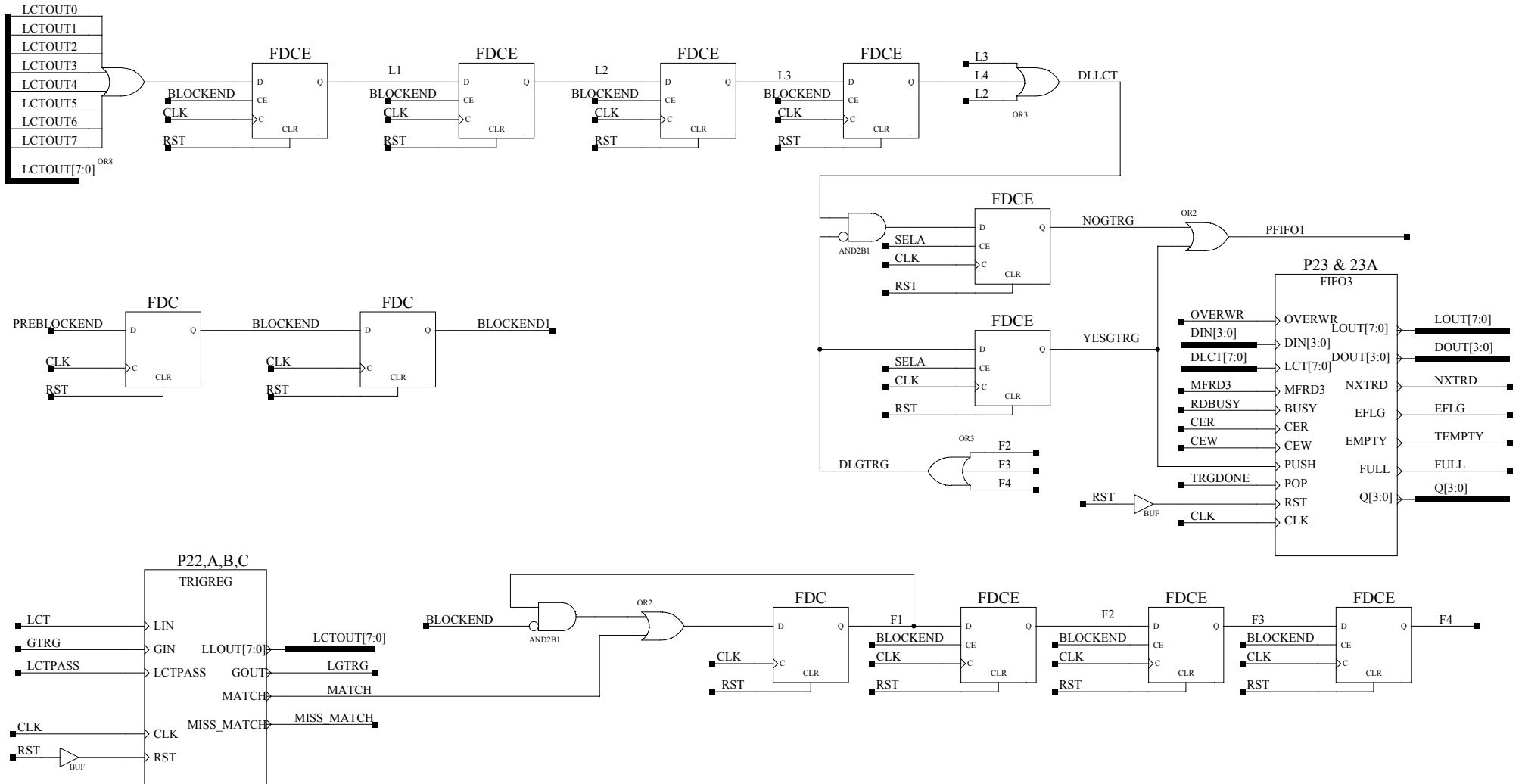


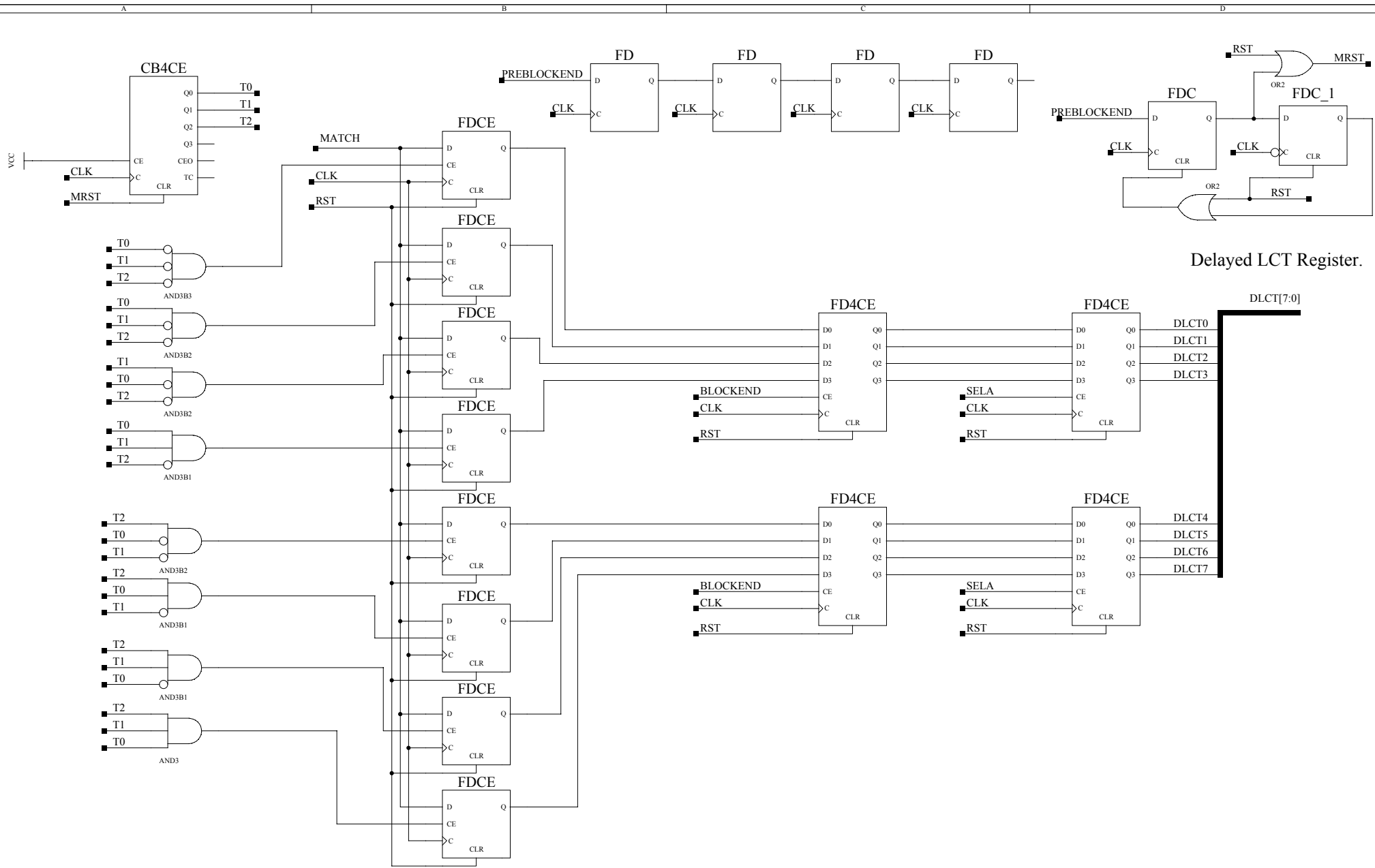






In TRIGREG: synchronize LCT and GTRG signals. Also pipeline LCT for 390ns GTRG latency and generate MATCH signal (dataavail). Then determine MATCHed LCT times relative to BLOCKEND and store in LCT Register DLCT[7:0]. Finally, write DLCT and SCA-BLOCKADR in FIFO3 and pop FIFO01. Free the block in NBADR if NOGTRG.





Delayed LCT Register.


LCT is synchronized in DAQMB

LCT REG.

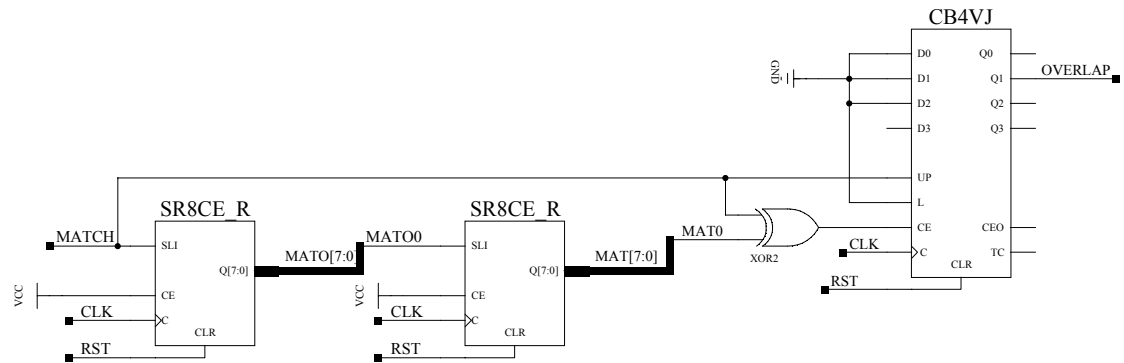
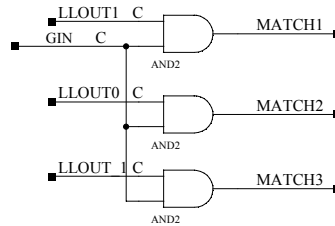
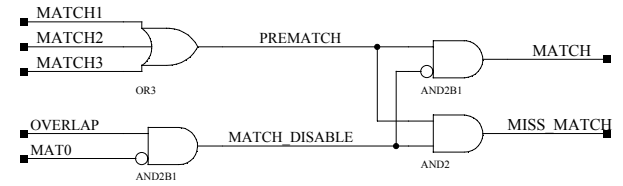
LLOUT[7:0]

LLOUT0
LLOUT1
LLOUT2
LLOUT3
LLOUT4
LLOUT5
LLOUT6
LLOUT7

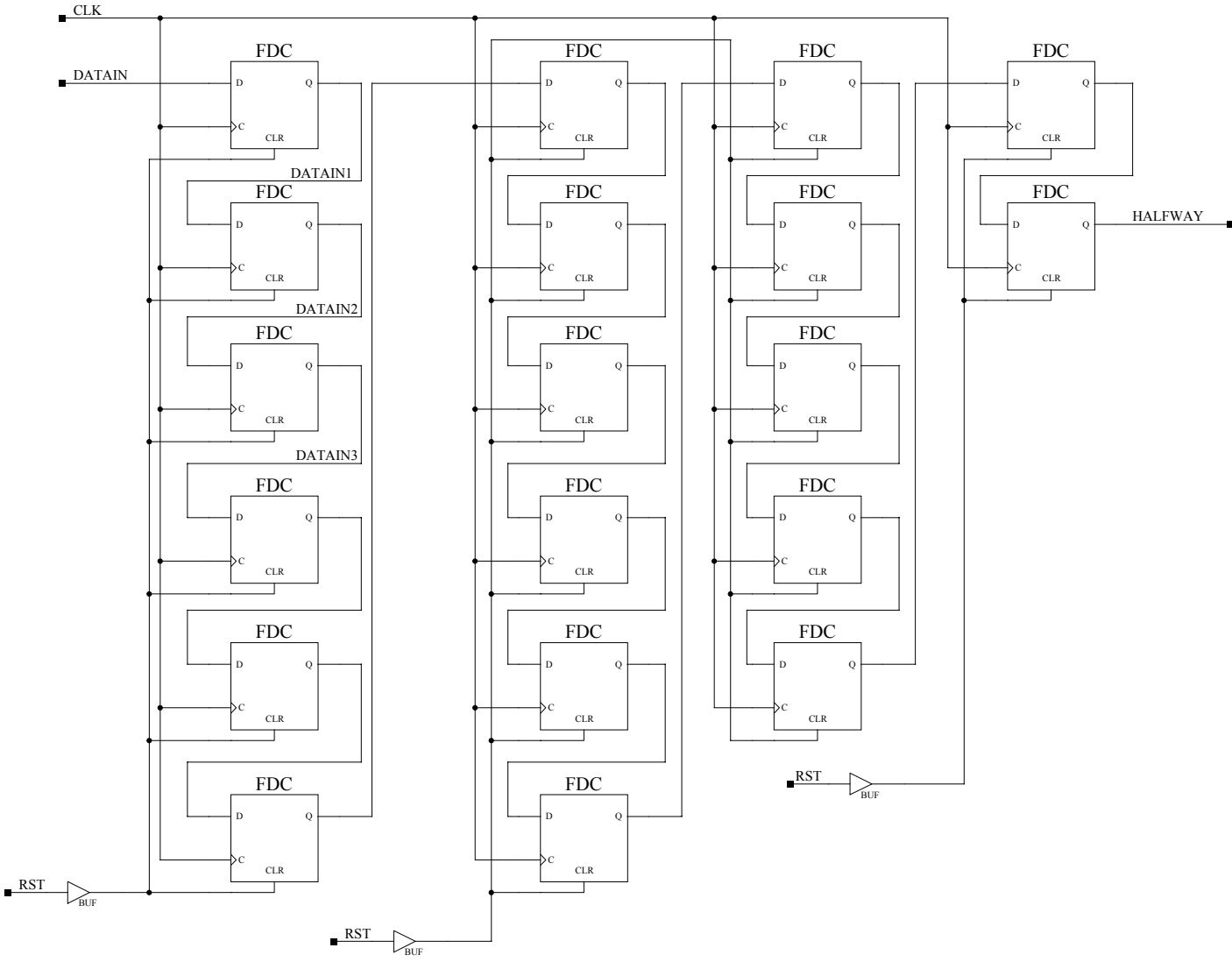
HALFWAY
HALF1
HALF2
HALF3

LIN  DATAIN
DATAIN1
DATAIN2
DATAIN3

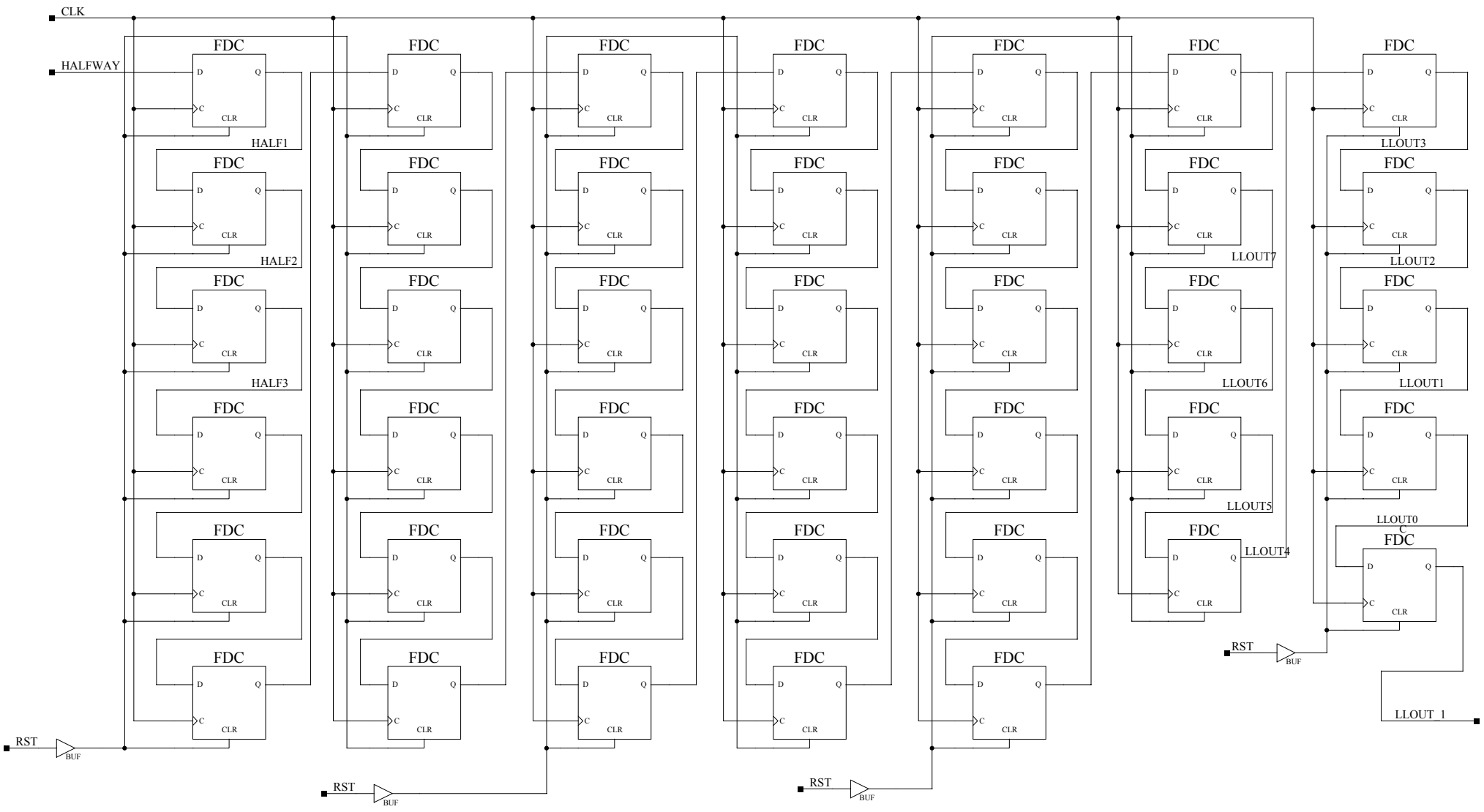
Global Trigger Synchronized at DAQMB, Matching with pipelined LCT.

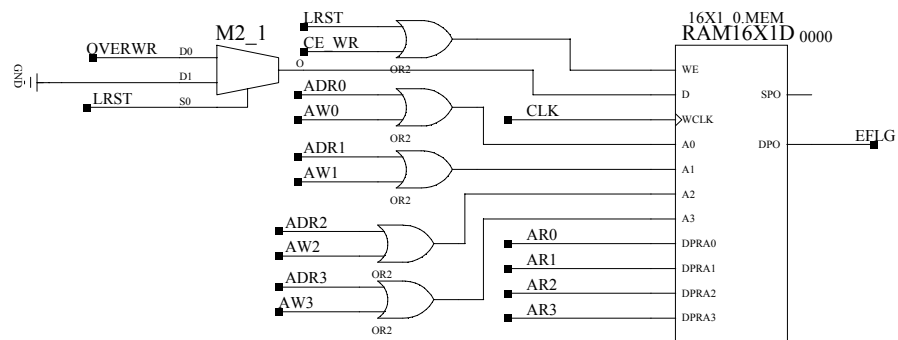


First part of LCT Pipeline, 1050ns.

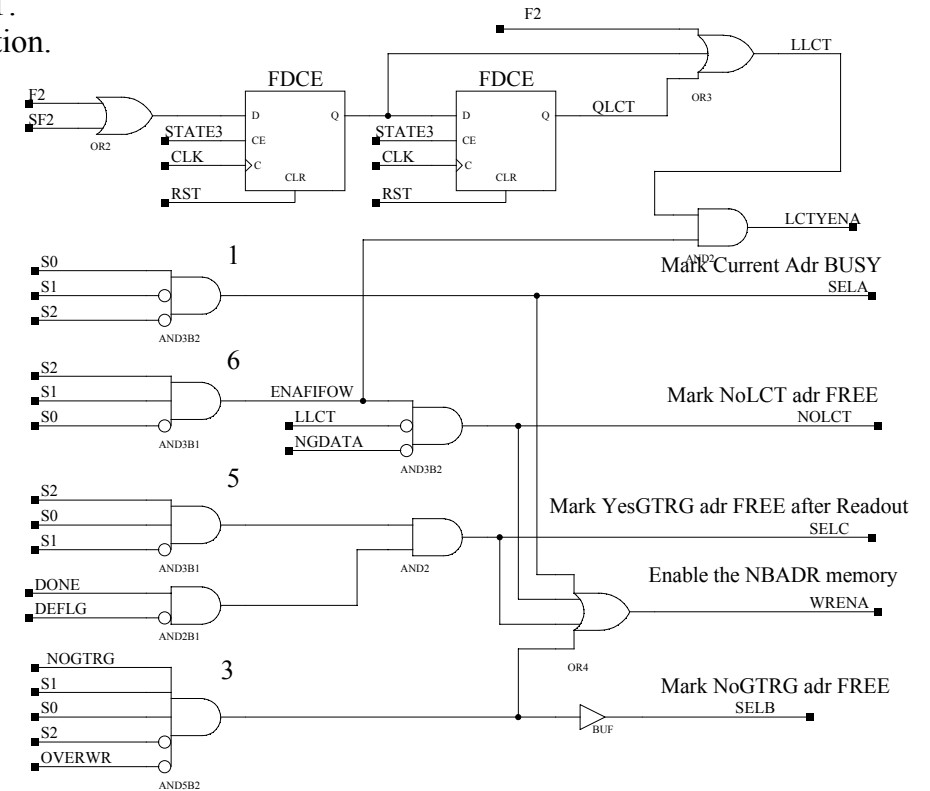
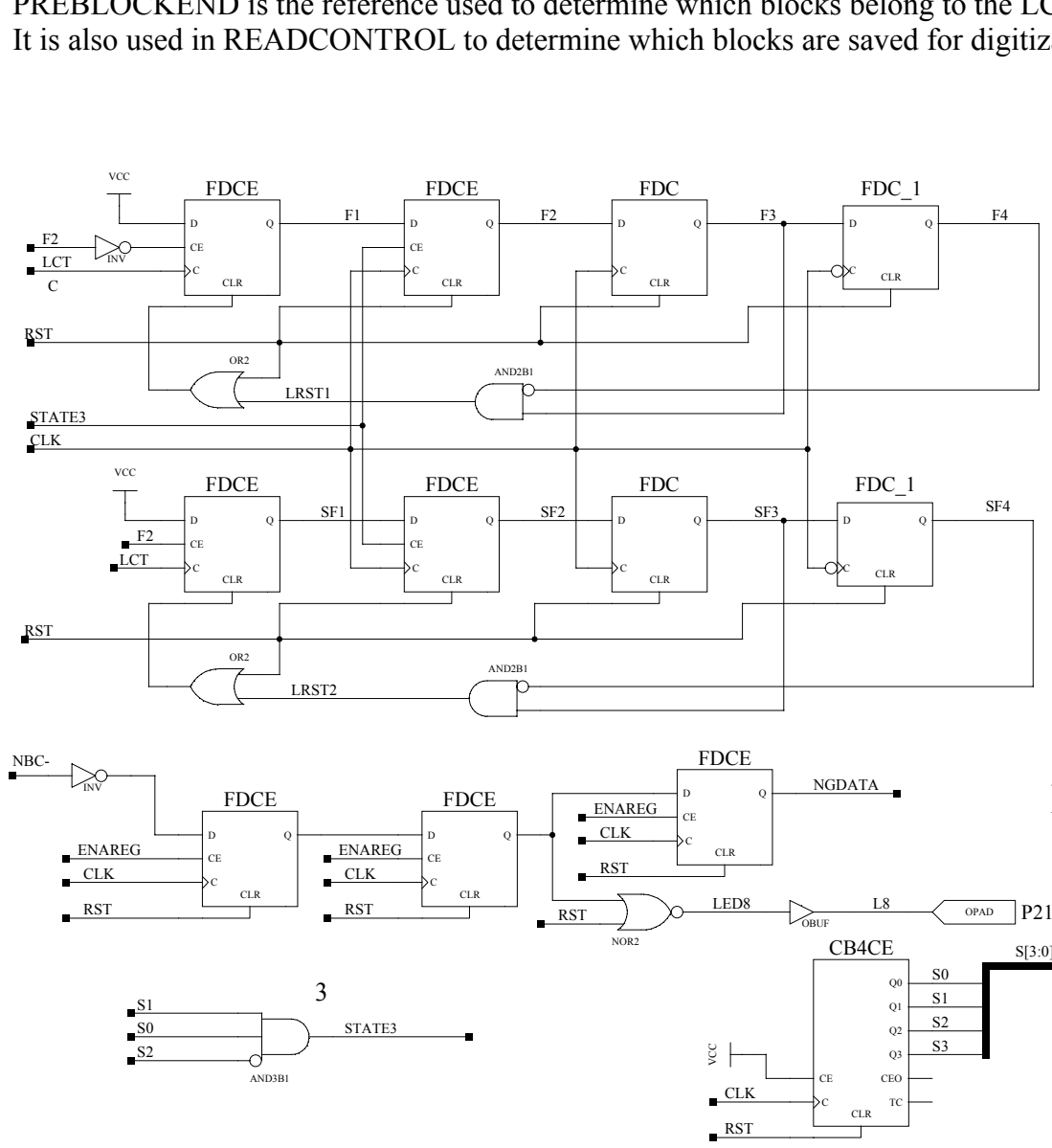


Second part of LCT Pipeline, 1950ns.





Bus S[2:0] is the primary state machine of the device.
 PREBLOCKEND is the reference used to determine which blocks belong to the LCT.
 It is also used in READCONTROL to determine which blocks are saved for digitization.



Do not free addresses on EFLG!!

