New Results on Opto-Electronics

K.K. Gan
The Ohio State University
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The Ohio State University

A. Ciliox, M. Holder, S. Nderitu, M. Ziolkowski
Siegen University
Outline

- VDC-I5
- VDC/DORIC-I5e
- QA
- BeO Opto-board
- Summary
VDC-I5: Bright and Dim Currents vs. $I_{set}$

- higher bright current as redesigned
- dim current close to target 1 mA
- rise/fall times, duty cycle, current consumption all within specs

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Optical Power of Normal & High Power Oxide VCSELs

both kinds of VCSELs produce similar optical power
- p+/oxide VCSELs have similar optical power in operating range (10-20 mA)
- oxide VCSELs have larger effective serial resistance
  - smaller VCSEL current when driven by VDC
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VDC-I5: VCSEL Current vs. $I_{set}$

*VDC-I5 output current for p+, normal and high power VCSELs*

- High power oxide VCSEL has lower maximum current: 15 mA
some VCSEL arrays contain a channel with much larger effective serial resistance
\[ 4 \text{ mA less VCSEL current when driven by VDC } \]
VDC/DORIC-I5e: Engineering Run

- convert from 3-metal to 5-metal layout
- minor improvements in DORIC:
  - default power distribution layer is now the 3rd layer and hence thinner
    - thicken power/ground lines
  - add MIMCAP bypass capacitors to power lines
    - reduced noise in internal signals
  - add ground plane over digital circuit as noise shield
    - signal is slightly slower due to stray capacitance to shield
  - convert reset from active high to low
    - for ease of implementation by DCS
    - slightly better performance at \( \pm 3\)\(^\circ\) corner transistor parameters
- submitted with MCC in April 2003
- status: wafer @ Bonn
VDC/DORIC/Opto-board Quality Assurance

- circuit boards: designed/built/tested
- LabView programs: written/tested
- DORIC passes QA
- opto-board passes QA
  - rise time of optical signal: < 1 ns
- VDC fails following QA:
  - VCSEL current at $I_{\text{set}} = 1.5 \text{ mA}$: 15 mA vs. 20 mA in QA
  - redefine spec in QA for high power oxide VCSEL?
  - rise time of optical signal: $\sim 1.5 \text{ ns}$ vs. < 1 ns in QA
Rise/Fall Time of Optical Signal

- Slower rise time due to a kink in signal and long leads in test board
  - Define rise/fall time as time duration for the signal to rise/fall from 20 to 80% instead of 10 to 90% of the amplitude
  - Both 10-90 and 20-80% are widely used by industry
- VDC passes opto-board QA
  - Redefine spec in VDC QA
QA Plans

- **VDC/DORIC QA:**
  - current use packaged chip to exercise QA system
  - just received probe cards
  - perform QA with probe station

- **opto-board QA:**
  - perform QA in temperature controlled chamber
Status of BeO Opto-board

- First batch:
  - 30 boards delivered in April
  - several open vias on each board due to insufficient gold filling
    ➔ repair with wire-wrap wires
PIN Current Threshold for No Bit Errors

- low PIN current thresholds for no bit errors independent of activity in adjacent channels
- no design error
Status of BeO Opto-board

- Second batch:
  - 31 boards delivered in June
  - vias overfilled and excess metal ground away
    → no open vias
  - 17 boards have shorts between power and ground lines
  - attempt to populate a second BeO board:
    - opto-pack housing fits well
    - opto-pack must be delivered with pins bent by 90° and flush with opto-board
    - one DORIC mounted backward
    - no visible damage to adjacent chip after replacement
  - board failed to work
  - replaced both DORICs
BeO Opto-board from 2nd Batch

34.7 °C

36.4 °C

Ambient: 22.5 °C

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- Both opto-boards have low PIN current thresholds for no bit errors independent of activity in adjacent channels.
- Awaiting quote from a second vendor.

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Summary

- all improvements in VDC/DORIC-I5 are successful
- VDC/DORIC/opto-board QA procedures exercised
- BeO opto-boards fabricated from 1st and 2nd batches operate with low PIN current thresholds with no bit errors