New Results on Opto-Electronics

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Introduction

● VCSEL Driver Chip (VDC):
  ✤ convert LVDS signal into single-ended signal appropriate to drive VCSEL

● Digital Opto-Receiver Integrated Circuit (DORIC):
  ✤ decode clock and command signals from PIN diode
Opto-electronics Team

● The Ohio State University:

● Siegen University:
  ✫ Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski
Results on VDC/DORIC-D3

- **VDC-D3:** performance is satisfactory
- **DORIC-D3:**
  - 2 dice in packages + one die on opto-board II
  - 24 µA minimum PIN current for no bit errors
  - uniformly low PIN current thresholds
  - DC feedback is working
Opto-Board Prototype III

- design for VDC-D3/DORIC-D3 and 4-channel VDC-I2/1-channel DORIC-I2
- compatible with VDC/DORIC-I3
- contain 7 opto-links for use in barrel and disk
- use SCT style opto-packs
- use 80-pin connector
- fabricated using FR4
- opto-board is working as designed
  - PIN current threshold for no bit errors is comparable with packaged dice
Opto-Board Prototype IV

- design for 4-channel VDC/DORIC-I4
- contain 7 opto-links for use in barrel and disk
- use 8-channel opto-packs
- use 80-pin connector
- last submission before using BeO
- to be designed for BeO but tested in FR4
- expect submission in summer 2002
Irradiated Opto-Board with VDC/DORIC-I1

Opto-packs

Thermocouple
Cold irradiated VCSELs produce much more light
turning over at high $I_{set}$ is due to 10 $\Omega$ in series used in measurement

dependence of bright current vs $I_{set}$ is as expected
Ripple in VDC-I2 Current Consumption

- VDC-I2 has more balance current consumption with VCSEL on and off
Current Consumption of VDC-I2

- current consumption of VDC-I2 is consistent with expectation
Clock Duty Cycle vs $I_{set}$

- clock duty cycle close to 50% at 10 mA bright current
Fall/Rise Time vs $I_{set}$

- fall/rise times somewhat above spec. (1 ns)

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ATLAS Pixel Week
DORIC-I2

- minor bugs due to clamping/protection diodes:
  - VPIN is limited to 3.2 V
    - current in diode contribute to measured minimum PIN current for no bit errors
  - CMOS driver is powered at 1.7 V via diode to digital VDD
    - CMOS driver can’t be turned off
    - contribute noise to pre-amp
      - minimum PIN current for no bit errors:
        - 27 µA vs 24 µA with diode blown
        - uniformly low PIN current thresholds
        - DC feedback is working!
DORIC-I2

- larger time constant in pre-amp successful prevents feedback loop from oscillating even with no input!
- larger time constant in delay control circuit successful prevents delay control circuit from oscillating!
- clock duty cycle: 46/50% on two DORIC tested
Improvements in VDC-I4

- convert VDC-I3 to be compatible with common cathode VCSEL array
Bright and Dim Current Consumption vs $I_{set}$

- VDC-I3/I4 has nearly equal current consumption
VDC Current Consumption

- simulations of VDC-I1/I2 reproduce observation
- VDC-I3/I4 consumes significantly less current
Improvements in DORIC-I4

● improved delay control circuit:
  ◆ centers duty cycle of recovered clock at 50%
  ◆ limits range of delays to prevent locking of recovered clock at half or twice frequency
  ◆ add reset for slow and controlled recovery

● optimized timing:
  ◆ two small delays added

● optimized internal digital signals:
  ◆ change edge detector output buffer resistor from 20K to 10K
    ➡ smaller voltage swing
    ➡ symmetric threshold crossing for +/- signals
  ◆ stronger exclusive OR output buffer for square recovered clock
Improvements in DORIC-I4 (cont.)

- improved pre-amp:
  - half the rise time
  - working on reducing noise
- optimize pre-amp design to be compatible with common anode PIN array
- submit a MPW run on April 15
Summary

● important to keep opto-board cold for maximum light output
● performance of VDC/DORIC-I2 is satisfactory