New Results on Opto-Electronics

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Outline

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- Results on VDC-I1/DORIC-I1 Irradiation
- Improvements in VDC-I2/DORIC-I2
- Improvements in VDC-I3/DORIC-I3
- Summary
Introduction

- **VCSEL Driver Chip (VDC):**
  - convert LVDS signal into single-ended signal appropriate to drive VCSEL
- **Digital Opto-Receiver Integrated Circuit (DORIC):**
  - decode clock and command signals from PIN diode
Opto-electronics Team

- The Ohio State University:

- Siegen University:
  - Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski
two designs were submitted

- **VDC-D3:**
  - new circuit to decouple bright/dim current adjustments
  - SCT bias circuit

- **VDC-D3P:**
  - same as VDC-D3 but with poly resistor in bias circuit
VCSEL Currents vs $I_{\text{set}}$

dependence of bright/dim currents on $I_{\text{set}}$ is as expected
VDC-D3 consumes ~ 17 mA for 10 mA VCSEL current @ 3.2 V
similar to VDC-D2
DORIC-D3

changes:

- new pre-amp with DC feedback to cancel offset at differential inputs
- SCT LVDS driver

preliminary results:

- clock has 50% duty cycle at CMOS driver and before LVDS driver
- clock has 40% duty cycle at LVDS driver
- 100 mV clock-like ripple on 1.6 V delay control line
  - ~ 50 µA minimum PIN current for no bit errors for 2 dice in packages + one die on opto-board III
  - DC feedback is working
September Irradiation of Opto-Electronics

- use 24 GeV proton test beam at T7
- cold box: purely electrical testing of VDC-I1 and DORIC-I1
- shuttle system: testing of 5 optical links on opto-board
Rise Time of Irradiated VDCs Before and After Annealing

annealing produces no significant change

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Fall Time of Irradiated VDCs Before and After Annealing

Annealing produces no significant change

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Bright Current of Irradiated VDCs Before and After Annealing

- irradiation slightly reduces light output
- annealing slightly increases light output
### Packaged DORIC-I1 Irradiation

<table>
<thead>
<tr>
<th>DORIC</th>
<th>#1</th>
<th>#2</th>
<th>#3</th>
<th>#4</th>
<th>#5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-irrad BER Threshold (µA)</td>
<td>150</td>
<td>?</td>
<td>130</td>
<td>124</td>
<td>102</td>
</tr>
<tr>
<td>Post-irrad BER Threshold (µA)</td>
<td>150</td>
<td>240</td>
<td>129</td>
<td>174</td>
<td>60</td>
</tr>
<tr>
<td>Post-annealing BER Threshold (µA)</td>
<td>104</td>
<td>172</td>
<td>121</td>
<td>149</td>
<td>445</td>
</tr>
<tr>
<td>Pre-irrad Duty Cycle (%)</td>
<td>48.8</td>
<td>?</td>
<td>45.6</td>
<td>47.4</td>
<td>49.2</td>
</tr>
<tr>
<td>Post-irrad Duty Cycle (%)</td>
<td>47.8</td>
<td>43.8</td>
<td>46.0</td>
<td>46.8</td>
<td>47.6</td>
</tr>
<tr>
<td>Post-annealing Duty Cycle (%)</td>
<td>46.8</td>
<td>44.0</td>
<td>44.0</td>
<td>45.4</td>
<td>47.4</td>
</tr>
</tbody>
</table>

- **DORIC #4**: wire bonds crushed ➔ die may be damaged
- **after irradiation and annealing:**
  - ☆ no degradation in bit error threshold except one die
  - ☆ no degradation in clock duty cycle

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VCSELs have slightly slower rise time after annealing
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Optical Power of Irradiated Opto-board Before and After Annealing

- VCSEL power reaches plateau after a week of annealing
- Fibers with various dosages have same insertion lost: \( \sim 15\% \)
- Failure for VCSEL to anneal is due to radiation damage
Summary of VDC-I1/DORIC-I1 Irradiation

- VDC-I1/DORIC-I1 continue to perform well after 40-50 Mrad
- Changes after irradiation/annealing are small except one die which has much higher bit error threshold
Improvements in VDC-I2/VDC-I3

- **VDC-I2:**
  - ✿ keep OSU design that decouples adjustment of bright and dim currents
  - ✿ new circuit that equalizes bright and dim current consumption
  - ✿ new LBL pads
  - ✿ submitted two designs: single and four-channel VDC

- **VDC-I3:**
  - ✿ further equalize bright and dim current consumption
  - ✿ consume less current
  - ✿ submitted single channel VDC in MPW
Bright and Dim Current Consumption vs $I_{\text{set}}$

- simulation of VDC-I1O reproduces observation
- VDC-I2 has much more equal bright and dim current consumption
- VDC-I3 further equalizes the current consumption
Bright Current vs $I_{set}$ with 10 Ω in Series

- simulation of VDC-I1O reproduces observation
- VDC-I3 has smaller bright current than VDC-I2
- VDC-I3 has a maximum of 22 mA without 10 Ω in series
VDC Current Consumption

- simulation of VDC-I1O reproduces observation
- VDC-I3 consumes significantly less current
VDC-I3
Simulation of DORIC-I1/I2 from Extracted Layout with Stray Capacitance plus Wire Bonds

- **DORIC-I1**: needs large PIN current for no bit errors
  - predict spikes as observed in lab
- **DORIC-I2**: can run at low PIN current (12 µA) with no bit errors

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Improvements in DORIC-I2/DORIC-I3

- DORIC-I2: differential pre-amp
  - numerous improvements

- DORIC-I3: single-ended pre-amp
  - add dummy channel to cancel noise except white noise which adds in quadrature
  - reduce maximum delay (2.0 ⇒ 1.5 x) in delay control loop to further reduce possibility of locking at half frequency
Simulation of DORIC-I3 from Extracted Layout with Stray Capacitance plus Wire Bonds

- predict to decode signal correctly up to
  - \( \pm 3\sigma \) process corners
  - \( \pm 50 \) mV pre-amp offset
Summary

- VDC-D3/DORIC-D3 basically work!
- radiation hardness of VDC-I1/DORIC-I1 appears adequate for pixel system!
- many improvements implemented in VDC-I2/DORIC-I2
- expect VDC-I3 to consume significantly less current
- single-ended pre-amp implemented in DORIC-I3