

New Results on VDC-D2 and DORIC-D2

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Outline

- Introduction
- Results on VDC-D2
- Results on DORIC-D2
- Plans

Introduction

- VCSEL Driver Chip (VDC):
 - ☆ convert LVDS signal into single-ended signal appropriate to drive VCSEL
- Digital Opto-Receiver Integrated Circuit (DORIC):
 - ☆ decode clock and command signals from PIN diode

Opto-electronics Team

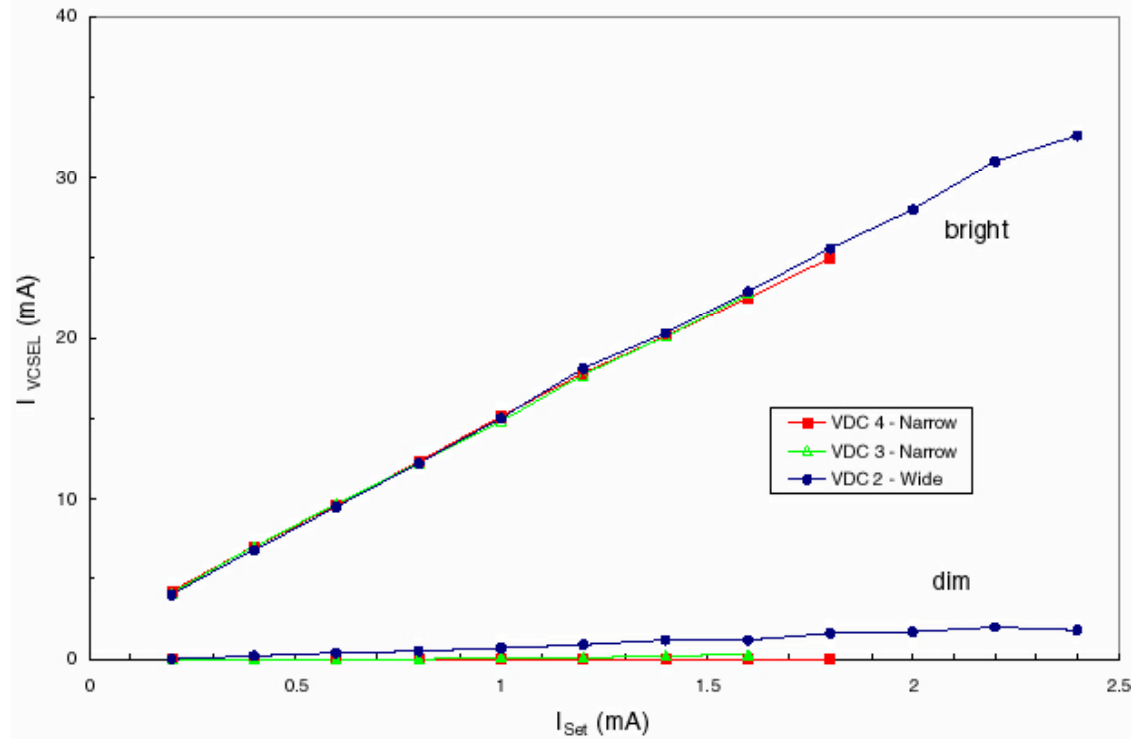
- Ohio State University:

- ☆ Kregg Arms, K.K. Gan, Mark Johnson, Harris Kagan, Richard Kass, Chuck Rush, Michael Zoeller

- Siegen University:

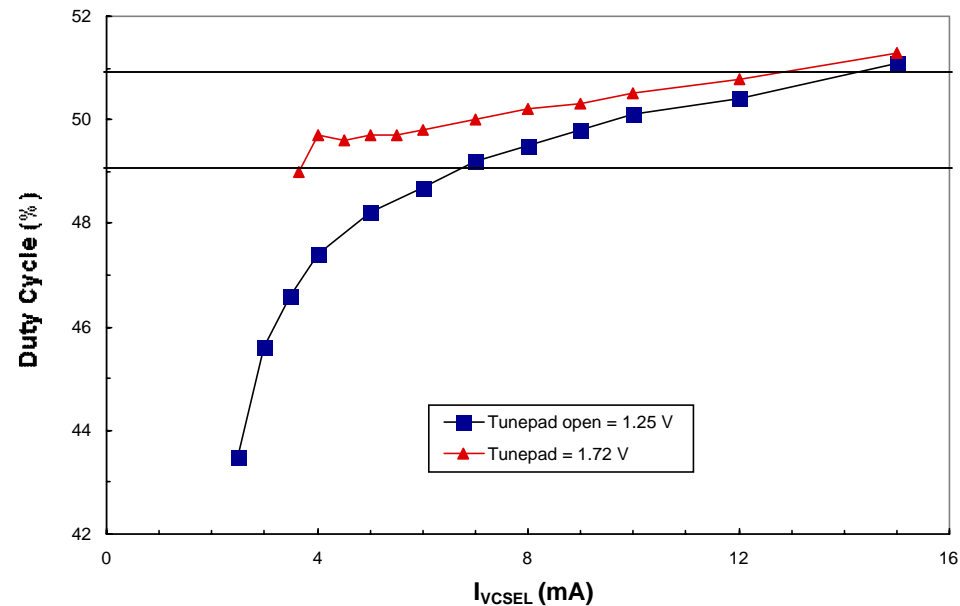
- ☆ Michael Kraemer, Joachim Hausmann, Martin Holder, Michal Ziolkowski

Bright/Dim Currents of VDC-D2



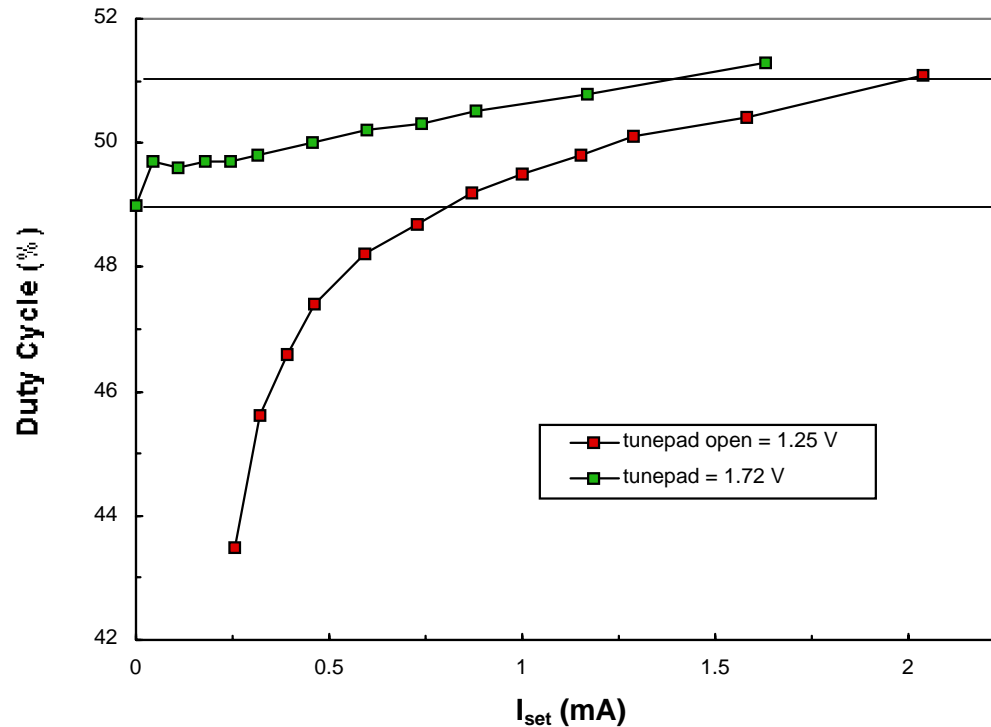
- two dice have dim currents < 1 mA

Duty Cycle vs VCSEL Current



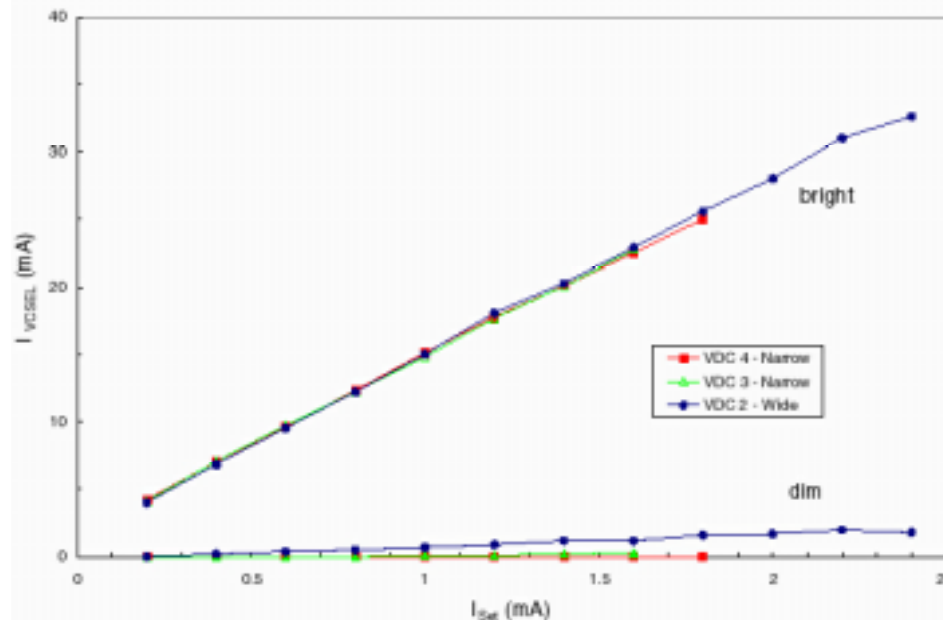
- deviate significantly from 50% duty cycle for low VCSEL current

Duty Cycle vs I_{set} Current



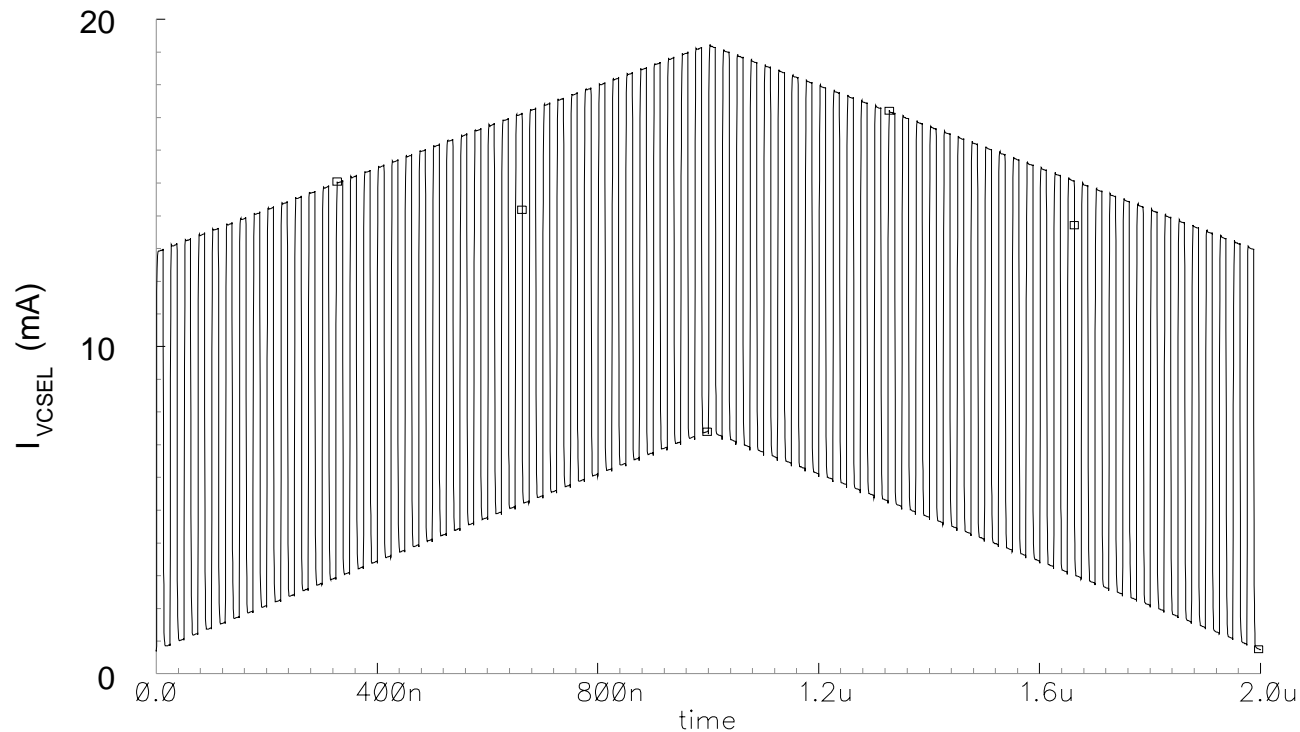
- deviate significantly from 50% duty cycle for low I_{set} current
- can reduce deviation significantly with tune-pad connected

Improvement in VDC-I



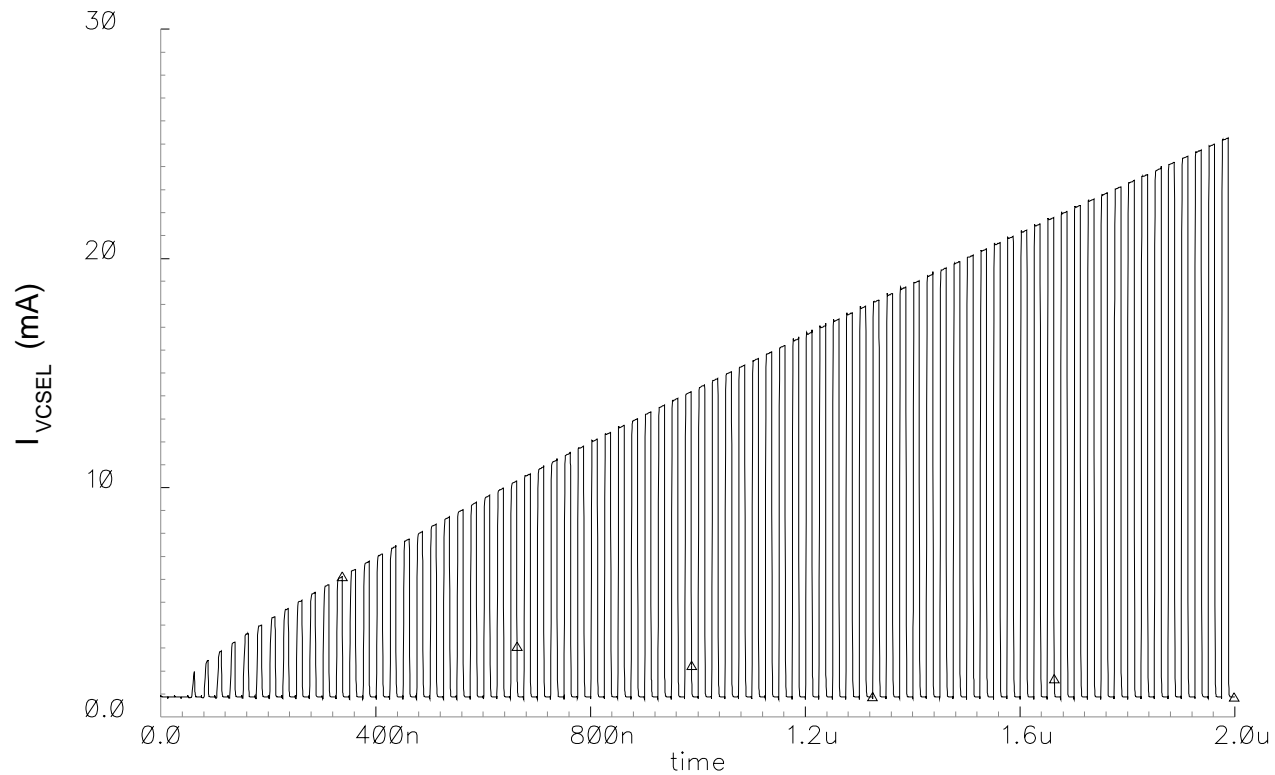
- ideal design: dim current depends on tune-pad but not I_{set}
- VDC-D2: dim current depends on I_{set} due to imperfect matching of currents in two transistors
 - ⇒ submit two versions of VDC-I:
 - DMILL version and a version with bright current controlled by I_{set} added to dim current controlled by tune-pad

VCSEL Current vs Tune-pad Current



- amplitude of VCSEL current remains constant as tune-pad current is increased from 0 to 1 mA

VCSEL Current vs I_{set}



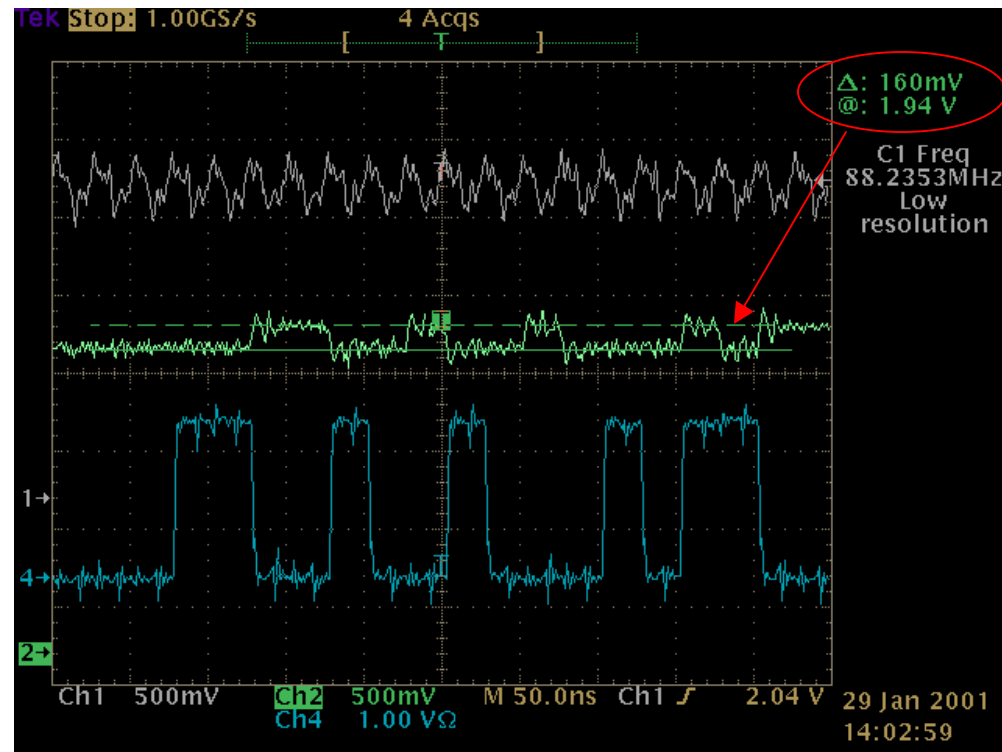
- dim current remains constant as I_{set} is increased from 0 to 2 mA

DORIC-D2 with LVDS Reset at VDD (Default)

Decoded clock

Decoded data

Input data

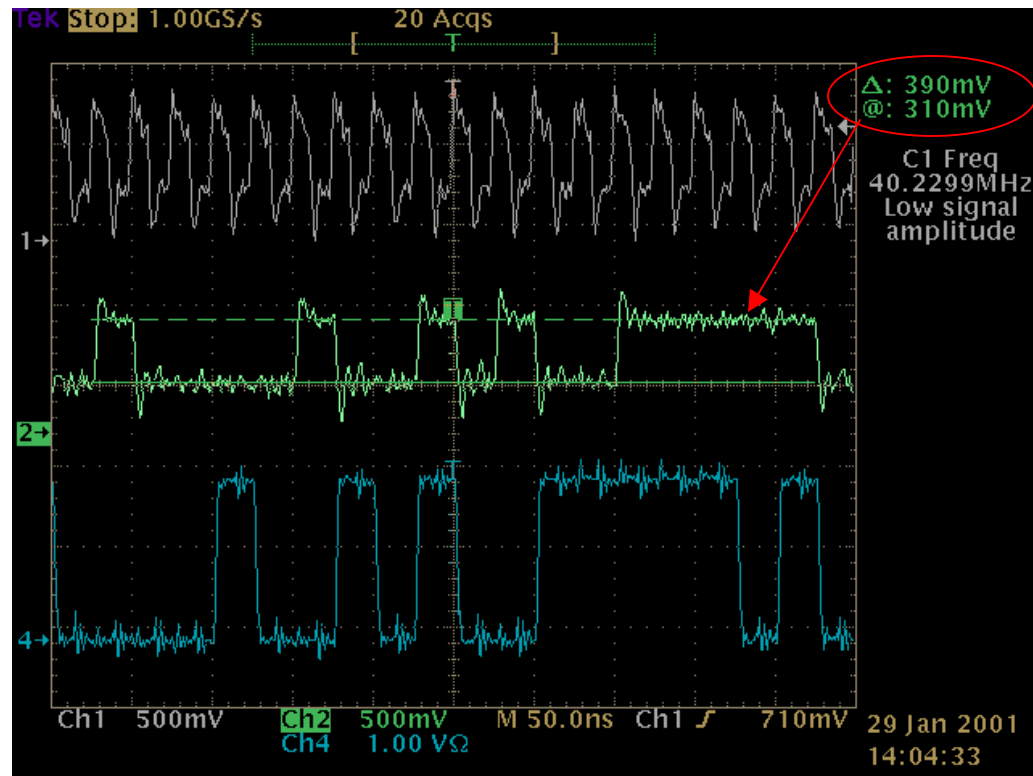


DORIC-D2 with LVDS Reset Grounded

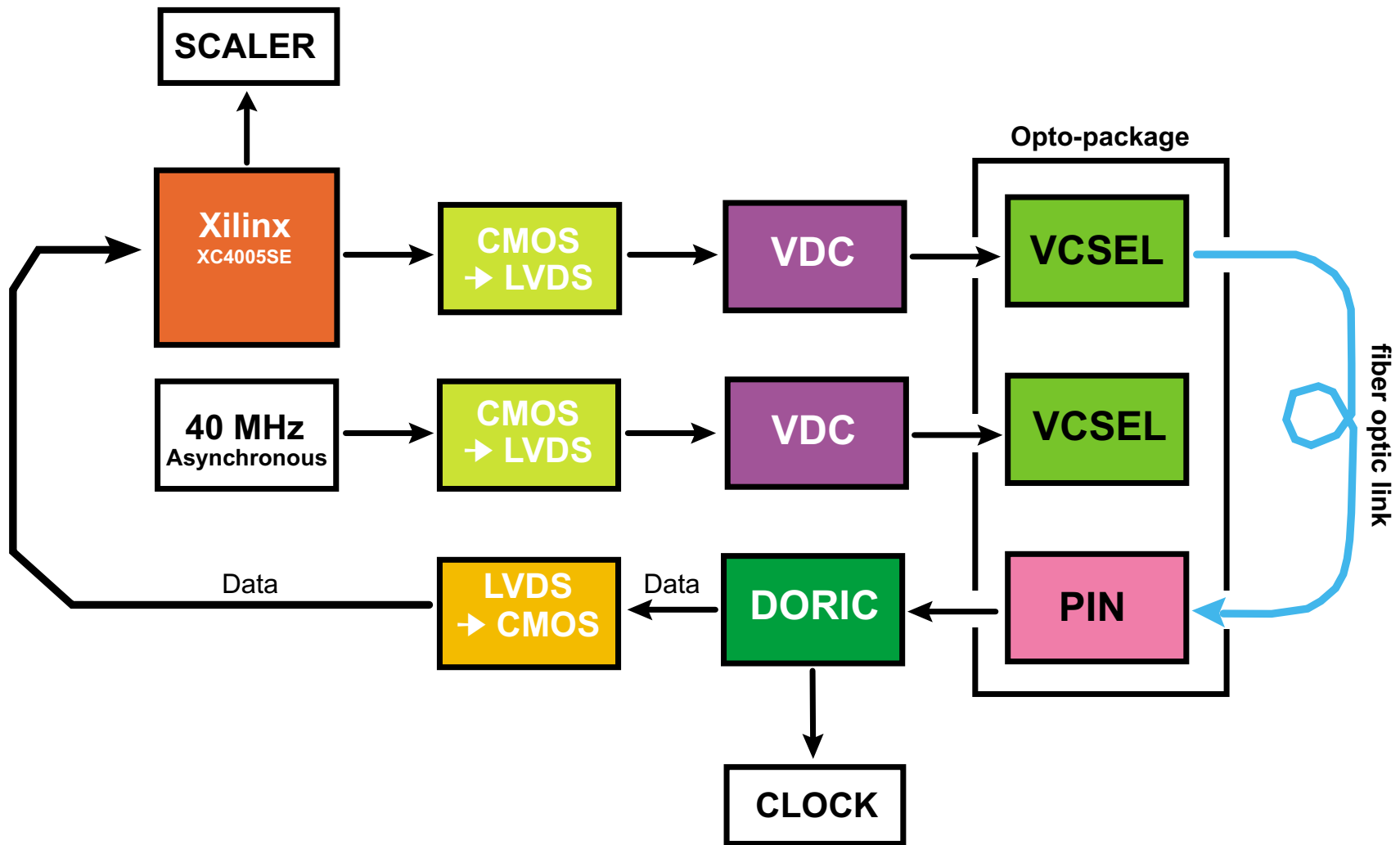
Decoded clock

Decoded data

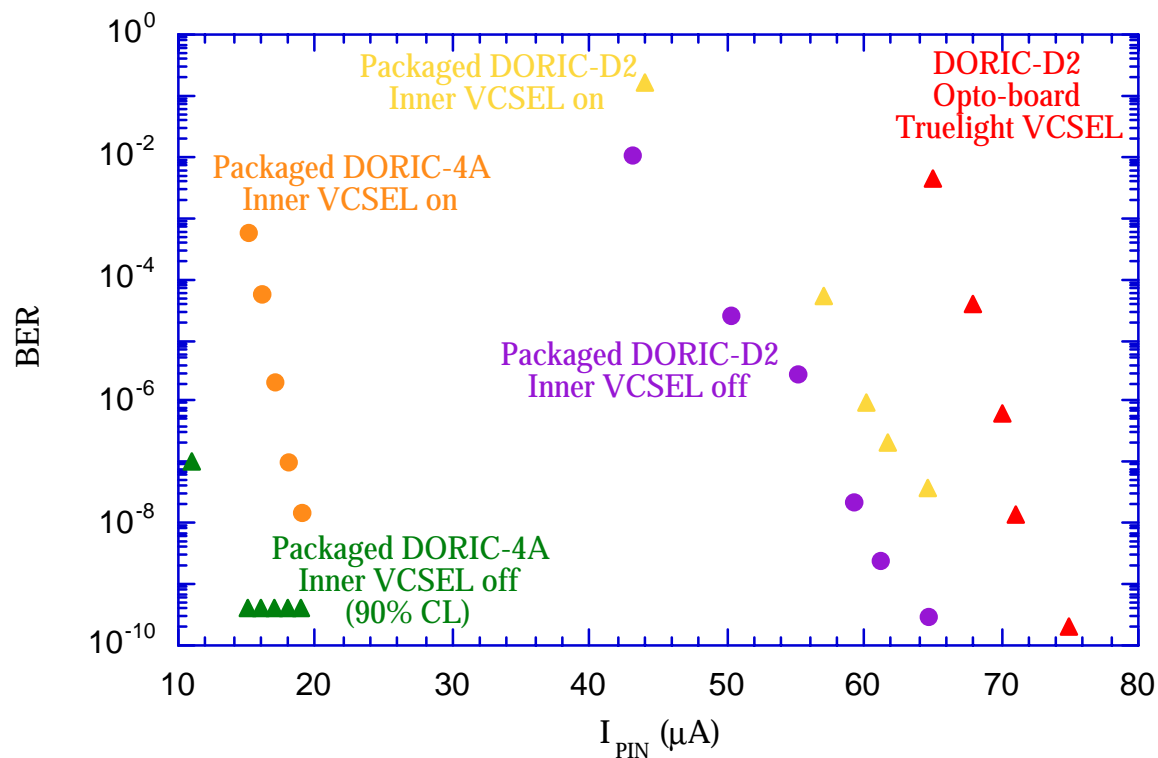
Input data



BER/Crosstalk Measurement with DORIC and VDC



Binary Error Rate



- DORIC-D2 has significantly more cross talk than DORIC-4A
- placing DORIC-D2 in close proximity to PIN yields similar BER

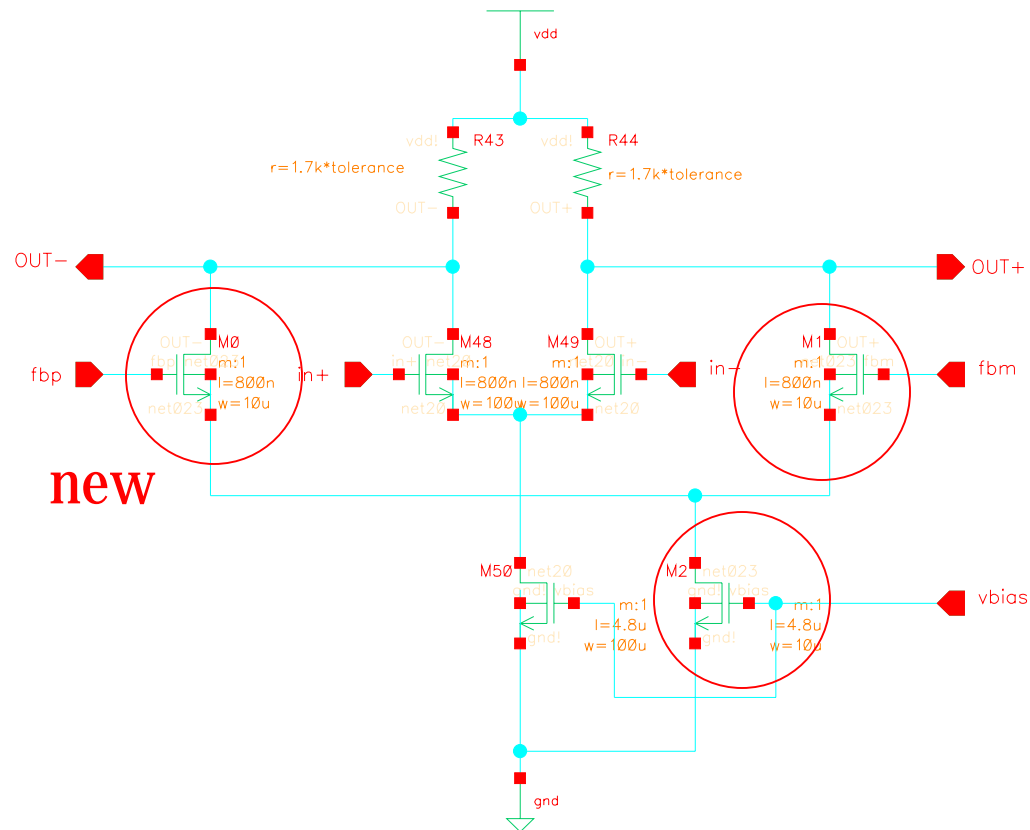
Investigation of Cross-talk

- observe spikes at edge-detector and pre-amp spy points
- pulsing test spy circuit induces a signal at LVDS outputs
- floating and grounding guard-ring has no effect on pre-amp
- back side silicon is highly resistive: $\sim 1 \text{ M}\Omega$
 - ☆ reduce to $\sim 100 \text{ K}\Omega$ when scratched
- currently investigating possibility of grinding and metalizing back side of bare dice

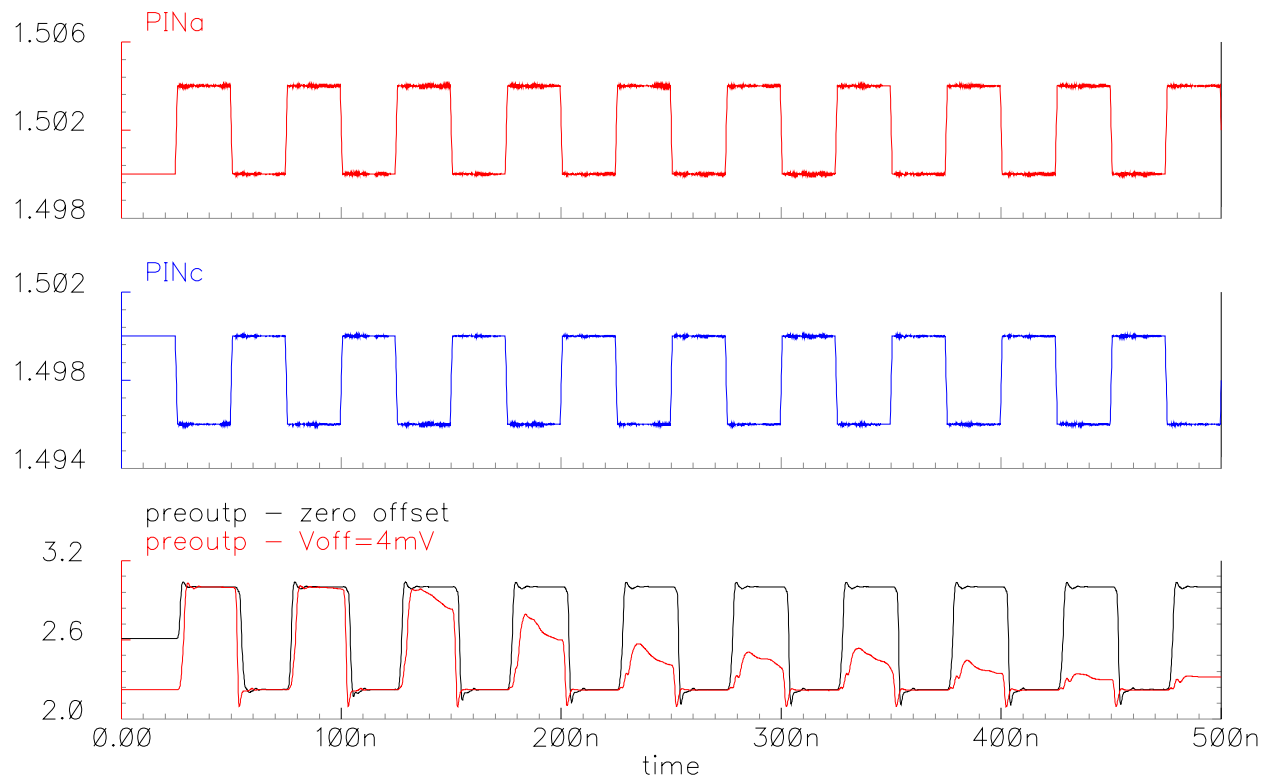
Pre-amp Offset

- 600 mV different at pre-amp +/- spy point outputs
- pre-amp has low gain for small signal and output distorted
- pre-amp offset estimates to be a few mV
- has designed a dc feedback circuit for DORIC-I
 - ☆ simulation shows that it will fix offset problem
 - ☆ need to include stray capacitance of traces in simulation to verify that circuit will not oscillate

Pre-amp with Feedback

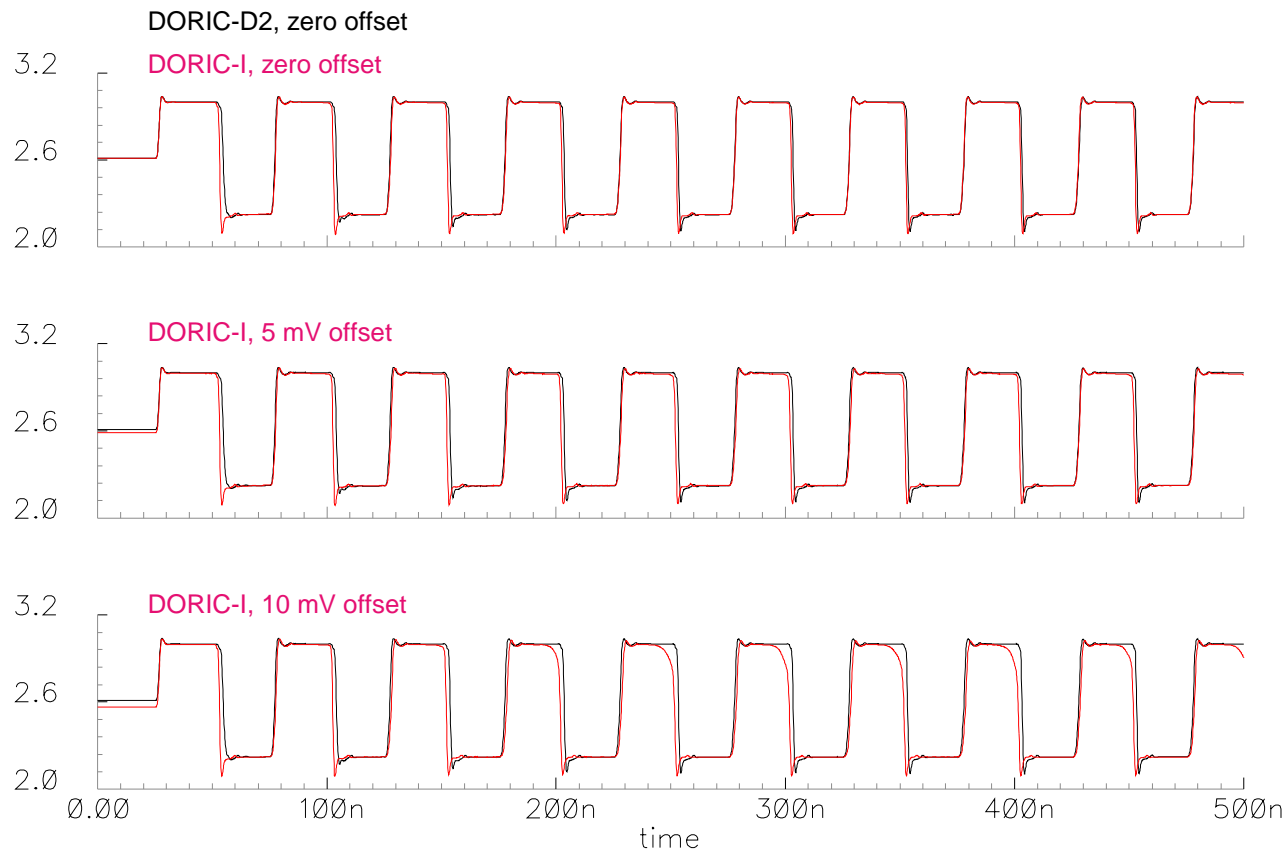


Simulation of DORIC-D2 Pre-amp



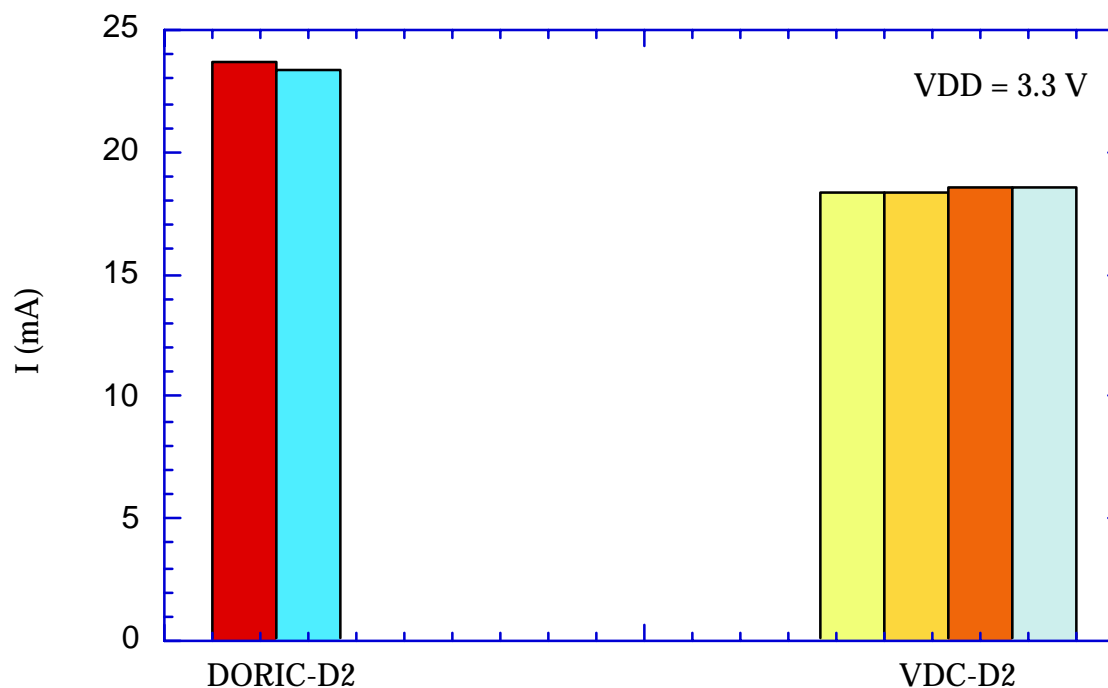
- no output signal for small input signal if there is an offset

Simulation of DORIC-I Pre-amp



- produce output signal similar to an pre-amp with no offset

Power Consumption



- current consumption consistent with expectations
- 7-channel opto-board:
 - ☆ 1.0 W @ 10 mA VCSEL current
 - ☆ 1.4 W @ 20 mA VCSEL current

Plans

- VDC-D2 and DORIC-D2 work but with some deficiencies
 - ☆ VDC-D2: some have low dim currents
 - ☆ DORIC-D2:
 - some pre-amps have small offset
 - cross-talks inside die
- will emphasize irradiation of DORIC-D2 in April
 - ☆ a new rad-hard bias circuit without requiring a reset is needed for any DMILL submission