Radiation-Hard ASICS for Optical Data Transmission in the First Phase of the LHC Upgrade

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Outline

● Introduction
● Result on VCSEL Driver Chip
● Result on PIN Receiver/Decoder Chip
● Summary
ATLAS proposed to add one more layer to the current pixel detector:
- “Insertable B-Layer” or IBL
- installation ~ 2015-6
- optical links will use VCSEL/PIN array as in current pixel detector
- an updated version of current driver (VDC) and receiver (DORIC) with redundancy and individual VCSEL current control would be a logical improvement
- experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
  - submission of 1st prototype chip (130 nm) in 2/2010
Chip Content

Design

VCSEL Driver (spare)
VCSEL Driver
VCSEL Driver with pre-emphasis
VCSEL Driver with pre-emphasis
CML Driver with pre-emphasis
Decoder (40Mb/s)
Decoder (40Mb/s)
Decoder (40Mb/s)
Decoder (40/80/160/320 Mb/s, spare)

Photo

1.5 mm
PIN Receiver/Decoder

Prototype chip only.
Command Decoder Interface

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders

In prototype chip only

Command Word

<table>
<thead>
<tr>
<th>COMMAND WR</th>
<th>STEER</th>
<th>STEER VDC/DORIC</th>
<th>SET DAC</th>
<th>CH. SELECT</th>
<th>DAC VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(15)</td>
<td>(14)</td>
<td>(13)</td>
<td>(12)</td>
<td>(11:8)</td>
<td>(7:0)</td>
</tr>
</tbody>
</table>
Test Card

Test card

PIN opto-pack
ULM 5 Gb/s

chip
Recovered Clock/Data

320 Mb/s

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Jitters/Thresholds

✔ Peak-to-peak clock jitter:
  - 40 Mb/s: 132 ps (normal)
  - 40 Mb/s: 1420 ps (multi speed)
  - 80 Mb/s: 750 ps
  - 160 Mb/s: 193 ps
  - 320 Mb/s: 103 ps

✔ Threshold for no bit errors:
  - 40 Mb/s:
    - Multi speed: 40 \( \mu \)A
    - Ch 1: 19 \( \mu \)A
    - Ch 2: 22 \( \mu \)A
    - Ch 3: 20 \( \mu \)A
  - 80 Mb/s: 58 \( \mu \)A
  - 160 Mb/s: 74 \( \mu \)A
  - 320 Mb/s: 110 \( \mu \)A
PIN Receiver/Decoder

✔ All channels work at 40 Mb/s

● Multi Speed version works at 40, 80, 160, and 320 Mb/s
  ◆ 160 and 320 Mb/s need external bias tuning for proper operation

✔ Steering signal to the spare channel works
VCSEL Driver Chip

Channel Select (3:0) -> Set DAC

Command Write

DAC Bits (7:0)

Write Enable (3:0)

LVDS input added for prototype chip only.

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VDC Results

- Power-on reset circuit
  - an open control line disables 6 opto-links in current pixel detector
  - implemented power-on reset circuit in prototype chip
  - chips power up with several mA of VCSEL current

- Test port
  - can steer signal received to spare VDC/VCSEL
  - can set DAC to control individual VCSEL currents

- All 4 channels run error free at 5 Gb/s
  - includes the spare with signal routed from the other LVDS inputs
VDC Test Setup

- Light from the 4 VCSELs:
  - Fiber aligned over VDC/VCSEL 2
VCSEL Driver with Pre-Emphasis

✔ Pre-emphasis working with tunable width and height

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160 Mb/s
Eye Diagrams @ 4.8 Gb/s

- No pre-emphasis
- Rise/fall times: ~60-90 ps
  - Measured with 4.5 GHz optical probe
- Bit error rate < 5x10^{-13}
Irradiation

- 2 chips were packaged for irradiation with 24 GeV/c protons at CERN in August
  - each chip contains 4 channels of drivers and receivers
  - total dose: $1.6 \times 10^{15}$ protons/cm$^2$
  - all testing are electrical to avoid complications from degradation of optical components
    - long cables limited testing to low speed
  - observe little degradation of devices
    - evaluation of full performance await return of devices to labs
- Previous VDC prototypes (130 nm) were irradiated in 2009
- VDC driving 25 Ω with constant control current
- Drive current decreases with radiation for constant
  - Driver circuit fabricated with thick oxide process
  - PMOS and NMOS have different threshold voltage shifts
  - Use only PMOS in the current mirror in 2010 prototype
- new VDC also drives 25 Ω with constant control current
- Decrease in drive current is small!

$1.6 \times 10^{15} \text{ p/cm}^2$
Single Event Upset

- SEU harden latches or DAC could be upset by traversing particles
  - 40 latches per 4-channel chip
  - SEU tracked by monitoring the amplitude of VDC drive current
  - 13 instants (errors) of a channel steered to a wrong channel in 71 hours for chip #1
    - similar upset rate in chip #2
      - $\sigma = 3 \times 10^{-16} \text{ cm}^2$
    - particle flux $\sim 3 \times 10^9 \text{ cm}^{-2}/\text{year} @ \text{opto-link location}$
      - SEU rate $\sim 10^{-6}/\text{year/link}$
Summary

- prototyped opto-chip for 2\textsuperscript{nd} generation ATLAS pixel opto-links incorporated experience gained from current links
  - add redundancy to bypass broken PIN or VCSEL channel
  - add individual VCSEL current control
  - add power-on reset to set VCSEL current to several mA on power up
  - VCSEL driver can operate up to \( \sim 5 \) Gb/s with BER < \( 5 \times 10^{-13} \)
  - PIN receiver/decoder properly decodes signal with low threshold
  - little decrease in VCSEL driver output current
  - very low SEU rate in latches/DAC
  - all added functionalities work!

All results are preliminary