Rad-Hard Opto-Link Upgrade

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Outline

- Upgrade plan/requirements
- Bandwidth of micro twisted-pair cables
- Bandwidth of fusion spliced SIMM-GRIN fibers
- Radiation hardness/speed of PIN/VCSEL arrays
Current Opto-Link Architecture

- Plan: upgrade based on current pixel link architecture to take advantage of R&D effort and production experience.

- micro twisted pairs decouple pixel and opto module ⇒ simplify both design/production.

- 8 m of rad-hard/low-bandwidth SIMM fiber fusion spliced to 70 m rad-tolerant/medium-bandwidth GRIN fiber.
Proposed Opto-Link Architecture

Current:
- FE/MCC
- 1 m wires
- Commands
- Data
- DORIC
- PIN
- VDC
- VCSEL
- 80 m fibers
- TTC
- 40 MHz
- 80 Mb/s

Proposed:
- FE
- Serializer/VDC
- 160 Mb/s
- 160 MHz
- TTC
- 640 Mb/s
Possible GBT-Lite Architecture

- **Module 1**
  - (160 Mb/s)
  - SEU Tolerant Serializer
  - 8b/10b Encoder

- **Module n**
  - (160 Mb/s)
  - SEU Tolerant Serializer
  - 8b/10b Encoder

- **CLK 4X**
- **CLK 5X**

- **XCK (160 MHz)**
- **DTO 1**
  - 800 Mb/s
  - 8b/10b

- **DTO n**
  - 800 Mb/s
  - 8b/10b
Case for DC Balancing in Opto-Link

- Some VCSELs require µs to produce full optical power
- Pixel TTC opto-link has been quite easy to operate
- Commercial high speed opto links are mostly DC balanced
  ⇒ DC balancing will likely make a more robust uplink!
Increasing Functionality in VDC?

- lost of VCSEL:
  - add capability to reroute data in VDC to spare VCSEL?
- difficult to operate present data links due to optical power spread in VCSEL arrays:
  - add current adjustment for each VCSEL channel?
VDC with Rerouting Capability?

Control Lines From DORIC

- Control Interpreter
- SEU Tolerant DACs
  - 1.5 to 2.5 V Logic Translator
- ISET & IBIAS
- VCSEL Driver
- ISET & IBIAS
- VCSEL Driver

- LVDS “like” Receiver
- SEU Tolerant DACs
  - 1.5 to 2.5 V Logic Translator

VDD = 1.5 V
VDD = 2.5 V

DTO (800 Mb/s)
VDC Status

- thick oxide (2.5 V) transistors are enclosed devices
- extracted simulations indicate bandwidth > 1 Gb/s
DORIC Status

- simulations of transimpedance amplifier + limiting amplifier yield 50% duty cycle for input current of 20-1000 µA
- preliminary simulations of LVDS “like” driver promising
Upgrade Feasibility with Present Infrastructure

- can micro twisted pair transmit at 160 MHz?
- can PIN operate at 160 MHz?
- can PIN array survive B-layer radiation dosage?
- can high-speed VCSEL array survive B-layer radiation dosage?
- can fusion spliced SIMM/GRIN fiber transmit at 640 Mb/s?
- we already know some of the answers from SLHC R&D
Bandwidth of Micro Twisted Pairs

- current pixel cable with thick insulation is quite optimum!
Eye Diagrams

- Transmission at 640 Mb/s is adequate
- Transmission at 1280 Mb/s may be acceptable
- 127 µm cable is slightly better
Bandwidth of Fusion Spliced Fiber

- 1 m GRIN fiber
- 8 + 80 m spliced SIMM/GRIN fiber

- transmission up to 2 Gb/s looks adequate
- current fibers can be reused
- current system uses 6-7 channels in 8-channel array/ribbon
- some spare ribbons were installed
- can have modest increase in # pixel modules
Si PIN responsivity decreases by 65\% after SLHC dosage

operation at 160 MHz is OK

completed irradiation of GaAs PIN from 3 vendors:

- Optowell, AOC, ULM
- responsivities will be measured soon
**VCSEL Power vs Dosage**

- irradiated VCSELs from 3 vendors to SLHC dosage
- all are acceptable for B layer replacement

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B Layer Workshop
Opto-Pack Development

- Current pixel detector uses Taiwan optical packages
  - VCSEL mounted on PCB with poor heat conduction
  - Micro soldering of 250 μm leads is difficult
- Ohio State develops new opto-pack for SLHC
  - Uses BeO base with 3D traces for efficient heat removal
  - Wire bond to driver/receiver chip
Results on Opto-Packs

- 35 VCSEL & 6 PIN opto-packs have been fabricated
  - all VCSEL opto-packs except one have good coupled power
  - principle of new opto-pack has been demonstrated
Summary

- Simple VDC design completed
  - VDC with more functionality proposed
- DORIC design in progress
  - Micro twisted-pair cable of current ATLAS pixel detector can be used for transmission up to 1 Gb/s
  - Fusion spliced SIMM/GRIN fiber can transmit up to 2 Gb/s
  - Si PIN can be operated up to 160 MHz
    - GaAs PIN evaluation in progress
  - Good high speed VCSELs from 3 vendors
  - Compact MT-style opto-pack based on BeO has been developed
  - Current opto-link architecture satisfies B-layer requirements