Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

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January 10, 2004

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Outline

- NLC Requirements
- ADC Design
- Progress Report
- Plans
Beam Position Monitor Requirements at NLC

- NLC will collide 180-bunch trains of e⁻ and e⁺:
  - bunch spacing: 1.4 ns
  - alignment of individual bunches in a train: < 1 μm
  - BPM determines bunch-to-bunch misalignment
  - high bandwidth kickers bring the train into better alignment on next machine cycle
- multi-bunch BPM system with digitizers:
  - 11-bit effective resolution
  - 500 MHz bandwidth
  - 2 G samples/s
## Requirements of NLC Digitizers

<table>
<thead>
<tr>
<th>Function</th>
<th>Qty.</th>
<th>Resolution (eff. bits)</th>
<th>Bandwidth (MHz)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LLRF Control</td>
<td>13,000</td>
<td>11</td>
<td>100</td>
<td>Slightly beyond state-of-the-art</td>
</tr>
<tr>
<td>Structure BPM</td>
<td>22,000</td>
<td>8</td>
<td>5</td>
<td>Existing technology</td>
</tr>
<tr>
<td>“Qaud” BPM</td>
<td>10,000</td>
<td>11</td>
<td>12</td>
<td>Existing technology</td>
</tr>
<tr>
<td>Multi-bunch BPM</td>
<td>1,200</td>
<td>11</td>
<td>500</td>
<td>Well beyond state-of-the-art</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>46,200</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Important to demonstrate feasibility of high speed/resolution digitizers
- Redesign of low level RF technology is needed without the digitizers
Proposal

- design a digitizer chip using deep-submicron technology (0.25 \( \mu \)m)
  - use enclosed layout transistors and guard rings
    - radiation hard: > 60 Mrad
    - no need for costly shielding and long cables
    - readily access to electronics for testing and maintenance

- extensive experience in chip design using Cadence
  - designed radiation-hard chips for CLEO III, ATLAS, CMS

- why OSU is interested?
  - help to solve a challenging NLC problem
  - potential applications in HEP

- 2002 Holtkamp Committee ranking: 2 on scale of 1 to 4 (lowest)
  - funded for 2003-4
12-bit Pipelined Digitizer

- input crudely digitized by 1st 3-bit cell
- digitized value subtracted from input
- difference is amplified by 8 and sent to 2nd 3-bit cell…
Digitizer for Multi-bunch BPM

- most challenging digitizer: 11 bit, 2 G samples/s, 500 MHz bandwidth

- input: sequence of doublets at 1.4 ns batch spacing
  - characterize with one parameter: pulse height
  - minimum sampling: 1/1.4 ns = 714 MHz
    - interleaving 3 digitizers for redundancy
    - 2 G samples/s
Precision

- submicron CMOS supply voltage: 2.5 V
  - differential signal: ~ 1.6 V full swing
  - LSB: $1.6 \, \text{V} / 2^{12} = 390 \, \mu\text{V}$
  - stability/accuracy of comparator thresholds, amplifier & S/H gains, charge injection:
    $195 \, \mu\text{V} = 0.5 \, \text{LSB} = 0.5 / 2^{12} = 0.012\%$
Fabrication Process

- gain-bandwidth requirement:
  - assume 0.7 ns for sample and 0.7 ns for hold
  - settling to 0.5 LSB for 12-bit digitizer requires $9 \cdot \frac{0.5}{2^{12}} \sim e^{-9}$
    - $t = \frac{0.7 \text{ ns}}{9} = 78 \text{ ps}$
    - rise time $= 2.2 \cdot t = 171 \text{ ps}$
    - gain x bandwidth $= 8 \times \frac{1}{2^{12}} \cdot t = 16.4 \text{ GHz}$
  - IBM process SiGe BiCMOS 6HP/6DM via MOSIS: 40 GHz NPN bipolar transistors
3-Bit Cell
3-Bit Cell Status

- simulated with Cadence
  - sample/hold + flash ADC/flip-flop: designed/simulated from schematic with parasitic capacitances
  - multiplexer: logic is fast but somewhat noisy
  - op-amp + encoder: still use ideal devices in simulation
design and simulated from schematic with parasitic capacitances
switch-on resistance small enough to allow 9\(\text{in}\) in 700 ps
switching offset (noise) largely cancelled with dummy switch:
\(100 \text{ mV} \Rightarrow 1 \text{ mV}\)
Cadence Simulation of Sample/Hold

Amplifier: ideal

Amplifier: current design

switch charge injection

amplifier signal not yet settle to 0.5 LSB in 0.7 ns

K.K. Gan

US LC Conference
Simulation of Amplifier

- rise time: 186 ps
- goal: 171 ps:
- precision at 0.7 ns:
  \[
  \frac{298 \text{ mV}}{270 \text{ mV}} \times 2^{10}
  \]

⇒ need 4x improvement for 12-bit precision
Plans

- **Year 2003-4:**
  - complete design of amplifier + 3-bit cell

- **Year 2004-5:**
  - layout, submission, and testing of the building block circuits
  - radiation hardness tests
  - continued system design of a prototype 11-bit digitizer