Radiation-Hard ASICs for Optical Data Transmission

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***Abstract*– We have designed two ASICs for possible applications in the optical links of a new layer of the ATLAS pixel detector. This new layer is to be installed inside the existing pixel detector for the initial phase of the LHC luminosity upgrade. The ASICs include a high-speed driver for a VCSEL and a receiver/decoder to extract the data and clock from the signal received by a PIN diode. Both ASICs contain 12 channels for operation with a VCSEL or PIN array. The ASICs were designed using a 130 nm CMOS process to enhance the radiation-hardness. The fabricated receiver/decoder properly decodes the bi-phase marked input stream with low PIN current. We are able to program the ASIC to bypass a broken PIN. The power-on reset circuit is also successfully implemented which sets the ASIC to a default configuration with no signal steering. We are awaiting the delivery of the VCSEL driver but some of the salient features of the design will be described.**

I. INTRODUCTION

The Large Hadron Collider (LHC) at CERN (Geneva) is currently the highest energy and luminosity collider in the world. However, planning has already been initiated to increase the design luminosity by a factor of five to $5x10^{34}$ $cm^{-2}s^{-1}$. The ATLAS experiment at the LHC plans to add a new pixel layer to the current pixel detector during the 2013 shutdown. As a result, the optical data transmission will require an upgrade to handle the higher data transmission speed. The upgrade for the optical links will be based on VCSEL and PIN arrays operating at 850 nm as in the current system. In preparation for the upgrade, two new ASICs, a 12-channel array driver and a 12-channel array receiver, have been designed using a 130 nm CMOS process for this new generation of optical links.

The ASICs [1] have been designed using IBM's 130 nm 8RF-DM CMOS process. The driver couples to a VCSEL array with one channel designated as a spare. Similarly for a receiver/decoder couples to a PIN array. With the inclusion of a remote control interface, this allows redundancy in both directions by enabling a signal to be re-routed from a bad VCSEL or PIN channel. The submitted chip contains twelve VCSEL drivers (VDC), twelve PIN diode receivers/decoders, and the associated circuitry to control the re-routing of the signals to the designated spare channels. All circuitry within the test chip was designed following test results and guidelines from CERN on radiation tolerant design in the 130 nm process used [2]. We have characterized the fabricated receiver/decoder and the results will be presented below.

II. PIN RECEIVER/DECODER ASIC

The PIN receiver/decoder ASIC contains twelve PIN diode receiver/pre-amplifiers. For the inner eight channels, each circuit also contains a 40 Mb/s bi-phase mark (BPM) clock/data recovery circuit with low voltage differential signal (LVDS) outputs for both the clock and data transmission to a front-end (FE) chip of a pixel module A five-channel multiplexer has been inserted in the post amplification path of each channel. If the PIN diode in one of the inner eight channels is non-functional, the multiplexer for that channel would accept the signal from a spare channel so that the BPM signal can be decoded for transmission to the appropriate FE chip. All circuits are designed to operate with a 1.5 V power supply. A block diagram of the ASIC is shown in Fig. 1.

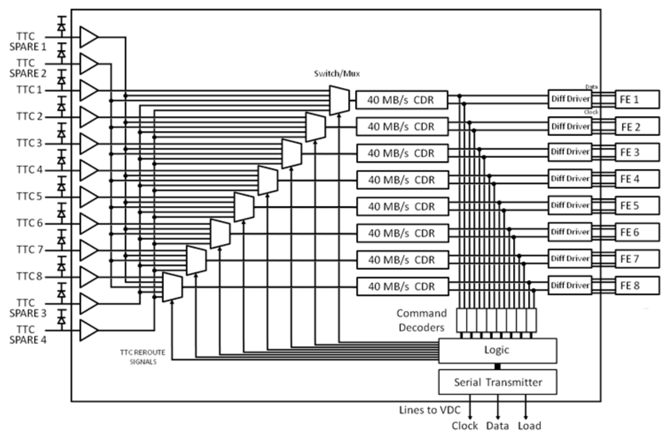

Fig. 1. Block diagram of the PIN receiver/decoder circuit.

In order to allow remote control over channel steering and other functionality within the chip, a command decoder has been included for each of the inner eight channels. The command decoder was designed for the FE chips of the new pixel layer. The command processor will act if a valid command is received on any command decoder. This allows working control if only one PIN channel is still alive. Because the chips will be resided in a high radiation environment, special care was taken to improve the single event upset (SEU) tolerance of the command decoder. In addition, all latches are based on a dual interlocked storage cell (DICE) latch designed for use in the configuration memory of the FE chips of the pixel detector.

The clock/data recovery circuits of all channels can properly decode the data at 40 Mb/s with no bit errors for low input PIN currents. The PIN current threshold (amplitude) for no bit errors is < 20 μA with only single channel active. The

Manuscript received November 15, 2011. This work was supported in part by the U.S. Department of Energy under contract No. DE-FG-02-91ER-40690 and by the German Federal Minister for Research and Technology (BMBF) under contract No. 056Si74.

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PIN current thresholds are 40-60 μA for all channels active with or without spares channels being steered over full length of the chip. These are higher than we would like and might be due to the long lead connecting the circuit to a PIN diode or problems with the supply routing/decoupling on the circuit board used to test the chips. These problems are under investigation. However, we expect to operate the chip with at least 100 μA of PIN current to minimize SEU induced by traversing charged particle and hence the above acceptable.

Figure 2 shows the eye diagrams of the recovered data and clock. The rise and fall times are ~0.5 ns. The clock jitter (peak-to-peak) at 40 Mb/s is ~1.4 ns for both single-speed and multi-speed channels. For the multi-speed channel, the jitter is smaller at higher operating speed, as little as ~100 ps at 320 Mb/s. It should be noted that the multi-speed channel requires external bias tuning for proper operation at 160 and 320 Mb/s due to the limited dynamic range of the clock duty cycle control circuitry. The steering circuit functions properly, i.e. signal received at the spare DORIC channel can be rerouted through the other DORIC channels. However, this can only be excised via the test port because the scan chain enable of the command decoder was left floating due to a miscommunication with the designer of the command decoder.

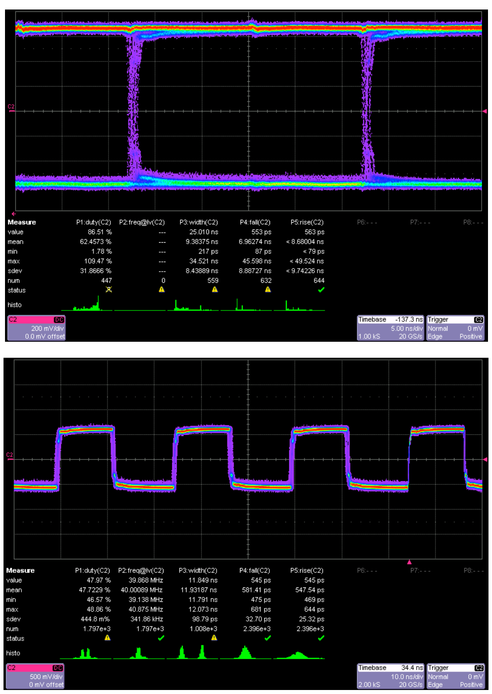

Fig. 2. Eye diagram of recovered data (top) and clock (bottom).

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Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use “Ref. [3]” or “reference [3]” except at the beginning of a sentence: “Reference [3] shows ... .” Type the reference list at the end of the paper using the “References” style.

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$$\int_0^{r_2} F(r,\varphi)\,dr\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda . \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm × 0.2 cm," not "0.1×0.2 cm^2." Do not mix complete spellings and abbreviations of units: use "J/cm^2" or "fluence per square centimeter," not "fluence/cm^2." When expressing a range of values, write "7 to 9," not "7-9" or "7~9," except for references [1]-[3].

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means "for example." An excellent style manual and source of information for science writers is [9]. A general IEEE style guide, *Information for Authors,* is available at http://www.ieee.org/portal/cms_docs/pubs/transactions/auinfo03.pdf.

Appendix

Appendices, if needed, appear before the acknowledgment.

Acknowledgment

We thank Tony Seibert for writing the original version of this document.

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