



Pixel Opto-board QA

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Pixel Opto-Board QA

Abstract

This document describes the mechanical and electrical QA for the Pixel opto-board and its components.

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1 SCOPE OF THE DOCUMENT

This document defines the mechanical, electrical and optical measurements that will be performed on the components of the opto-board and the associated accept/reject criteria.

2 INTRODUCTION

The ATLAS pixel detector has three barrel layers and six disks. For the outer two barrel layers (L1 and L2) and disks, each opto-board contains seven data and clock/command links. Each data link contains one VDC (VCSEL Driver Chip) channel driving a VCSEL channel. Each clock/command link contains one DORIC (Digital Opto-Receiver Integrated Circuit) channel receiving a signal from a PIN channel. The DORIC and VDC are fabricated in a 4-channel array while the VCSEL and PIN in an 8-channel array. Therefore each opto-board contains two VDCs and DORICs and one PIN and VCSEL opto-packs. All individual components must be certified to meet the QA before being mounted on an opto-board. The assembled opto-board must then pass the QA for mounting onto the PP0. In view of maximizing the number of available spares, all opto-boards will contain seven links although six links are needed in about half of the opto-boards. The ASICs must be tested at 2.5 V and the PIN currents refer to the current amplitude. The PRBS (Pseudo Random Bit String) used in the test must be bi-phase mark (BPM) encoded on a 40 MHz clock.

For the inner barrel layer (B), there are fourteen data links to handle the higher occupancy and hence the opto-board has two more VDC chips and one more VCSEL opto-pack.

3 QA DEFINITIONS OF THE ASICS

3.1 VDC QA

VDC converts an input LVDS signal into an output current appropriate to drive a VCSEL. There is a control current (I_{set}) to adjust the “bright” (on) current. A “dim” (off) current is generated to ensure fast on/off switching of the VCSEL.

We perform a simple test of the VDC due to the high yield. A 20 MHz signal is sent to all channels simultaneously with I_{set} at 0.5 mA and each channel drives a 25 Ω to simulate a VCSEL. The current consumption is required to be ~75 mA. The output of each channel should show a respectable signal and all signals should look similar in amplitudes.

Since the above test is good enough to produce opto-boards of high yield, the following tests (and the corresponding QA requirements) as originally planned are now unnecessary.

Table 1: VDC measurements

Test	Item	Comments
1.1	current consumption	
1.2	$I_{bright} / I_{dim} - I_{set}$ curve	DC measurement
1.3	rise & fall time, duty cycle	40 MHz, $I_{set} = 0.6$ mA

This will result in the pass/fail tests listed in Table 2.

Table 2: VDC QA

Test	Item	Units	Min	Max	Comments
2.1	current consumption	mA	54	66	40 MHz, $I_{set} = 0.6$ mA
2.2	V_{set}	V	0.8	1.0	$I_{set} = 0.6$ mA
2.3	I_{bright}	mA	10	-	$I_{set} = 0.6$ mA
2.4	I_{bright}	mA	20	-	$I_{set} = 1.5$ mA
2.5	I_{dim}	mA	0.8	1.1	$I_{set} = 0.6, 1.5$ mA
2.6	rise & fall time	ns	-	1	40 MHz, $I_{set} = 0.6$ mA
2.7	duty cycle	%	46	54	40 MHz, $I_{set} = 0.6$ mA

3.2 DORIC QA

The DORIC decodes the BPM signal received by a PIN into clock and command LVDS signals. We perform a simple test of the DORIC due to the high yield. Four independent BPM signals are sent to the four channels of the DORIC simultaneously. The BPM signal corresponds to a data bit for every 16 clock cycles. The PIN current in each channel is set to be $\sim 500 \mu\text{A}$. The current consumption is required to be $\sim 80 \text{ mA}$. Both polarities of the decoded LVDS clocks should have a frequency of 40 MHz with approximately the expected amplitude. Similarly the decoded command signals should have the correct data structure, 1 in 16, with approximately the expected amplitude.

Since the above test is good enough to produce opto-boards of high yield, the following tests (and the corresponding QA requirements) as originally planned are now unnecessary.

Table 3: DORIC measurements

Test	Item	Comments
3.1	current consumption	
3.2	LVDS clock	
3.2.1	common mode & amplitude	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
3.2.2	rise & fall time	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
3.2.3	jitter, duty cycle	PRBS @ $I_{\text{PIN}} = 50, 100, 1000 \mu\text{A}$
3.3	LVDS command	
3.3.1	common mode & amplitude	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
3.3.2	rise & fall time	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
3.3.3	delay w.r.t. clock	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
3.3.4	BER – I_{PIN} curve	PRBS @ $I_{\text{PIN}} = 50, 100, 1000 \mu\text{A}$

This will result in the pass/fail tests listed in Table 4.

Table 4: DORIC QA

Test	Item	Units	Min	Max	Comments
4.1	current consumption	mA	67	81	without input and PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.2	clock +/- common mode	V	0.9	1.1	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.3	clock +/- amplitude	V	0.32	0.40	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.4	clock rise & fall time	ns	-	1	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.5	clock jitter	ns	-	1	PRBS @ $I_{\text{PIN}} = 50, 100, 1000 \mu\text{A}$
4.6	clock duty cycle	%	46	54	PRBS @ $I_{\text{PIN}} = 50, 100, 1000 \mu\text{A}$
4.7	command +/- common mode	V	0.9	1.1	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.8	command +/- amplitude	V	0.32	0.40	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.9	command rise & fall time	ns	-	1	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.10	command delay w.r.t. clock	ns	0	3	PRBS @ $I_{\text{PIN}} = 100 \mu\text{A}$
4.11	bit errors	-	-	0	PRBS @ $I_{\text{PIN}} = 50, 100, 1000 \mu\text{A}$ for 100 s

4 QA DEFINITIONS OF THE OPTO-BOARD

An assembled opto-board must pass both the mechanical and electrical QA listed below.

4.1 MECHANICAL QA

The opto-board must fit inside a volume of 7 x 19.55 x 80 mm³. A jig containing a male 80-pin connector will be used for the test. When the opto-board is mounted on the connector, it must fit inside the jig or else be rejected.

4.2 OPTO-ELECTRICAL QA

The measurements that must be performed on an opto-board after the burn-in are listed in Table 5. The results on the optical power measurement must be stored in the PDB.

Table 5: Opto-board measurements

Test	Item	Comments
5.1	current consumption	$I_{set} = 0.55 \text{ mA}$, PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
5.2	L	$I_{set} = 0.55 \text{ mA}$
5.3	rise & fall time	40 MHz @ $I_{set} = 0.55 \text{ mA}$, PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
5.4	jitter	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$
5.5	duty cycle	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$
5.6	clock & command common mode/amplitudes	PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
5.7	dark current	+10 V
5.8	BER	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$

This will result in the pass/fail tests listed in Table 6.

Table 6: Opto-board QA

Test	Item	Units	Min	Max	Comments
6.1	current consumption	mA	177	217	330-400 mA for opto-board with 14 data links
6.2	L	μW	500	-	$I_{set} = 0.55 \text{ mA}$ and change of no more than 20% from the opto-pack QA value
6.3	rise & fall time	ns	-	1	40 MHz @ $I_{set} = 0.55 \text{ mA}$, PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
6.4	jitter	ns	-	1	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$
6.5	duty cycle	%	46	54	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$
6.6	clock and command +/- common modes	V	0.9	1.5	PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
6.7	clock and command +/- amplitudes	V	0.2	0.5	PRBS @ $I_{PIN} = 100 \text{ }\mu\text{A}$
6.8	dark current	μA	-	1	+10 V
6.9	bit errors	-	-	0	PRBS @ $I_{PIN} = 50, 1000 \text{ }\mu\text{A}$ for 60 mins with all links active

5 REFERENCES