



MUON Cathode
FE Electronics



SCA Master FPGA Test

Code: /home/fast/fastdaq/daqmb-new2.8/Utils/rad_test.c
/home/fast/fastdaq/daqmb-new2.8/Utils/rdbkfpfga.c

Running: 1. select SCAM run test
2. write down time for run start
3. monitor current for latchup

Test1 Configurations: digital : (1:100) flags: cbits-# bits checked bbits-#bad bits
Checks FPGA configuration memory.

On Error: do nothing but write summary to output

Test2 Capacitor Error: digital: (1:1) flags -errcap
Looping on pedestal pulser read back and predict future capacitor blocks and check prediction with ddu readout. Blocks should alternate:
e.g. 0123 4567 0123 4567 ...
An error here may not be fatal but may just be a spurious LCT.

On Error: write capacitor history to file
1st error (lev 0) – reset capacitor predictions
2nd error (lev 1) – global reset, ddu reset, reset capacitor predictions
3rd error (lev 2) – full reprogram, ddu reset, global reset, reset capacitor predictions

Test3 Read Error: digital: (1:1) flags -rerr
Buckeye 0 output is tied to SCAM read addresses.
The addresses are tested bit for bit (see error format below).

On Error: write ddu information to file.
1st error (lev 1) – global reset, ddu reset, reset capacitor predictions
2nd error (lev 2) – full reprogram, ddu reset, global reset, reset capacitor predictions

Test4 Write Error: digital: (1:1) flags -werr,werr2
Buckeye 0 output is tied to SCAM write addresses.
The addresses are tested bit for bit (see error format below).

werr- means ddu information is not correct
werr2- means capacitors that are being written disagree
with those predicted (similar to caperr)

On Error (werr2) : write capacitor history to file

- 1st error (lev 0) – reset capacitor predictions
- 2nd error (lev 1) – global reset, ddu reset, reset capacitor predictions
- 3rd error (lev 2) – full reprogram, ddu reset, global reset, reset capacitor predictions

On Error (werr): write ddu information to file.

- 1st error (lev 1) – global reset, ddu reset, reset capacitor predictions
- 2nd error (lev 2) – full reprogram, ddu reset, global reset, reset capacitor predictions

Test5 DDU Error: digital: (1:1) flags -ddu_err

ddu_err=1 Checksum error in readback. Probably not related
to a SCAM FPGA problem.

ddu_err=2 ddu has no data or wrong count

On Error: write capacitor history to file

- 1st error (lev 0) – do nothing
- 2nd error (lev 1) – global reset, ddu reset
- 3rd error (lev 2) – full reprogram, ddu reset, global reset

Output:

/home/fast/data/tmp_files/scamMMDD_HH:MM.dat
Error values and tables are written when an error occurs.

Display:

Terminal: every 100 pulses summary is displayed

```
hrs mins sec errs cnt somerrcnt errcap ddu_err  
wrerr2 werr rrerrr lev cbits bbits
```

Format:

/home/fast/data/tmp_files/scamMMDD_HH:MM.dat

Capacitor error:

hrs min secs error summary

hrs min secs event numberofcaperrs

capacitor history

```
0 0 0.30 cnt 11 somerrcnt 1 errcap 1 dduerr 0 wrerr2 0 wrerr 0 rrerr 0 lev 0 cnfig 249111 0 ddu 3140  
*** caperror 0 0 0.30 cnt 11 capcnt 1 errseq 0  
2 3 1 6 4 5 2 0 1 5 7 6
```

DDU error – 3140 bits read

```
0 0 2.40 cnt 21 somerrcnt 2 errcap 0 dduerr 2 wrerr2 0 wrerr 0 rrerr 0 lev 0 cnfig 249111 0 ddu 3140
*** dduerror 0 0 2.40 21
```

Read or Write error

```
0 0 4.54 cnt 31 somerrcnt 3 errcap 0 dduerr 0 wrerr2 0 wrerr 0 rrerr 1 lev 0 cnfig 249111 0 ddu 3140
*** rrerr 0 0 4.54 cnt 31
```

data format blkcapchan

```
buckeye 0
0 blk 7 data 734 735 736 737 738 739 73a 73b 73c 73d 73e 73f 730 710 711 712
1 blk 7 data 714 715 716 717 718 719 71a 71b 71c 71d 71e 71f 710 700 701 702
2 blk 7 data 704 705 706 707 708 709 70a 70b 70c 70d 70e 70f 700 f1d f1d f1d
3 blk 5 data 504 505 506 507 508 509 50a 50b 50c 50d 50e 50f 500 510 511 512
4 blk 5 data 514 515 516 517 518 519 51a 51b 51c 51d 51e 51f 510 530 531 532
5 blk 5 data 534 535 536 537 538 539 53a 53b 53c 53d 53e 53f 530 520 521 522
6 blk 5 data 524 525 526 527 528 529 52a 52b 52c 52d 52e 52f 520 560 561 562
7 blk 5 data 564 565 566 567 568 569 56a 56b 56c 56d 56e 56f 560 570 571 572
8 blk 5 data 574 575 576 577 578 579 57a 57b 57c 57d 57e 57f 570 550 551 552
9 blk 5 data 554 555 556 557 558 559 55a 55b 55c 55d 55e 55f 550 540 541 542
10 blk 5 data 544 545 546 547 548 549 54a 54b 54c 54d 54e 54f 540 f1d f1d f1d
11 blk 4 data 444 445 446 447 448 449 44a 44b 44c 44d 44e 44f 440 450 451 452
12 blk 4 data 454 455 456 457 458 459 45a 45b 45c 45d 45e 45f 450 470 471 472
13 blk 4 data 474 475 476 477 478 479 47a 47b 47c 47d 47e 47f 470 460 461 462
14 blk 4 data 464 465 466 467 468 469 46a 46b 46c 46d 46e 46f 460 420 421 422
15 blk 4 data 424 425 426 427 428 429 42a 42b 42c 42d 42e 42f 420 f1d f1d f1d
```

data format capchan (two greycode counters every third write seen)

```
buckeye 1
0 blk 7 data 20 33 37 14 16 11 01 06 04 27 23 30 32 35 15 12
1 blk 7 data 03 07 24 26 21 31 36 34 17 13 00 02 05 25 22 20
2 blk 7 data 37 14 16 11 01 06 04 27 23 30 32 35 15 12 10 03
3 blk 5 data 34 17 13 00 02 05 25 22 20 33 37 14 16 11 01 06
4 blk 5 data 27 23 30 32 35 15 12 10 03 07 24 26 21 31 36 34
5 blk 5 data 13 00 02 05 25 22 20 33 37 14 16 11 01 06 04 27
6 blk 5 data 30 32 35 15 12 10 03 07 24 26 21 31 36 34 17 13
7 blk 5 data 02 05 25 22 20 33 37 14 16 11 01 06 04 27 23 30
8 blk 5 data 35 15 12 10 03 07 24 26 21 31 36 34 17 13 00 02
9 blk 5 data 25 22 20 33 37 14 16 11 01 06 04 27 23 30 32 35
10 blk 5 data 12 10 03 07 24 26 21 31 36 34 17 13 00 02 05 25
11 blk 4 data 01 06 04 27 23 30 32 35 15 12 10 03 07 24 26 21
12 blk 4 data 36 34 17 13 00 02 05 25 22 20 33 37 14 16 11 01
13 blk 4 data 04 27 23 30 32 35 15 12 10 03 07 24 26 21 31 36
14 blk 4 data 17 13 00 02 05 25 22 20 33 37 14 16 11 01 06 04
15 blk 4 data 23 30 32 35 15 12 10 03 07 24 26 21 31 36 34 17
```

Write error 2

```
0 0 10.85 cnt 51 somerrcnt 5 errcap 0 dduerr 0 wrerr2 1 wrerr 0 rrerr 0 lev 0 cnfig 249111 0 ddu 3140
*** werr2 0 0 10.85 cnt 51
```

Configuration Error – 249111 configuration bits with 5 bad

```
0 0 14.08 cnt 100 somerrcnt 5 errcap 0 dduerr 0 wrerr2 0 wrerr 0 rrerr 0 lev 0 cnfig 249111 5 ddu 3140
```