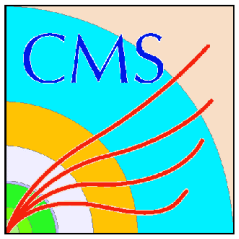

MUON Cathode
FE Electronics

The Ohio State University

CPLD FPGA Test

Code: /home/fast/fastdaq/daqmb-new2.8/utils/rad_test5.c

Running: 1. select CPLD run test
2. write down time for run start
3. monitor current for latchup

This program is identical to the SCAM program but the interpretation is obviously different. Configuration is checked for the CPLD and on reprogramming only the CPLD is reprogrammed. CPLD's take a very long time to program so the proton flux should be chosen accordingly. Note: after reading out the CPLD it is necessary to do a global reset and ddu reset before pulsing and reading out the system. That is why so many global resets are seen.

Output:

/home/fast/data/tmp_files/cpldMMDD_HH:MM.dat