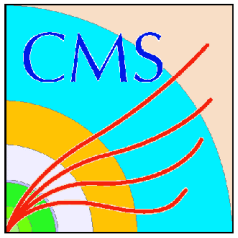

MUON Cathode
FE Electronics

The Ohio State University

Channel Link Test

Code: /home/fast/chanlnk/chanlnk.c (*make chanlnk* to compile)

Running: 1. type chanlnk
2. write down time for run start
3. monitor current for latchup

Connections:

The board requires 3V and 5V supply (marked on voltage cable). The TTL JTAG cable is the only other required connection. The switches on the board should be set to DDDUDUUU (0-7) for proper operation. The push button resets the FPGA program.

Irradiation:

Since the LVDS and Channel Link chips are nearly back to back on the board they will obviously be irradiated at the same time. We should first irradiate the transmitter chips. If all goes well we can then irradiate the receiver chips. Replacement chips are provided in case one burns out a chip.

Test : digital : (1:1)

Randomly generated data is shifted through the cable at 40 MHz. Both Channel Link and LVDS transmitter/receivers are tested. Comparison of transmitted and received signals is done inside the FPGA. An error counter separately counts the number of channel link and LVDS errors recorded.

Monitor:

If no errors are recorded the program will write out a summary every 10000 JTAG reads. If an error is recorded it will print out *** err before the output. The channel link takes 10 msec for its phase- lock loop to recover. In this time the program may output several errors for the same SEU. This is just a crude method of checking the phase-lock loop recovery. If the SEU lasts for more than 10 msecs there is definitely something wrong !

Output:

/home/fast/chanlnk/data/chanlnkMMDD_HH:MM.dat

Format:

/home/fast/chanlnk/data/chanlnkMMDD_HH:MM.dat

```
*** err 5 0 0 2.180000 errs 1 schan 1 slvds 1 lvds 00 chan 00 clko 3
clk1 4

      format: nevt hrs mins secs errs …

      schan, slvds  - status flags for channel link conductors and lvds
                      conductors. If these are not set to 1 basic cable
                      connections are not present.
      lvds,chan -     error counters for lvds and channel link errors
                      respectively
      clk0,clk1 -     counters attached to the input clock and the
                      channel link clock which has passed through the
                      cable. These should equal if the clocks are in
                      phase.
```