

Dan: Coordinate with DDU and DCC design to avoid vias for Gigabit signals

Be careful about the TX, RX definition. For now, the TX means from DCC to DDU, RX means from DDU to DCC

D785H

CMS CSC DDU, DCC P3 Backplane Schematics

Version 1

MBRD_BLK

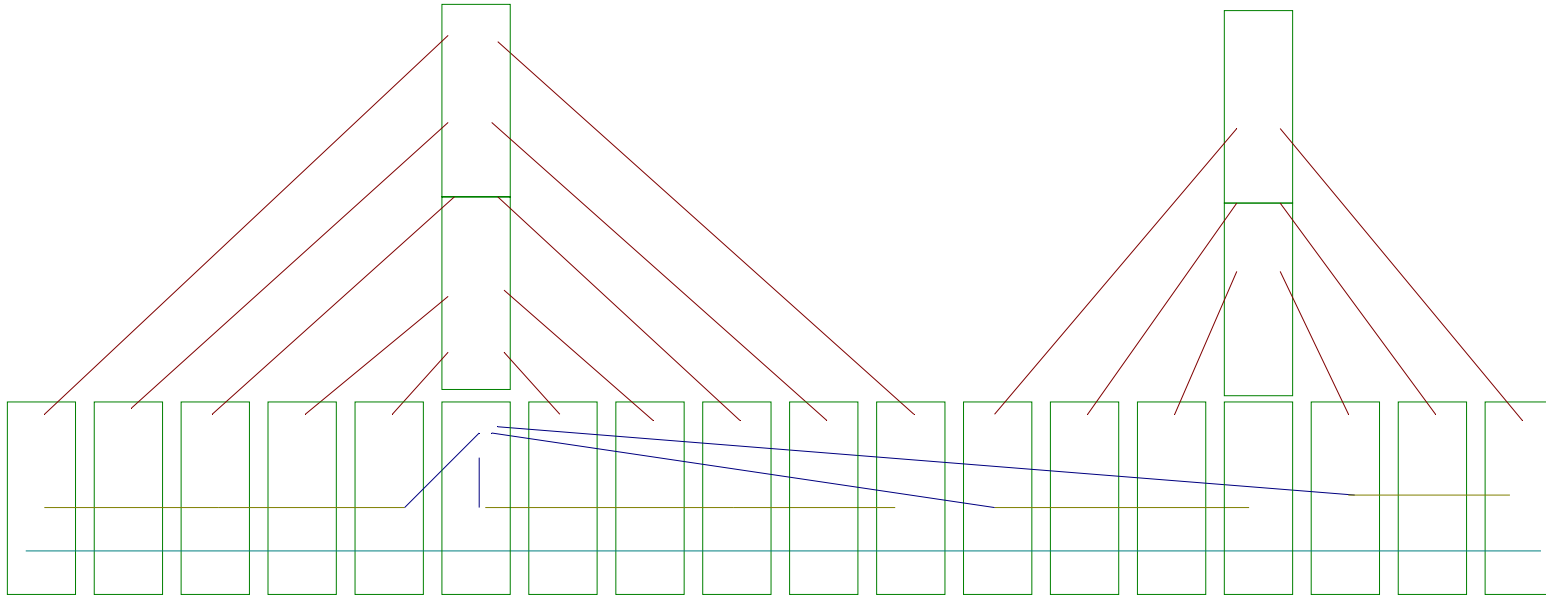
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THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

DCCBP: The DDU/ DCC crate custom backplane design

The First 11 slots are used for 9 --> 1, 4/5 --> 1 configuration,
All the slots are used for 2/3 --> 1 configuration

July 30, 2003: Initial design

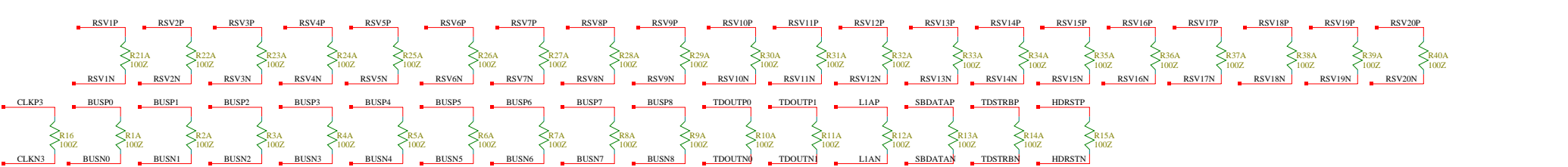
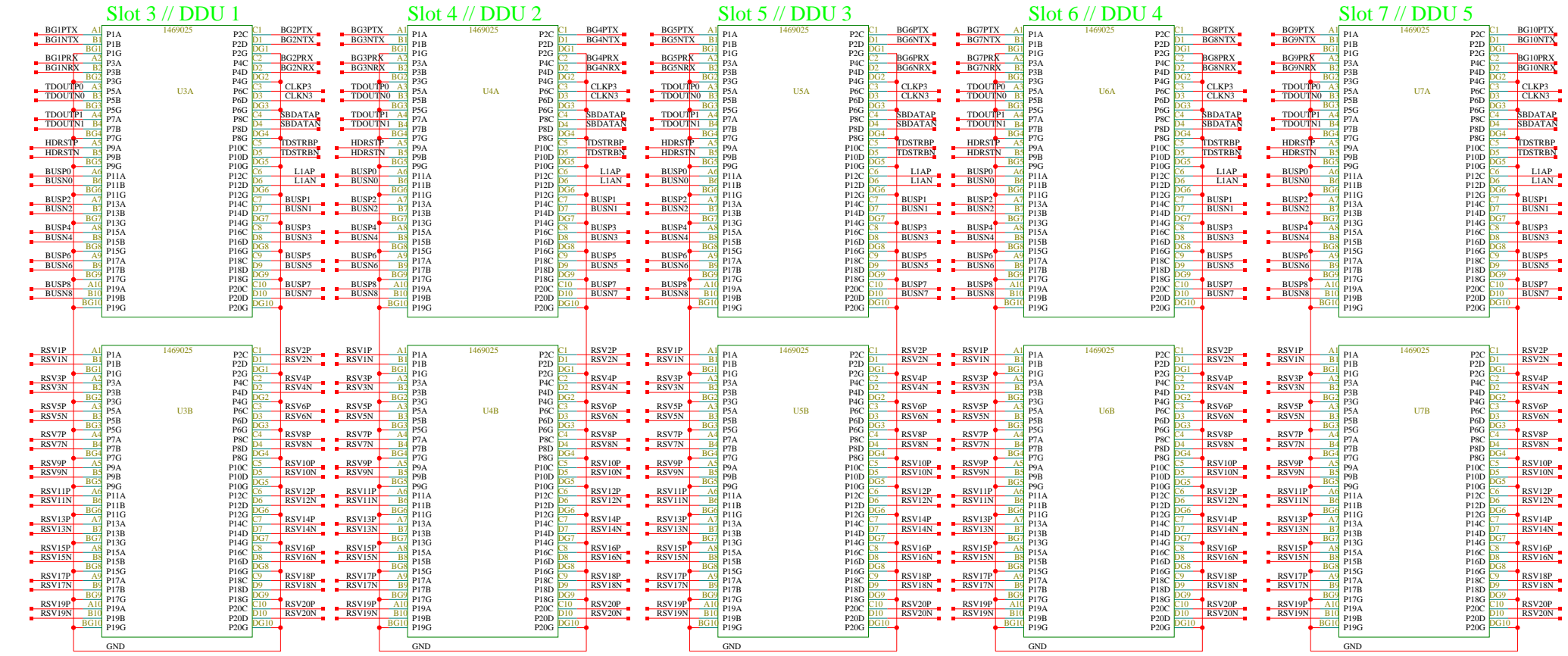
Aug. 8, 2003: Change the pin out on the connectors



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Slot# 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
 Board C
 D D D D D D D D D D D D D D D D D D D
 T D D D D D C D D D D D D D D D C D D D
 R U U U U U C U U U U U U U U U C U U U
 L

The bus signals are terminated on both ends of the backplane with 100 Ohm
 The clock signals are terminated on this Slot 8 DCC and the backplane
 clock3: slot 3, 4, 5, 6, 7



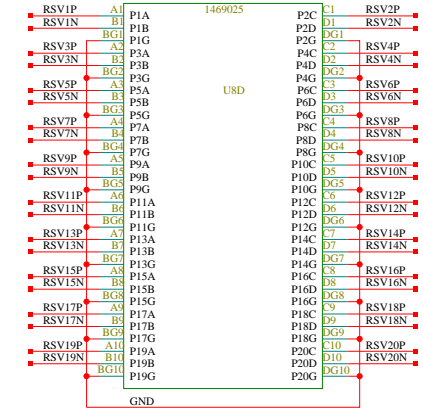
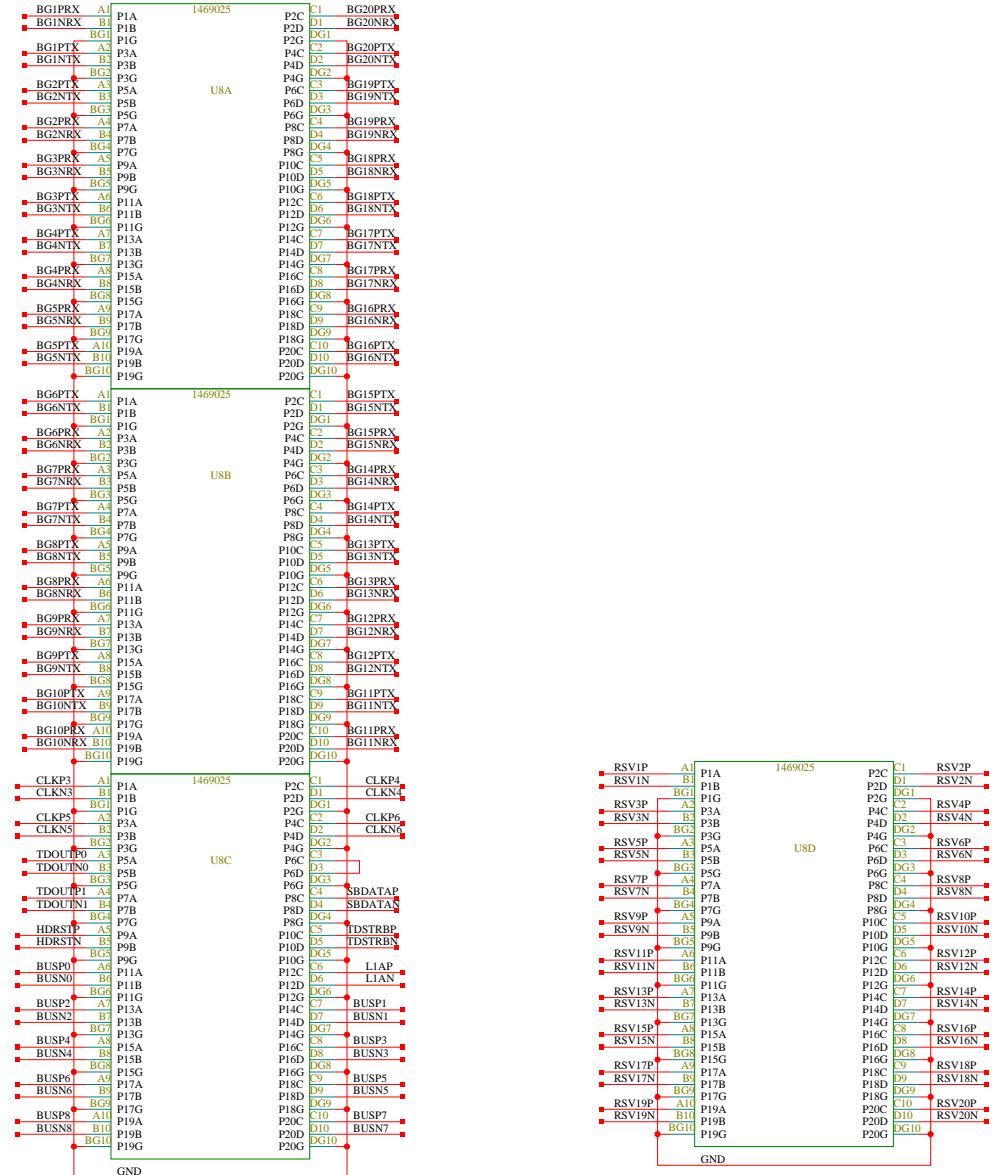
BAP and BAN is connected, SENSEOUT will be high to indicate active DCC

The bus signals are terminated on both ends of the backplane with 100 Ohm

The clock signals are terminated on this board and the backplane, except the passive DCC slot
 clock3: slot 3,4,5,6,7; clock5: 8,9,10,11,12,13; clock6: 14,15,16,17; clock4: 18,19,20
 (clock 8 is the active DCC, clock 17 is the passive DCC)

Need add the Clock terminator on the DCC

Slot 8 // DCC 1



Slot#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
Board	C	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
T	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
R	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
L	U	U	U	U	U	U	U	C	U	U	U	U	U	U	U	U	U	C	U	U	U	

The bus signals are terminated on both ends of the backplane with 100 Ohm

The clock signals are terminated on this Slot 8 DCC and the backplane

clock6: slot 9, 10, 11, 12; clock4: 13, 14, 15, 16

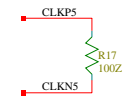
Slot 9 // DDU 6

Slot 10 // DDU 7

Slot 11 // DDU 8

Slot 12 // DDU 9

Slot 13 // DDU 10



Slot#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
Board	C	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	T	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	R	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	L	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

The bus signals are terminated on both ends of the backplane with 100 Ohm
The clock signals are terminated on this Slot 8 DCC and the backplane
clock6: slot 14, 15, 16, 17

Slot 14 // DDU 11

Slot 15 // DDU 12

Slot 16 // DDU 13

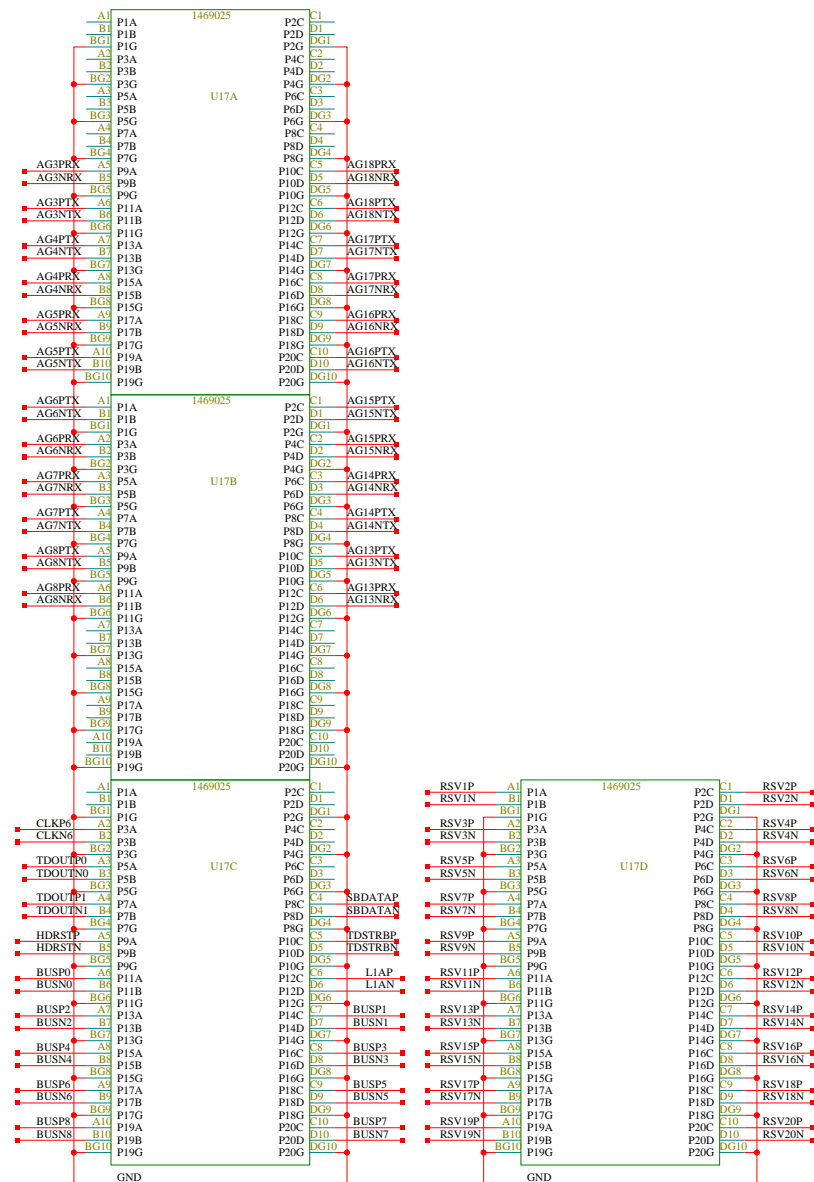


Slot 17 // DCC 2

BAP and BAN is open, SENSEOUT will be low to indicate passive DCC

The bus signals are terminated on both ends of the backplane with 100 Ohm

The clock signals are terminated on this board and the backplane, except the passive DCC slot
 clock3: slot 3,4,5,6,7; clock5: 8,9,10,11,12,13; clock6: 14,15,16,17; clock4: 18,19,20
 (clock 8 is the active DCC, clock 17 is the passive DCC)



Use the CLK5 termination on the passive DCC for active DCC CLK6 termination

