Results of Radiation Test of the Cathode Front-end Board for CMS Endcap Muon Chambers

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Abstract

After a brief overview of the CMS EMU electronics system, results on radiation induced Single Event Effects, TID and Displacement Effects will be reported. These results are obtained by irradiating the components on electronics boards with 63 MeV protons and 1 MeV neutrons. During the proton irradiation, the electronics board was fully under power, all components on the board were active and the data was readout in the same way as designed for CMS. No deterioration of analog performance for each the three CMOS ASIC's on the tested board was observed, up to a dose of 10 kRads. Each of the tested FPGA's survived beyond the dose of 30 kRads. No Single Event Latch-up (SEL) was detected for the CMOS ASIC's up to a proton fluence of 2 x 10^{12} per cm^2. Single Event Upsets (SEU) in FPGA's were detected and their cross sections measured. SEU mitigation with triple module redundancy and voting was implemented and tested.

I. Introduction

The CMS Endcap Muon (EMU) system [1] uses Cathode Strip Chambers (CSC's). Each CSC module is trapezoidal in shape and consists of 6-layers. A CSC layer is basically a MWPC with one of the two cathode planes segmented into strips. The CSC modules are arranged to form vertical disks (called stations) and they are oriented so that the anode wires are in the azimuthal direction and the cathode strips are in the radial direction. Charged tracks are bent by the endcap yoke magnetic field in the azimuthal direction. The precise measurement of the azimuthal coordinate of a hit is achieved by interpolation of charges induced on neighboring cathode strips.

The CSC electronics performs two main functions: 1) to acquire precise muon position and timing information for offline analysis; and 2) to generate muon trigger primitives for the Level-1 trigger system. The electronics system [2] consists of boards mounted directly on the chambers as well boards located in VME crates around the peripheral of the iron disks.

This paper reports the results of radiation tests performed on the Cathode Front-End Board (CFEB), one of the on-chamber boards. In section II we briefly describe the architecture and functions of the CFEB. The expected radiation environment in the endcap region and our radiation test plan are discussed in Sections III and IV. Results will be given in section V and a short conclusion in the last section.

II. The Cathode Front-end Board (CFEB)

The CFEB [2] consists of 96 input channels per board. Each front-end board is designed to read out a section of the chamber 16 strips wide by 6 layers deep. Figure 1 shows the top side of the CFEB-99 prototype. The main active components on the board are listed in Table 1.

The input signals from each of the strips are sent into 16-channel amplifier-shaper ASIC's (There are six such ASIC's on the CFEB, three on the top side and three on the bottom side of the board). Each input signal is amplified and shaped into voltage pulses. The output of the shaper is sampled every 50 ns and held in Switch Capacitor Arrays (SCA ASIC's) during the Level-1 trigger latency. The SCA write- and read- addresses are generated by the readout control FPGA on the CFEB. When trigger conditions are satisfied, the stored voltage samples are digitised, multiplexed and sent by cable to the DAQ system.

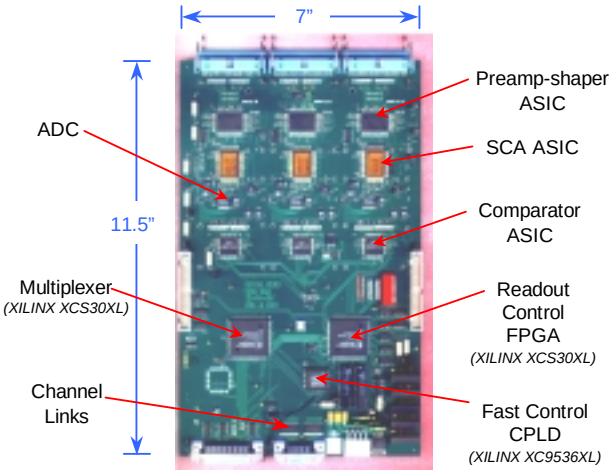

Figure 1: The CSC Cathode Front-end Board Prototype CFEB-99

Another output of the shaper is connected to the trigger path whose main component is a Comparator ASIC. The comparator ASIC locates the centroids of the strip charge

clusters in each chamber layer to an accuracy of half the strip width and marks its time. The resulting information is sent via cable to an off-chamber trigger board for trigger primitive generation.

Table 1: Active components on the cathode front-end board.

Component Type	***Number per board***
Preamp-Shaper (16 ch ASIC)	6
SCA (16 ch ASIC)	6
Comparator (16 ch ASIC)	6
ADC (12 bits, 20 MHz)	6
Readout Controller FPGA	1
Multiplexer FPGA	1
Fast Control CPLD	1

III. EMU RADIATION LEVELS

One of the primary requirements for EMU electronics boards is that they must be able to withstand the LHC radiation environment. The inner most CSC's (ME1/1 chambers) are subjected to the highest radiation levels. For electronics located on these chambers, calculated [3] neutron fluence above 100 KeV is $6x10^{11}$ cm^{-2} (Figure 2) and Total Ionisation Dosage (TID) is 1.8 kRad, integrated over 10 LHC years ($5x10^{7}$s) at the designed luminosity of $10^{34}cm^{2}s^{-1}$. The energy spectrum of the neutrons, shown in figure 3 for ME1/1, is essentially flat and cuts off at about 1 GeV. The neutron energy spectra for other EMU chambers have approximately the same shape.

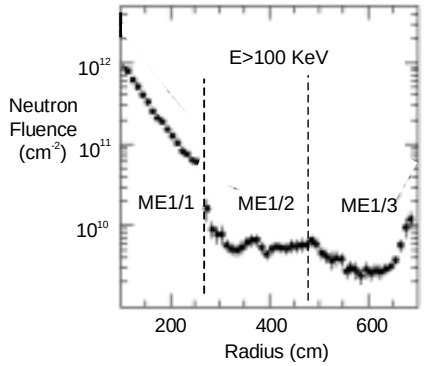

Figure 2: Neutron Fluence (for 10 LHC year) in CSC station 1.

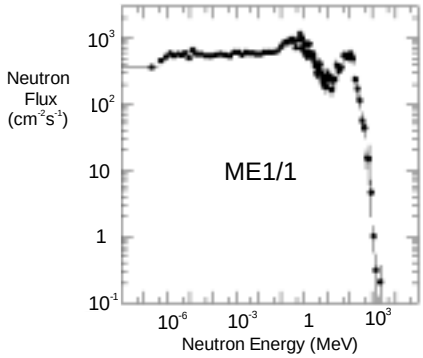

Figure 3: Neutron energy spectrum for the inner most CSC.

IV. RADIATION TEST PLAN

Radiation effects on micro-electronics circuits fall into two categories: cumulative effects and Single Event Effects (SEE).

Cumulative effects are caused by exposure to both ionising radiation (TID) and to neutrons (Displacement damage). TID can affect CMOS as well as bipolar devices while displacement damage affects only bipolar or biCMOS devices. Both TID and Displacement damage degrade the analog performance of the chip. They could lead to chip failure if the dosages are sufficiently high.

SEE's are caused by nuclear reaction of charged hadrons and neutrons. Heavy ions produced in a hadronic reaction can pass through sensitive regions of a chip, causing destructive or hard errors like Single Event Latch-ups (SEL) or static errors such as Single Event Upsets (SEU). An SEL is due to radiation-induced turn-on of parasitic transistors in a CMOS chip. When latch-up occurs, the chip symptomatically draws a large current and it can fail if power is not turned off quickly. An SEU is due to an upset in the content of a memory cell in the chip. SEU's can interrupt logic functions of an FPGA, for example. SEU's are usually recoverable by rewrites or by recycling the power.

Since the same cathode front-end board will be used for all the CSC's in the EMU system, all the ASIC's and COTS (Componets Off-The-Shelf) on the CFEB must be able to tolerate the worst case neutron fluence and ionisation dosage mentioned in the previous section. To take into account the uncertainties in the calculation, the tolerance of the CFEB will be tested up to three times the calculated levels.

The goals of the radiation tests are thus the following:

- Measure the cross sections for Single Event Effects (SEU and SEL). Use the measurements to predict SEE rates for neutron fluence of $2x10^{12}$ cm^{-2}.
- Measure the degradation of analog performances of ASIC's due to TID effects up to a dose of 5-10 kRads.
- Measure degradation of analog performance due to displacement damage of bipolar or biCMOS devices for a neutron fluence of $2x10^{12}$ cm^{-2}.

Modelling and calculations done by Huhtinen and Faccio [4] show that in the LHC radiation environment, SEU's are caused primarily by high energy (>20 MeV) hadrons. They also showed that at these energies the SEU cross section is approximately independent of particle type and energy. Therefore, our approach, summarized in Table 2, is to test CMOS devices for SEU, SEL TID effects with a 63 MeV proton beam (at UC Davis) and test bipolar devices with 1 MeV neutrons from a reactor (at The Ohio State University).

Table 2: Radiation Test Plan

	63 MeV Protons	***1 MeV Neutrons***
CMOS devices	SEU, SEL, TID	
Bipolar devices	SEU, SEL, TID	Displacement

V. Results

A. Proton Irradiation Tests of CFEB-99

The tests were carried out using 63 MeV Proton beams at the UC Davis cyclotron facility. During the irradiation, the CFEB-99 prototype board is positioned perpendicular to the proton beam and the beam is collimated to irradiate only one ASIC or COTS at a time. The beam profile is approximately flat over the aperture (adjustable up to 50mm x 50mm). The CFEB-99 board is under power and the test data is read out via an 8 m cable into the DAQ Motherboard that transmits the data by optical links to a PC interface board plugged into the PCI bus of a PC. This readout set up is close to that for the final EMU electronics system. The test results are summarized below.

1) *Preamplifier-shaper ASIC*

The preamplifier-shaper (Buckeye) ASIC is a 0.8 μm CMOS chip with linear capacitors manufactured by AMI. It was irradiated with a proton fluence of 2.28 x 10^{12} cm^{-2} for a total time of about 2 hours. The corresponding TID is 300 kRad. **No SEL was observed.** There were no shift register errors. **No change in amplifier-shaper noise was observed from 0-30 kRad** (see Figure 4 and Footnote 1). The gain of the ASIC for each of the 16 channels was observed to decrease with dose (Figure 5). Self-annealing - recovery of the amplifier gain when the chip is not under irradiation - was observed. For a dose of 5 kRads, the decrease in gain is small. Furthermore, this dosage was reached in less than 2 minutes during the test, while in CMS the same dosage would be cumulated over 10 LHC-years. Therefore with self-annealing, the decrease in gain is completely negligible in the LHC environment.

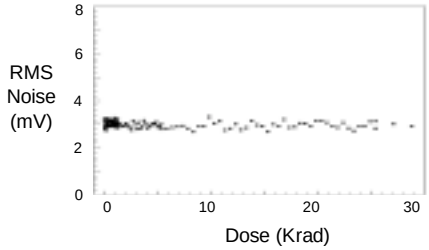

Figure 4: Noise of the Buckeye ASIC versus dose.

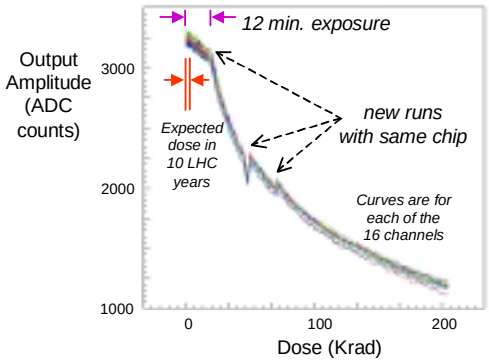

Figure 5: Gain of the amplifier-shaper ASIC versus dose.

2) *Switched Capacitor Array (SCA) ASIC*

The SCA ASIC is also a 0.8 μm CMOS chip with linear capacitors manufactured by AMI. The chip was irradiated with a total proton fluence of 1.7 x 10^{12} cm^{-2} in two runs, each lasting about an hour**. No SEL was observed. There was negligible change in noise and cell pedestals.** During the irradiation, test input pulses were sampled, stored in the SCA and then digitised.

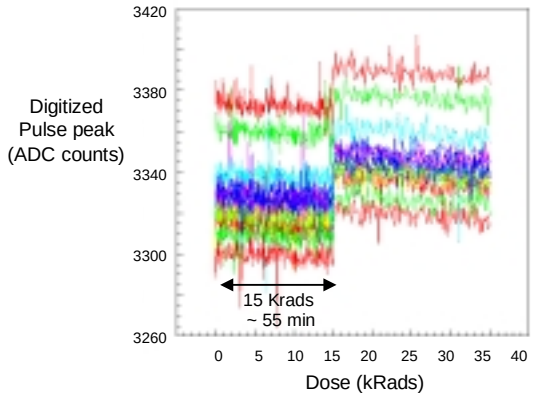

Figure 6: Performance of the SCA ASIC versus dose.

Figure 6 shows the digitised pulse peak versus dosage for each of the 16 channels. The small decrease over dose is due to the output amplifier gain drop. With self-annealing this is also not a problem at LHC rates.

3) *ADC (Analog Device 9225, 12 bit, 20 MHz)*

The ADC was irradiated with a proton fluence of 2.7 x 10^{12} cm^{-2}. No SEL was observed. No degradation of the ADC performance was observed up to 35 kRad.

4) *Comparator ASIC*

The comparator ASIC is manufactured by Alcatel-Mietec using 0.7 μm n-well technology. The chip was irradiated with a proton fluence of 1.1 x 10^{12} cm^{-2}. **No SEL was observed.** The changes in discriminator threshold and in comparator offsets for each of the 16 channels were measured as a function of dose, as shown in Figure 7. These changes are within ± 0.4 mV from 0 – 15 kRads, not large enough to affect the performance of the ASIC.

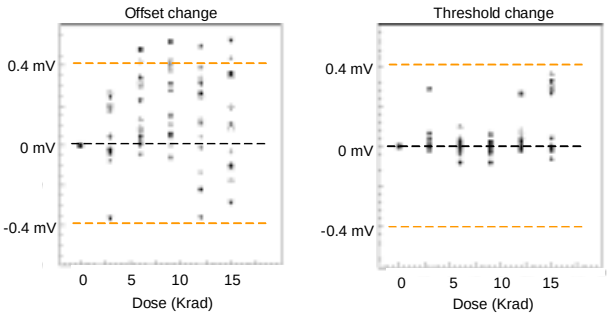

Figure 7: Changes in discriminator thresholds and comparator offsets versus radiation dose.

5) Readout Control FPGA (XLINX Spartan XCS30XL)

The readout controller was irradiated with a total of 9.9 x 10^{10} cm^{-2} of protons (TID=13.4 kRads) in two runs. **No SEL was observed.** During the irradiation, the SCA read/write addresses generated by the controller were read back and checked against predictions. A total of 27 SEU's were detected. SEU's interrupt the functioning of the FPGA. Once an SEU occurs, the FPGA must be reloaded to recover from the error. The above measurement gives an **SEU cross section** of **$2.7 \times 10^{-10} cm^2$**. Configuration memory errors were independently measured. We found that only 6% of the configuration memory errors generate real SEU's, while 30% of the detected SEU's had no accompanying configuration memory error.

6) Multiplexer FPGA (XLINX Spartan XCS30XL)

The multiplexer was irradiated with a total of 2.9 x 10^{11} cm^{-2} of protons (TID=38.1 kRads) in six runs. **No SEL was observed**. During the irradiation, a total of 27 SEU's were detected, corresponding to an **SEU cross section** of **$1.2 \times 10^{-10} cm^2$**. All SEU's are recoverable by reloading the FPGA. Additional configuration memory errors are also observed, but they do not affect the operation of the chip.

7) Fast Control CPLD (XILINX XC9536XL)

The CPLD generates SCA sampling clock as well as ADC clock. It also provides controls to the multiplexer. Two CPLD chips were tested. Chip #1 was irradiated with a proton fluence of 2.8 x 10^{11} cm^{-2} (TID=37.8 kRads) and chip #2 with fluence of 3.1 x 10^{11} cm^{-2} (TID=41.3 kRads). **No SEL was observed for either chips**. During the irradiation, a total of 106 SEU's were detected for chip #1 and 117 SEU's were detected for chip #2. The two sets of data were consistent with each other, yielding an **SEU cross section** of **$3.8 \times 10^{-10} cm^2$**. All SEU's are recoverable by reloading the CPLD.

8) LVDS Driver (SN90LV031), Receiver (SN90LV032)

Both are CMOS devices. Each chip was irradiated with 10 kRads of protons. No error was detected.

B. Proton Irradiation Tests of CFEB-00

The total SEU cross section per board measured for CFEB-99 is 7.7 x 10^{-10} cm^2, corresponding to a worst case SEU rate of 10^{-5} per second ($7.7 \times 10^{-10} cm^2$ x 2×10^{12} n's cm^{-2} / 5×10^7 s) or 1 SEU per CFEB in about 30 hours. This is not a small rate, since there are over 2000 CFEB's in the whole detector, about 500 of these are on the ME1/1 chambers.

To reduce the SEU rate per board, a new prototype CFEB was built (CFEB-00) which uses only one FPGA (XILINX Virtex XCV50). All the functions previously performed by the two XILINX Spartan FPGA's and by the CPLD were consolidated and programmed into the XILINX Virtex chip on the CFEB-00. For SEU mitigation, triple module redundancy with voting was implemented for key functions of the chip. The CFEB-00 was radiation tested with protons. The results of new components tested are summarized below.

1) Controller-Multiplexer (XILINX Virtex XCV50)

The chip received a total of 9.9 x 10^{10} cm^{-2} of protons (TID=12.5 kRads) in six runs. **No SEL was observed.** During the irradiation, total of 16 SEU's were detected, corresponding to an **SEU cross section** of **$1.7 \times 10^{-10} cm^2$**. All SEU's are recoverable by reloading the FPGA. The SEU rate per board is a factor of 4.5 lower than that on CFEB-99. The SEU measurements for the various FPGA's are summarized in Table 3.

2) ISPROM (XILINX XC1802)

The ISPROM is used on the CFEB to reload FPGA. It is important to test their radiation tolerance. Two chips were irradiated. Chip #1 received 1.92×10^{11} p/cm^2 (TID=26.1 kRads); chip #2 received 0.84×10^{11} p/cm^2 (TID =11.3 kRads). There were two SEU's observed for chip #1 and 1 SEU observed for chip #2. None of the three errors were related to the chip memory. During the last 30% of exposure read back errors were observed on the ISPROM yet the ISPROM loaded the Virtex FPGA properly and the FPGA showed no memory errors.

3) Logic Device – AND/OR gates (74HC58)

This CMOS chip was irradiated with 10 kRads of protons and showed no errors.

Table 3: Measured SEU Cross Sections for various XILINX FPGA's

Device (Function)	Proton Fluence (10^{11} cm^{-2})	Dosage (kRad)	Number of SEU's	SEU Xection (10^{-10} cm^2)
XILINX Spartan XCS30XL (Readout Control)	1.0	13.4	27	2.7
XILINX Spartan XCS30XL (MUX)	2.9	38.1	34	1.2
XILINX CPLD XC9536XL	5.9	79.1	223	3.8
XILINX Virtex XCV50 (Readout Control & MUX)	0.9	12.5	16	1.7

C. Proton Irradiation of Other Components

1) Channel Links

Channel links were radiation tested using a home made test board. The board consists of a transmitter and a receiver channel link pair plus an FPGA. Randomly generated data is shifted through a short cable at 40 MHz. Comparison of the transmitted and received data is done inside the FPGA. The transmitter and receiver were each irradiated with 1.48 x 10^{12} protons per cm^2 (TID=200 kRads). There were 277 SEU's for the receiver and 1023 SEU's for the transmitter. The SEU's correspond to bit errors in the data. Extrapolate to 10 LHC year operation, the radiation induced bit errors in the data is a negligible fraction of the total data bits transmitted.

2) CMOS Output Current OpAmp (AD8591)

This is a CMOS device. It is used to generate +2.5 V for the Virtex chip. The chip showed no degradation after receiving 10 kRads of proton irradiation.

3) Other Miscellaneous Components

The following COTS were each irradiated with 10 kRads of protons. No degradation of their performances were observed.

- CMOS Buffer (IDT74ALT16244)
- Silicon Delay Chips
- Bus Multiplexer (IDT74ALV162268)

D. Neutron Irradiation of Bipolar Devices

The bipolar chips used on the CFEB are voltage regulators, voltage references, current Feedback OpAmps, and diode arrays. These components must be tested for tolerance to displacement damage from low energy neutrons. Tests were done at The Ohio State nuclear reactor with 1 MeV neutrons. Special boards were made to test samples of each of the components. They were each irradiated with a fluence of 2 x 10^{12} neutrons per cm^2. During irradiation, the components were not under power. The functions of the components were checked after they were irradiated. The devices that pass the tests are listed below.

- Adjustable voltage regulator: LM1117-adj
- Voltage reference (2.5V, 5mA) : LM4120-2.5
- Voltage reference (1.8V, 5mA) : LM4120-1.8
- Shunt voltage refernce : LM4041
- Diode array (reverse-biased) : SDA321
- Current Feedback OpAmp: AD8011
- Thermisters

VI. CONCLUSIONS

The cathode front-end board to be used for CMS endcap muon system has been tested for tolerance to 63 MeV protons as well as to 1 MeV neutrons. No deterioration of analog performances for each the three CMOS ASIC's and other CMOS COTS on the CFEB was observed for TID up to 10 kRads. All tested FPGA's survived beyond TID of 30 kRads. No SEL was detected for each of the three ASIC's up to 2 x 10^{12} protons per cm^2. Bipolar devices tolerant to 1 MeV neutron radiation up to $2x10^{12}$ per cm^2 were identified.

The only adverse effects found on the CFEB were SEU's. They occur in the commercially available FPGA's and Channel links. SEU's in Channel Links are not serious problems as they only cause rare data bit errors. However, SEU's induced in FPGA's interrupt their operation. Once an SEU occurs, the FPGA must be reloaded to recover from the error. We measured SEU cross sections for several XILINX FPGA's using 63 MeV protons. The SEU rate per CFEB is reduced significantly by using a single XILINX Virtex FPGA per board implemented with triple module redundancy voting. To recover from radiation induced SEU's in CMS, we plan to periodically reload the FPGA's on all the CFEB's. Based on our SEU cross section measurement, the reloading frequency is estimated to be about once every 20 minutes at peak LHC luminosity. Since the reloading takes only 5 ms, the resulting deadtime is negligible.

We conclude that the CFEB as currently designed is tolerant to the predicted radiation environment in the Endcap Muon region of CMS.

Acknowledgements - We thank our collaborators from UCLA for their assistance in testing the comparator ASIC. The development of the CFEB and the work reported in this paper are supported by the U.S. Department of Energy.

VII. REFERENCES

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3. M. Huhtinen, CMS COTS Workshop, November 1999. Calculation results are posted at the web site http://cmsdoc.cern.ch/~huu/tut1.pdf
4. M. Huhtinen and F. Faccio, Nucl. Instrum. Methods Phys. Res., A : 450 (2000) no.1, pp.155-72

VIII. FOOTNOTES

1. During the proton irradiation test, the CFEB could not be properly grounded and shield. When the CFEB is properly mounted on a CSC and shielded, the noise level is about 1.25 mV instead of the 3 mV shown here.