DAQMBV

CMS CSC DAQ Motherboard VME interface FPGA

VME interface and Slow control

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DAQMB VME interface FPGA Design
This FPGA do the slow control for CFEB and DAQMB by VME --> JTAG, or direct VME command
Modification history:
  Nov. 27, 2000: Modification based on Dan's D741Z design, which convert VME to JTAG, add DAQMB specific functions
  Nov. 29, 2000: Base structure of the Design is ready; Dec. 5, 2000: preliminary design passed APR
  Feb. 2, 2001: Totally new scheme design on m:\wv\cmsdaqmb\daqmbv\ and Spartan-II
  Feb. 28, 2001: Modify to be consistent with new COMMAND scheme
  Apr. 9, 2001: Finished Modification, and pin Allocation according to DAQMB PCB Layout
  Apr. 13, 2001: Ready for DAQMB debugging, 178 IOBs are used
  July 24, 2001: Optimization based on the version1 design.
**Title:** VME Power-on Reset

**Diagram Description:**

- **Command Decoder**
  - **DAQMB VME Interface**
  - CMS CSC Electronics

- **Gaps:**
  - Fastclk is in phase with Midclk, but they are not in phase with Slowclk.
  - PROMs and ADCs use Slowclk, Virtex-E and DAC use Midclk.

**Clocks:**
- **Fastclk:** 40MHz
- **Midclk:** 10MHz
- **Slowclk:** 2.5MHz
- **Slowclk2:** 1.25MHz

**Notes:**
- Fastclk is in phase with Midclk, but they are not in phase with Slowclk.
- PROMs and ADCs use Slowclk.
- Virtex-E and DAC use Midclk.
CFEB JTAG Clock: 1.25MHz, which is controlled by ENABLE.
The DAC can work at 10MHz, FPGA can work at 33MHz, PROM can work at 10MHz, but it can only be Re-programmed at about 1.25MHz.
The guess number for BUCKEYE is 5MHz.
DAQMB Controller FPGA JTAG Clock: 10MHz, which is synchronized with MIDCLK
The FPGA can work at 33MHz, the Serial Flash Memory can work at 20MHz
DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK
The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz
The ISP does not work at 2.5MHz or faster

Both FPGA and CPLD will drive VPROM's JTAG line, tri-state when not in use
Serial ADC (MAX1270/1271) Interface clock: 1.25MHz, Divided SLOWCLOCK is used
The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz
Serial DAC (MAX5154/5155) interface clock: 5MHz
The MAX 5154/5155 requires the minimum clock period is 100ns.
Device Selection

Device code:

- 05 | VME Interface FPGA
- 01 | CFEB JTAG
- 02 | DAQMB Controller FPGA JTAG
- 03 | DAQMB Controller PROM JTAG
- 04 | VME Interface PROM JTAG
- 05 | Dual DAC for Calibration
- 06 | FIFO Read/Write
- 07 | DAQMB ADC Interface
- 08 | Low Voltage Monitoring Interface
- 0F | Emergency PROM Programming, Reserved for Emergency CPLD

Device Selection Diagram
CFEB Selection and Readback logic

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CFEBs JTAG control
DAQMB VME Interface
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GU 2A
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DAQMBV 20C
CFEB JTAG commands:

- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register
- 08 || Write CFEB Select Register
- 09 || Read CFEB Select Register
This OR gate may generate GLITCH

DTACK for Load Instruction/Data Register command
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Controller FPGA JTAG Control
DAQMB VME Interface
CMS CSC Electronics

GU 2B

30B
CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register
CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register
DTACK for Load Instruction/Data Register command
CFEB JTAG command decode

CFEB JTAG commands:
- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register
DTACK for Load Instruction/Data Register command
Burr-Brown ADS7809, or Analog Devices AD977 interface logic

Procedure: Pull BBCONV low for 400ns after VME command, then go back high. Disable the counter
After ADC BUSY go low to high, send another BBCONV low for 400ns, and enable the counter
At same time disable the BUSYSHOT. After 16 Clock cycles, set DTACK low to indicate Data Ready
Reset the DTACK after VME Address changed, the BB Read cycle ends
Serial ADC Selection and Readback Logic
Serial ADC Command Decoder:
00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 || Read Data Back from Burr-Brown Register
04 ||
05 ||
06 ||
08 || Write Serial ADC Chip Select Register
09 || Read Serial ADC Chip Select Register

CFEB JTAG command decode

Serial ADC Commands decoder
00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 || Read Data Back from Burr-Brown Register
04 ||
05 ||
06 ||
08 || Write Serial ADC Chip Select Register
09 || Read Serial ADC Chip Select Register
FIFO Data-loading path selection, and setting readback
Parallel FIFO Read/Write Command Decoder:

00 | Write to FIFO, 00 for LastWord/Overlap (no last, no overlap)
01 | Write to FIFO, 01 for LastWord/Overlap (last, no overlap)
02 | Write to FIFO, 10 for LastWord/Overlap (no last, overlap)
03 | Write to FIFO, 11 for LastWord/Overlap (last and overlap)
04 | Read low order 16 bits, no FIFO read counter Increment
05 | Read low order 16 bits, and FIFO read counter Increment
06 | Read high order 2 bits, no FIFO read counter Increment
07 | Read high order 2 bits, and FIFO read counter Increment
08 | Write FIFO Select Register, (more than 1 FIFO can be enabled)
09 | Read FIFO Select Register, just to check 08 function
11 | Just Increment FIFO Read Counter
Serial ADC Selection and Readback Logic

ADC Selection and Readback
DAQMB VME Interface
CMS CSC Electronics
Serial ADC Command Decoder:

- **00**: Write Control Byte to MAX1271's
- **01**: Read Data Back from 1271 Register
- **02**: 
- **03**: 
- **04**: Write Low Voltage Power Register
- **05**: Read Low Voltage Power Register
- **06**: 
- **07**: 
- **08**: Write Low Voltage Monitoring Serial ADC Chip Select Register
- **09**: Read Low Voltage Monitoring Serial ADC Chip Select Register