DAQMBP

CMS CSC DAQ Motherboard PCB Schematic

REV 4

MBRD_BLK

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210
DAQMB, It check and concentrate the DATA (CFEB, CLCT/TMB/ALCT) from one chamber, and then send to DDU

Oct. 23, 2000: Modify the design based on m:\wv\d741t\rev3\, an intermediary design
Nov. 1, 2000: The new scheme is ready, need update the CCB link, and CLCT/TMB link, and possibly CLCT/TMB FIFO.
Nov. 2, 2000: Preliminary design is ready. Need feedback from Dan, and coordination with UCLA, Rice and FLorida for backplane
Dec. 6, 2000: Double checked the signals by feed backs from FPGA design
Jan. 18, 2001: Modify the ADC design, use three MAX1271, and one ADS7809/AD977
Jan. 22, 2001: Modify the Backplane interface design. For CCB, use GTLP/LVTTL transceiver, TMB, use FPGA GTLP property
Feb. 7, 2001: Modify according to backplane PCB design, Add Flash ram
Feb. 14, 2001: Double check, and modify the VME interface and “emergency” handling
Feb. 26, 2001: Further check, Changed the DAC to MAX5154
Mar. 5, 2001: Add TLK2501/1501 for GLINK, and Changed the Temprature ADC Refs
July 3, 2001: Modifications by the Rev3 PCB debug
Keep Channel Link and buffers close to FIFOs

F1 Input/Output

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip. Shared by the two 16827's.

Three filter CAPs per power pin on Channel Link.

Serial SCAM data

End flag
FEB Error Flag
Usually Overlap

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip. Shared by the two 16827s.
Disable all FIFOs for ~50ns during readout switching?
Set FWFT mode: Sdata HIGH during falling edge of MRST.

Need PULL-DOWNS on:
- Lastword, Eflag, OEN, read_one

Need PULL-UPS on:
- Overlap, rst, f_rst, kill_dav, dav, emptyf*
Keep Channel Link and buffers close to FIFOs

F2 Input/Output

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip.
Keep Channel Link and buffers close to FIFOs

Three filter CAPs per power pin on Channel Link.

Otherwise, one filter CAP per power pin, one TANT per chip.

F3 Input/Output
Keep Channel Link and buffers close to FIFOs

Three filter CAPs per power pin on Channel Link.

F4 Input/Output
Stuff either R67 or R68, but not both
Load R68, BM low, 36 bit in and 36 bit out. (actually, only 18 low-order bits used)
Load R67, BM high, 36 bit in and 18 bit out. The high-order 18-bit go out first, then low-order 18-bit
These are the functions if the LVDB monitor uses 6 ADCs.

Default mode setting
Connect all the signals on this page to FPGA
For pin compatible with different FPGA, use IO** pins
125MHz to match with Gigabit ethernet
NOTE: All high speed serial lines must be smooth, no right angles and no layer changes.
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**TMB[14:0]: CLCT/TMB data to 18-bit fifo**

**TMB[29:15]: Additional CLCT/TMB data to 36-bit fifo**

**TMB30: DDU special word flag**

**TMB31: Last word flag bit**

**TMB32: 40MHz clock to write to FIFO**

**TMB33: Fifo write enable inverted**

Span(7:1) Used to exchange information in CFEB calibration mode