

# FAKEBPC

Fake BackPlane Control FPGA

CMS CSC DAQ

FBPCNTRL

ELECTRONICS LAB  
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## Fake BackPlane Control FPGA

This is the Fake BackPlane Control FPGA design, to simulate CCB and TMB

Jan. 24, 2001: Initial design finished

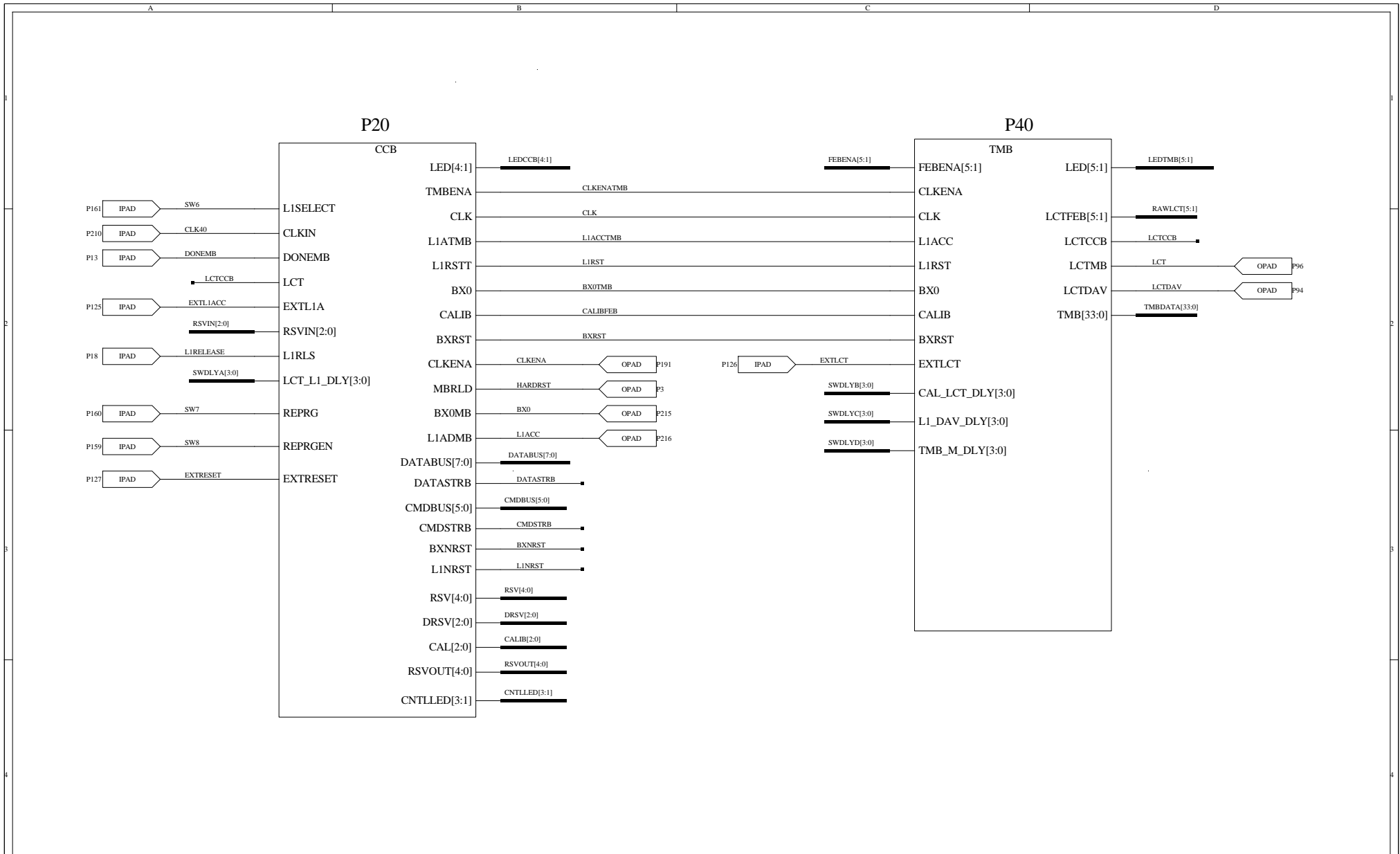
Feb. 22, 2001: Copy the design from M:\WV\D741FBP\FBPFPGA\ here, and modify it according to BackPlane signals

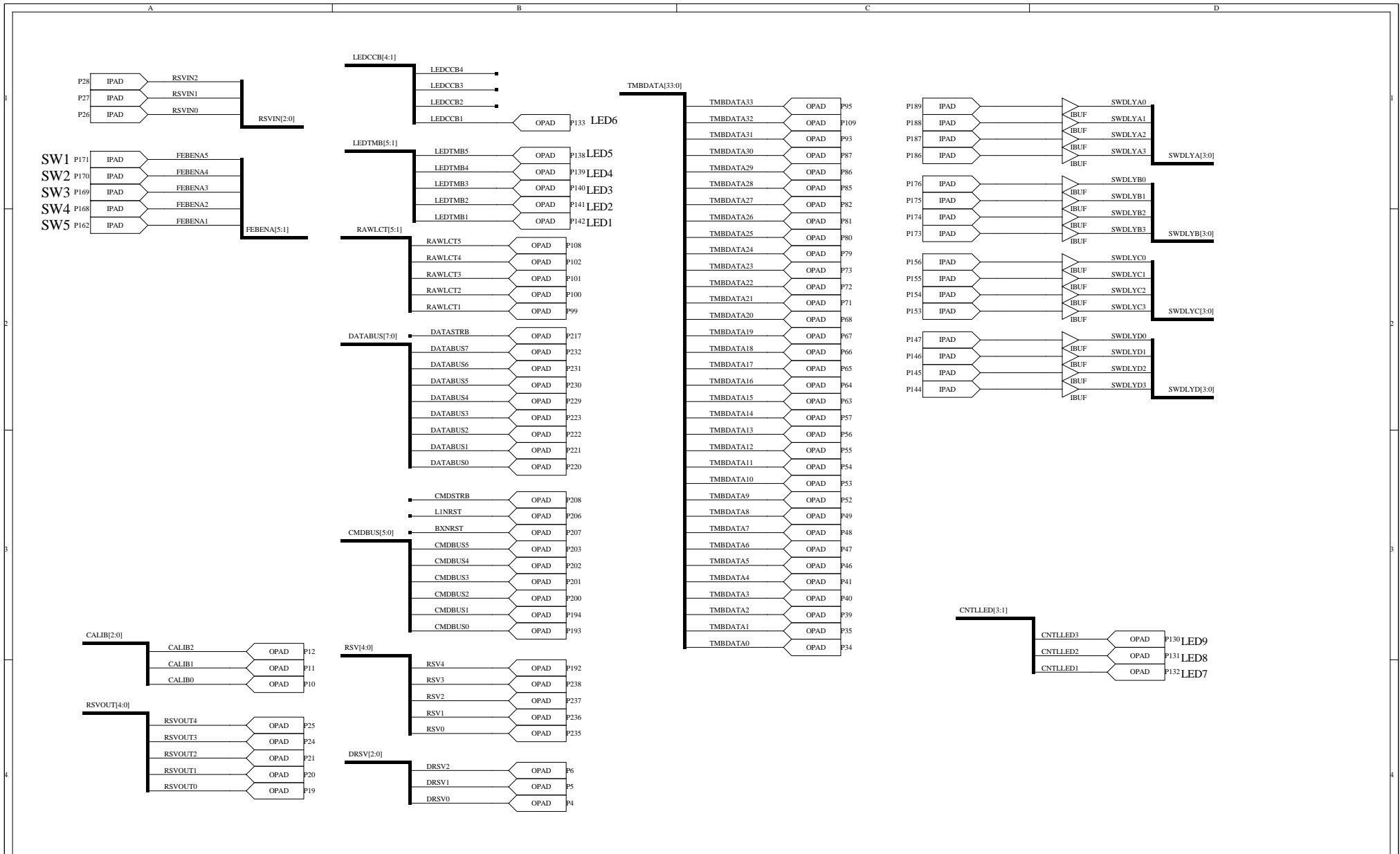
Feb. 27, 2001: Double check the design, and add dummy I/O logic for Reserved Signals

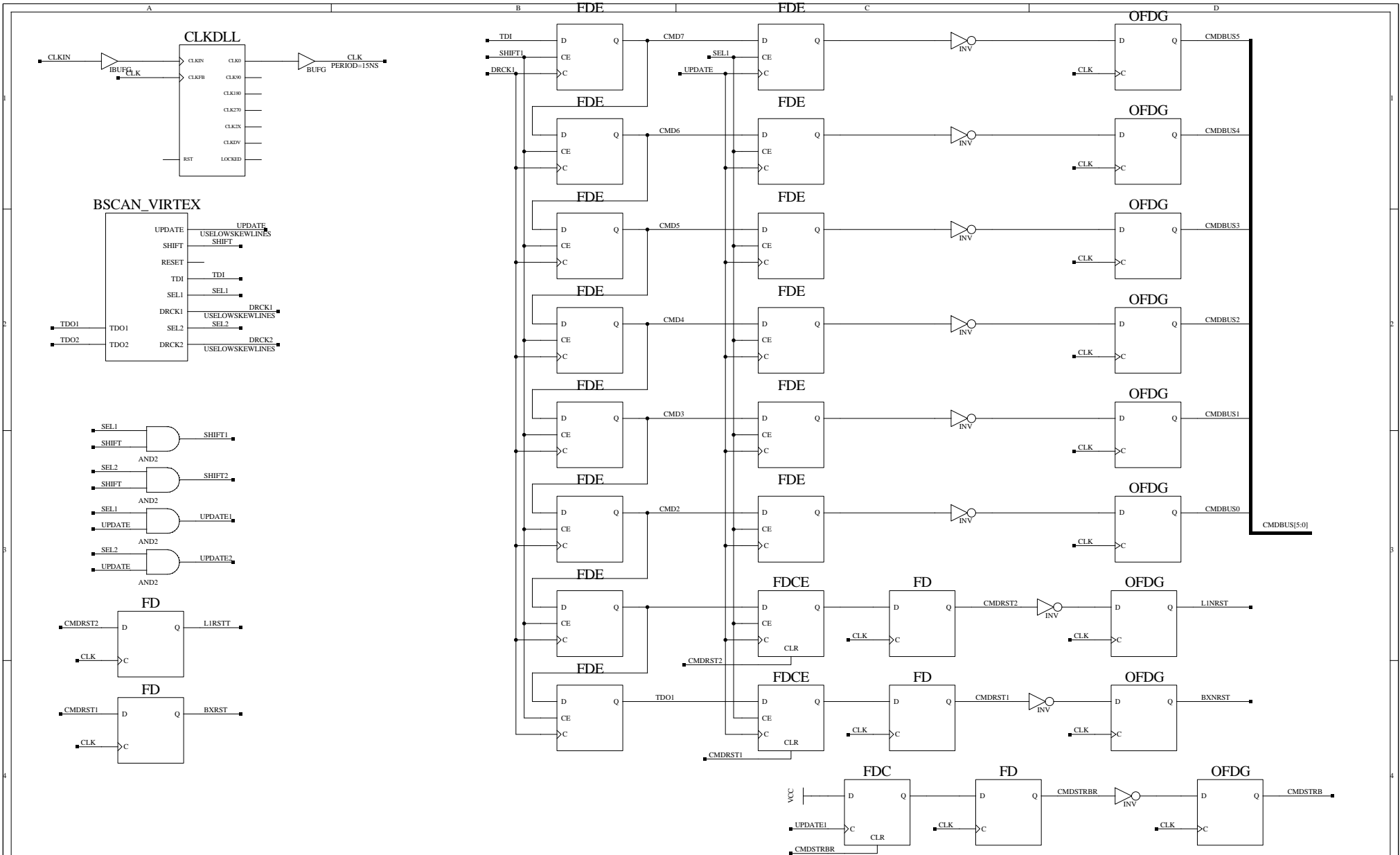
Jan. 16, 2002: Simplify it, and virtually disabled the JTAG

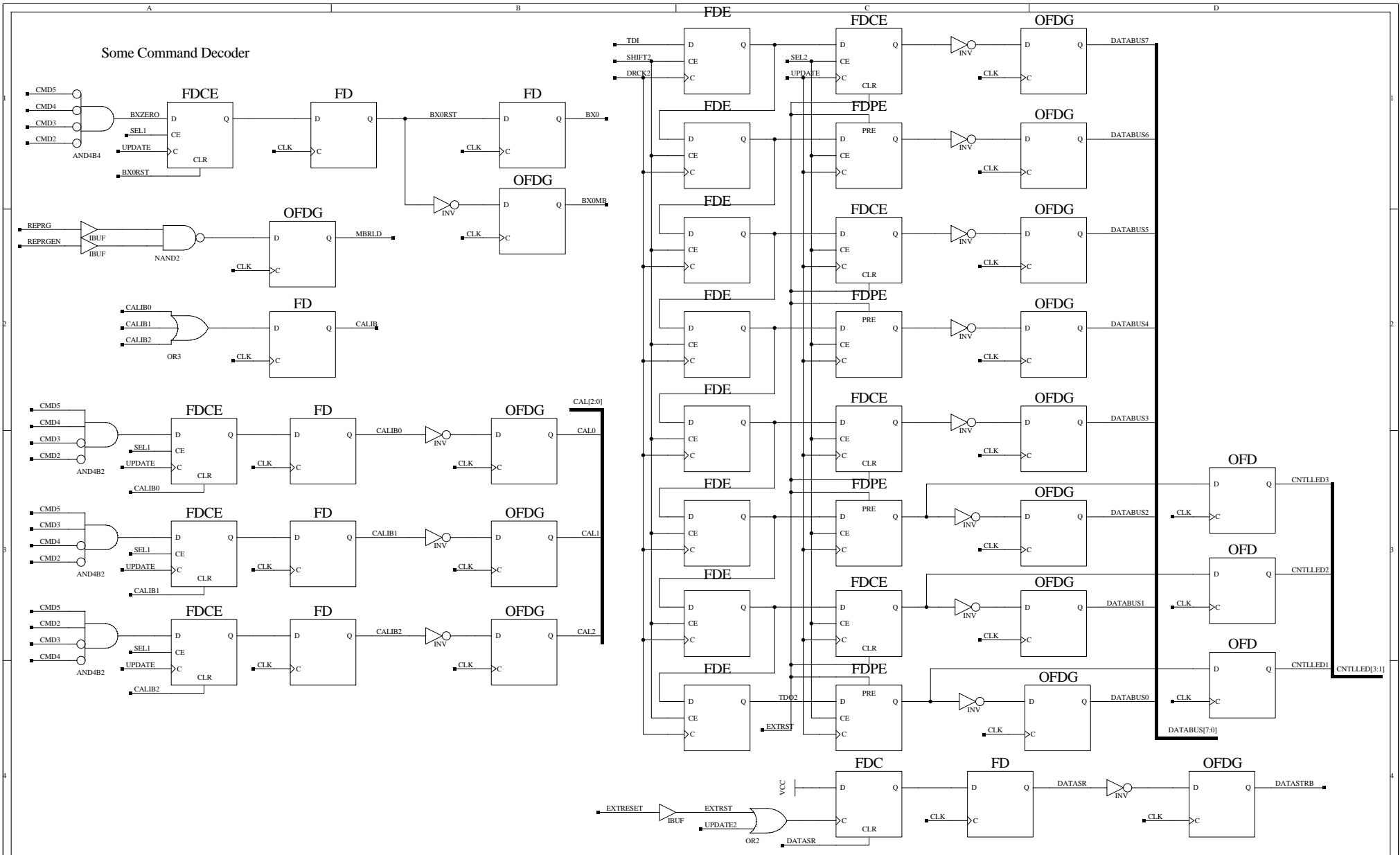
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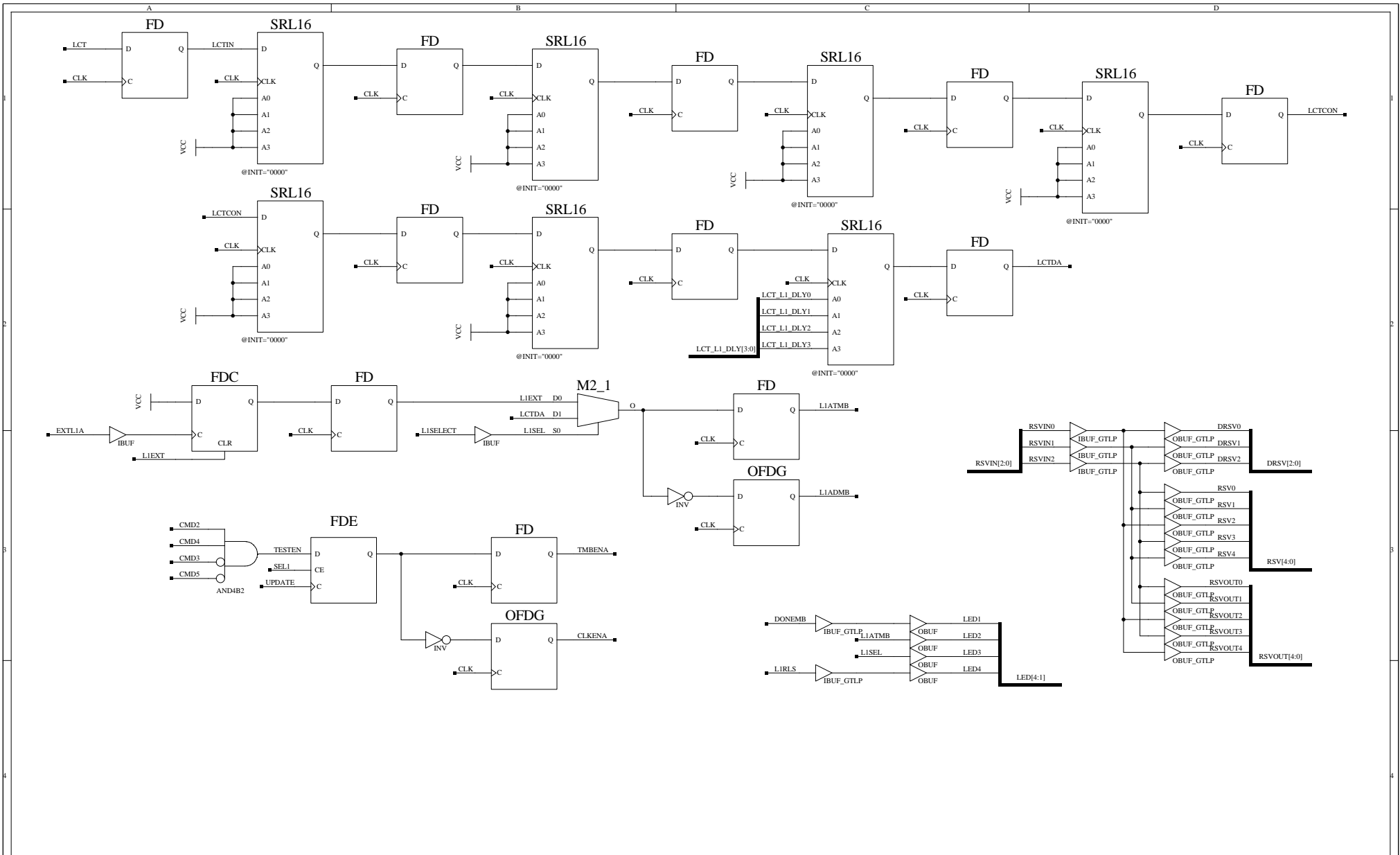
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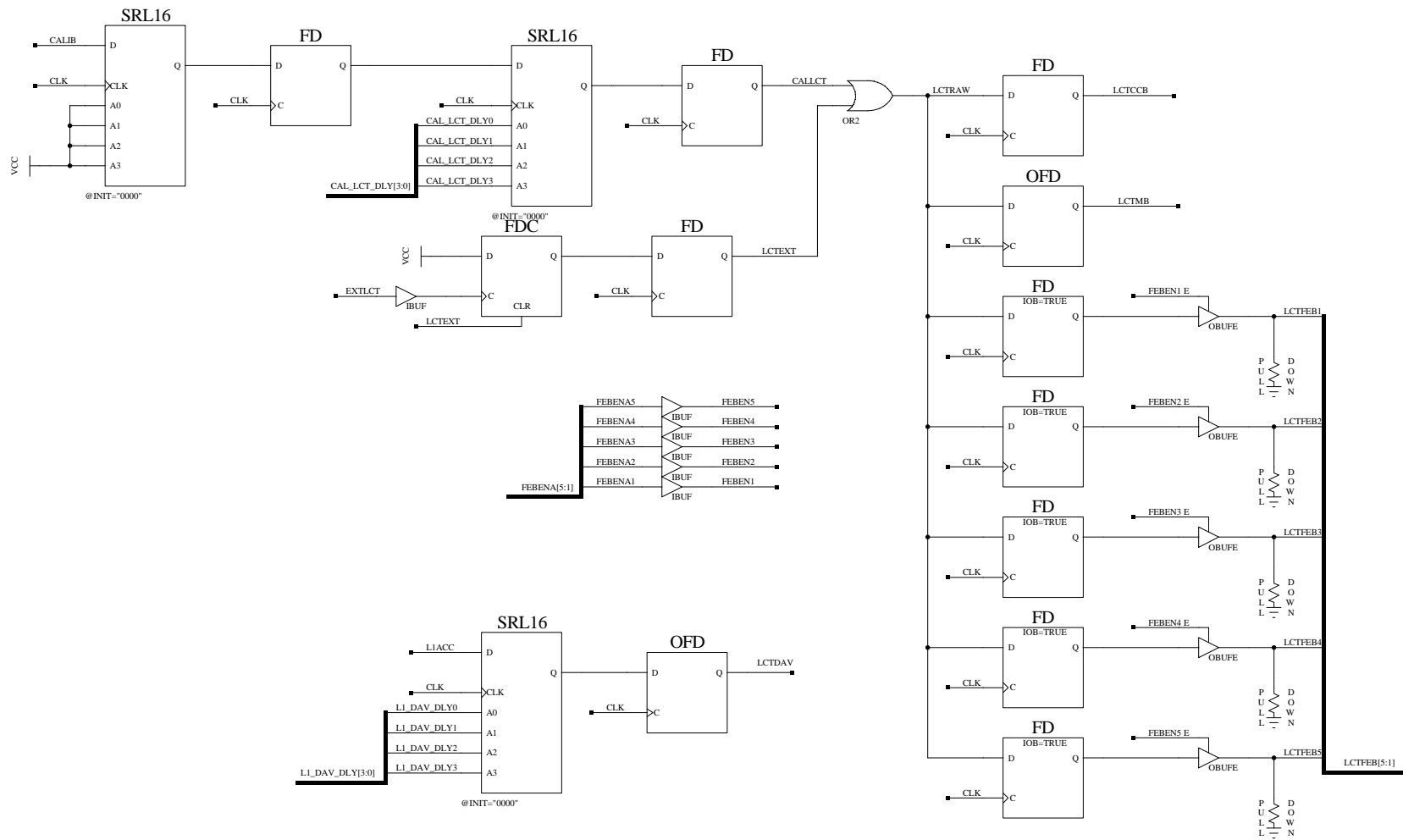


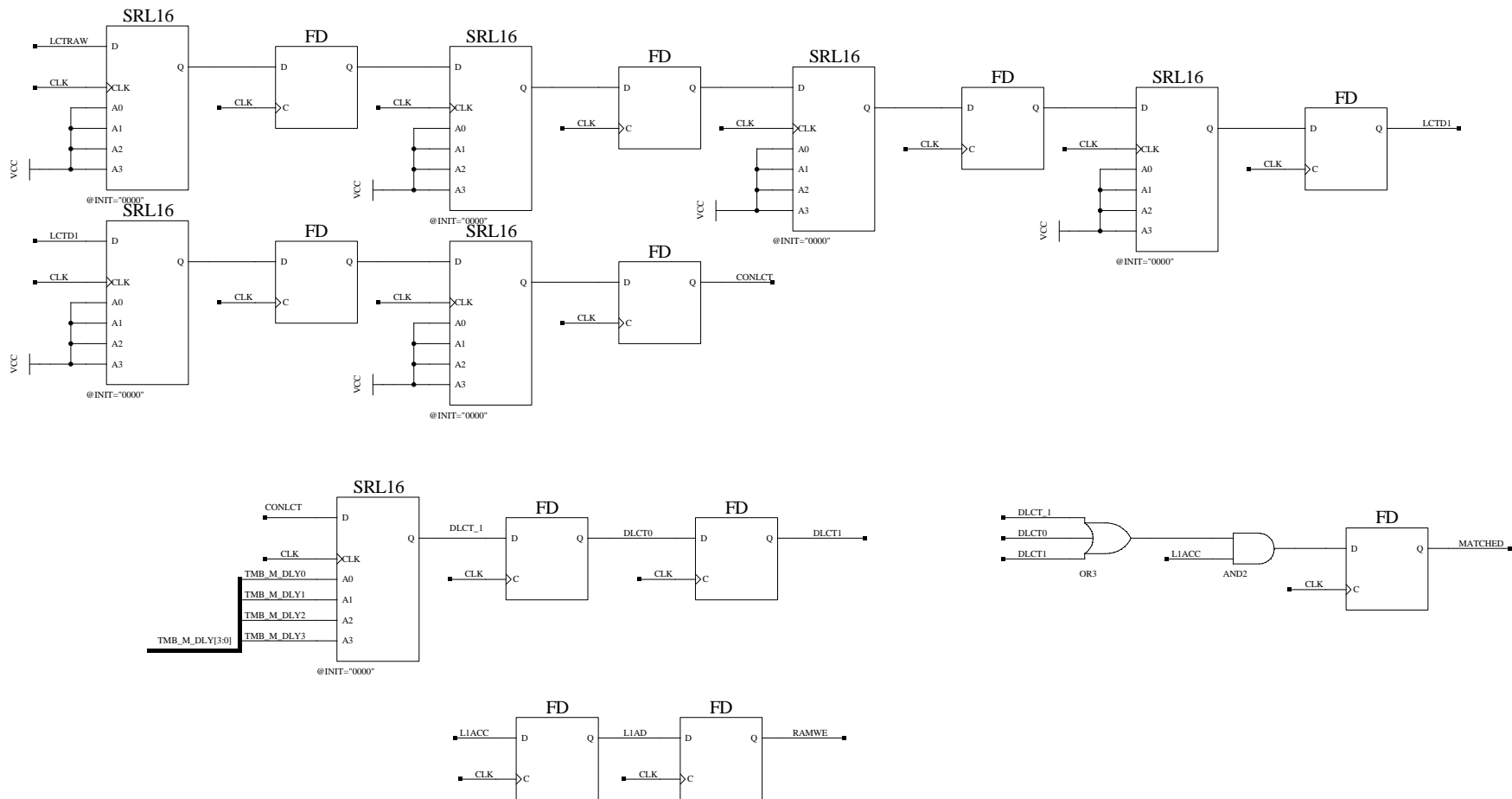


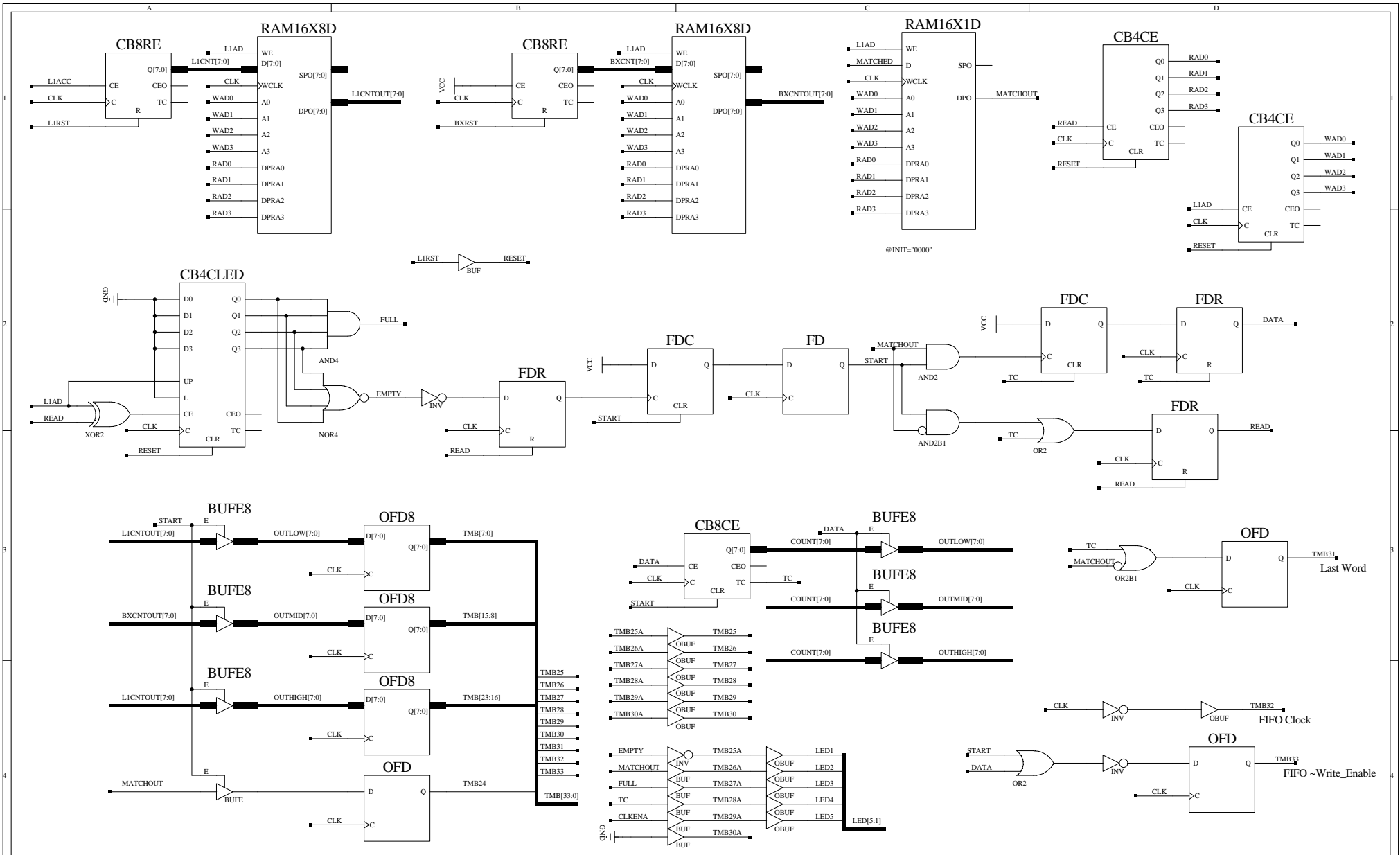


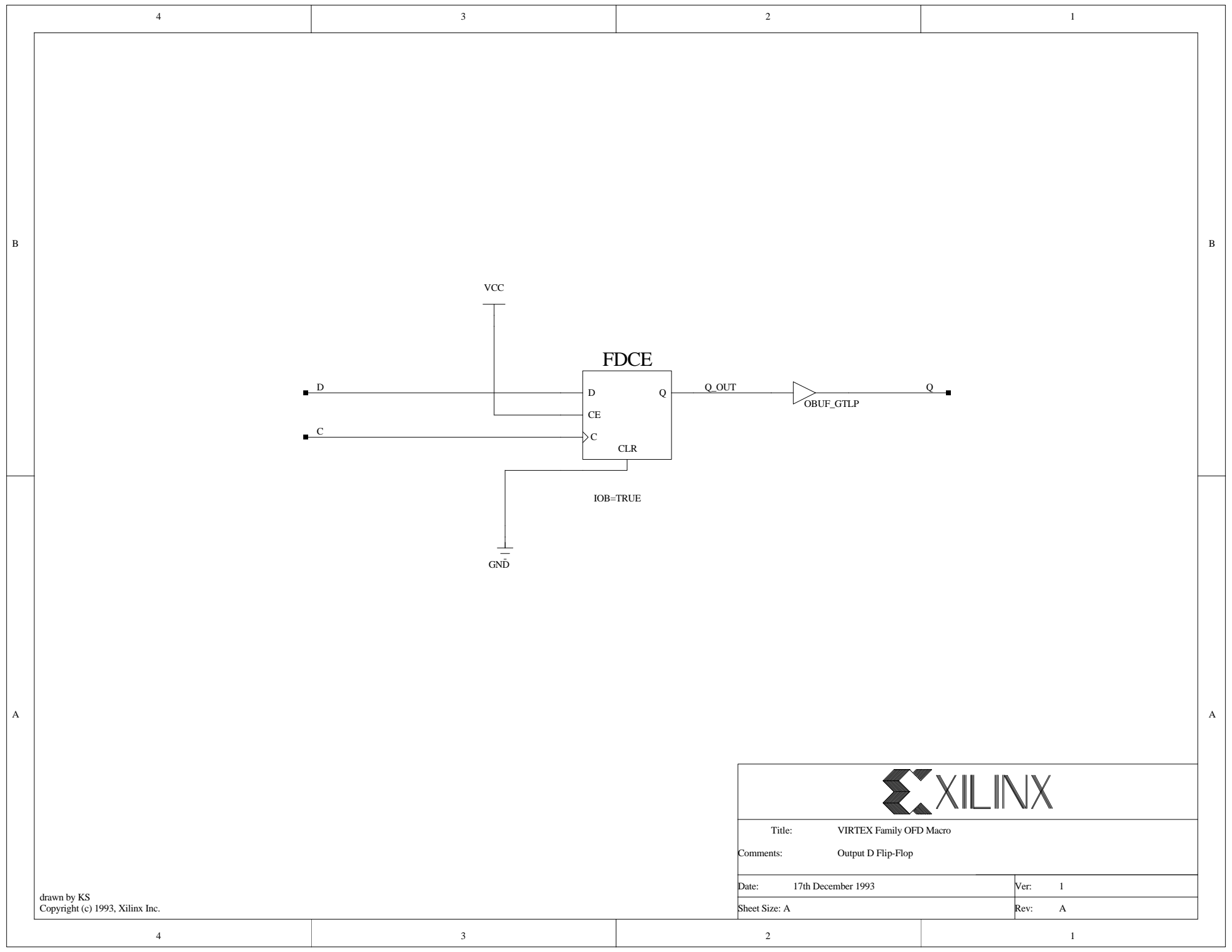













drawn by KS  
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Comments:	Output D Flip-Flop
Date:	17th December 1993
Ver:	1
Sheet Size:	A
Rev:	A