this DDU:
add _BX Offset_ to Flash SRAM

D785B: VME_CTRL (file 0ddu_vme)

2-7-2005_9:36

CMS CSC DDU, VME FPGA

BF005A01 Version 5

v1: extend 34-bit shiting to 48 bits
v2: revert 48-bit shift to 34 bits for all Read cases, add logic for RdFIFO case
v2r2-3: tune XferWcnt timing for RdFIFO case
v2r4: increase SCLK to 24mA, add 200Z terminator
v3: tune for AutoSLD & LEDser0, add VME_Rdy+4 to DDU_SRDY
v4: tune Reset for AutoSLD
v5: Tune DTACK timing for VME-JTAG

Set 3 Banks to 3.3V I/O (banks 2,3,4)

RST_1=Soft_Reset for FPGAs and ALL FIFOs

LABELLED BACKWARDs ON SWITCH BLOCK!

PART=XC2V500-5-FG456
PROM=XC18V04-VQ44 (PARALLEL)

D785B\ddu4_vme\vme4ctrl

VMECNTRL

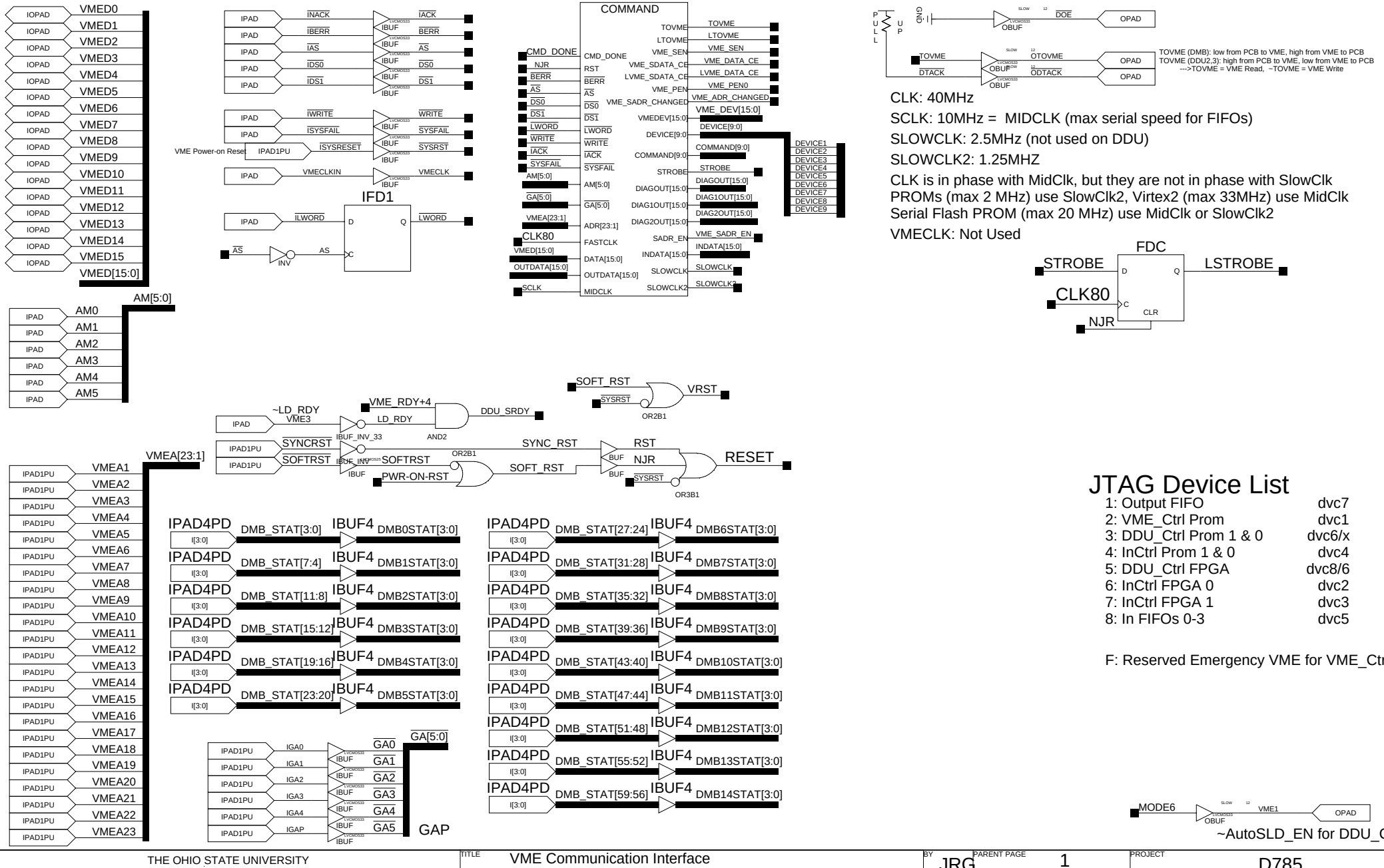
Mode 1 Switch Block, reversed labels on board
1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4 } 00 for Standard Debug, 01 for VME-Serial
6: Mode Bit 5 } 10 for Flash RAM, 11 for VME-Parallel
7: Disable Auto Serial Load
8: Set all IO bits HIGH, ~FPGA version on LEDs

VME Broadcast Addresses:
24=OSU-TCB "Test Control Board"
25=DMB
26=TMB
27=Both DMB and TMB
28=DDU
29=DCC

Use LFF and SLINK_READY to pause mid-event?
Replace EmptyIN/FIFO_EMPTY PUs?

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

To Do:
- COMPARE L1NUM & BXN (DMB T00)
- Watch for TRG buff overflows
- Tune CRC logic for DMB error case
- Connect and drive FMM signals
  ---> Set correct default state on board!
- Monitor: Active-DAV mismatch warn, MOVLP bad evt, BXN match err



JTAG Device List

1: Output FIFO	dvc7
2: VME_Ctrl Prom	dvc1
3: DDU_Ctrl Prom 1 & 0	dvc6/x
4: InCtrl Prom 1 & 0	dvc4
5: DDU_Ctrl FPGA	dvc8/6
6: InCtrl FPGA 0	dvc2
7: InCtrl FPGA 1	dvc3
8: In FIFOs 0-3	dvc5

F: Reserved Emergency VME for VME_Ctrl

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics

BY: JRG	PARENT PAGE: 1	PROJECT: D785	
DATE: 1-18-2005_16:31		FILE: VMECNTRL . 1	PAGE: 2A

DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK

The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz

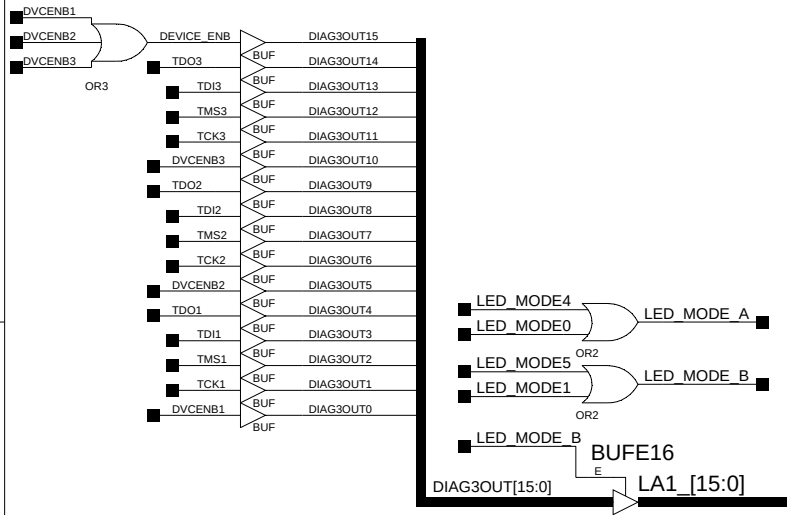
The ISP does not work at 2.5MHz or faster

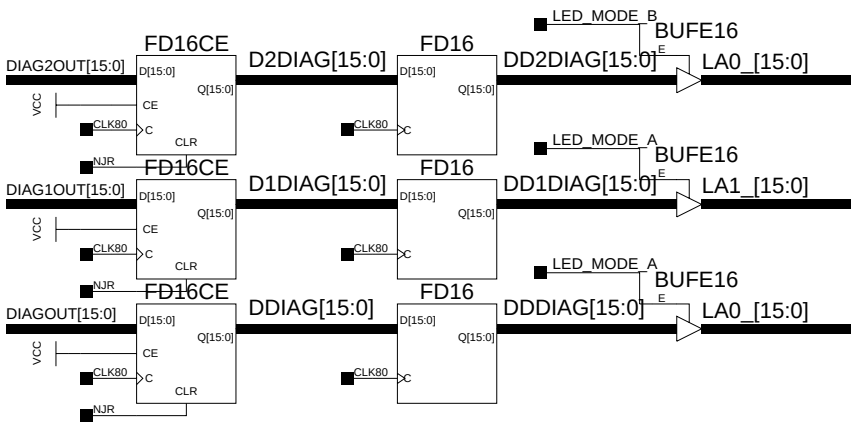
Free LED_Modes

LA free: 7,12,13,14

LEDs Free: 7,12,13,14

TP 2-4 Used: 0,1

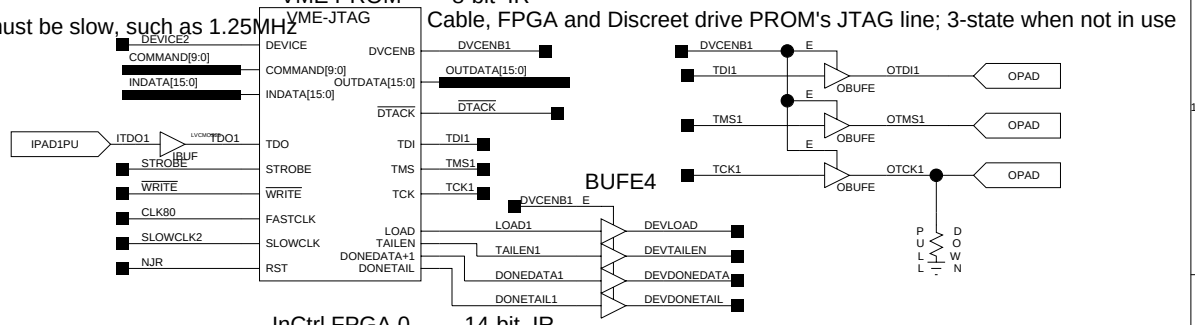




VME PROM 8-bit IR

VME-JTAG

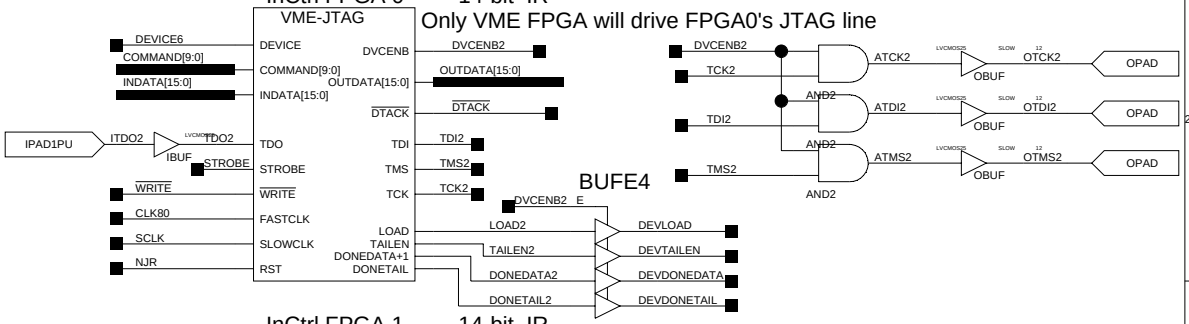
Cable, FPGA and Discreet drive PROM's JTAG line; 3-state when not in use



InCtrl FPGA 0 14-bit IR

VME-JTAG

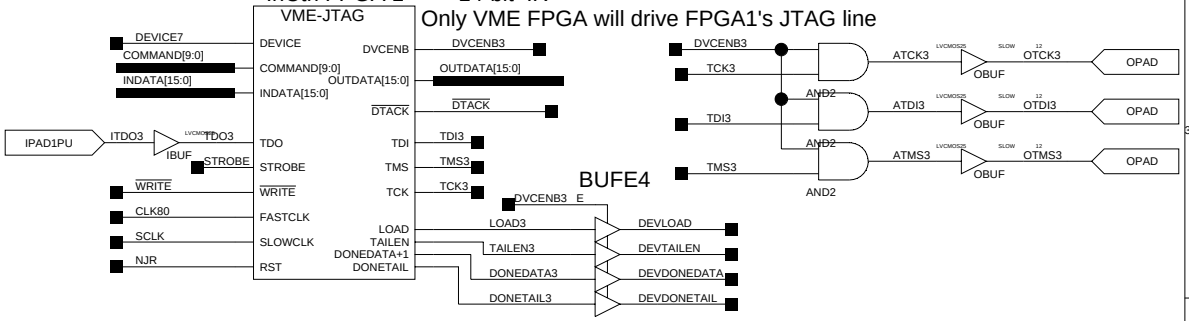
Only VME FPGA will drive FPGA0's JTAG line



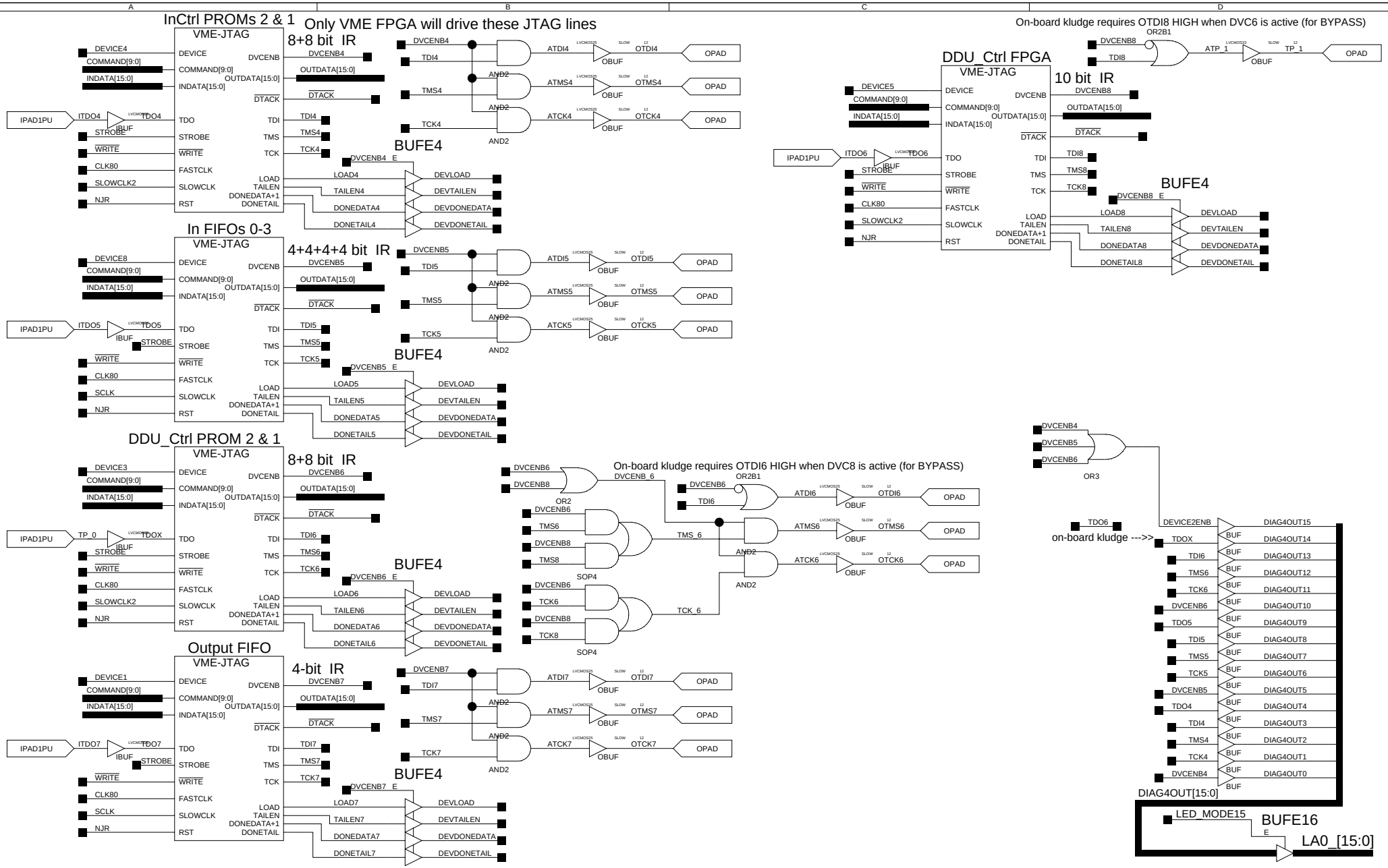
InCtrl FPGA 1 14-bit IR

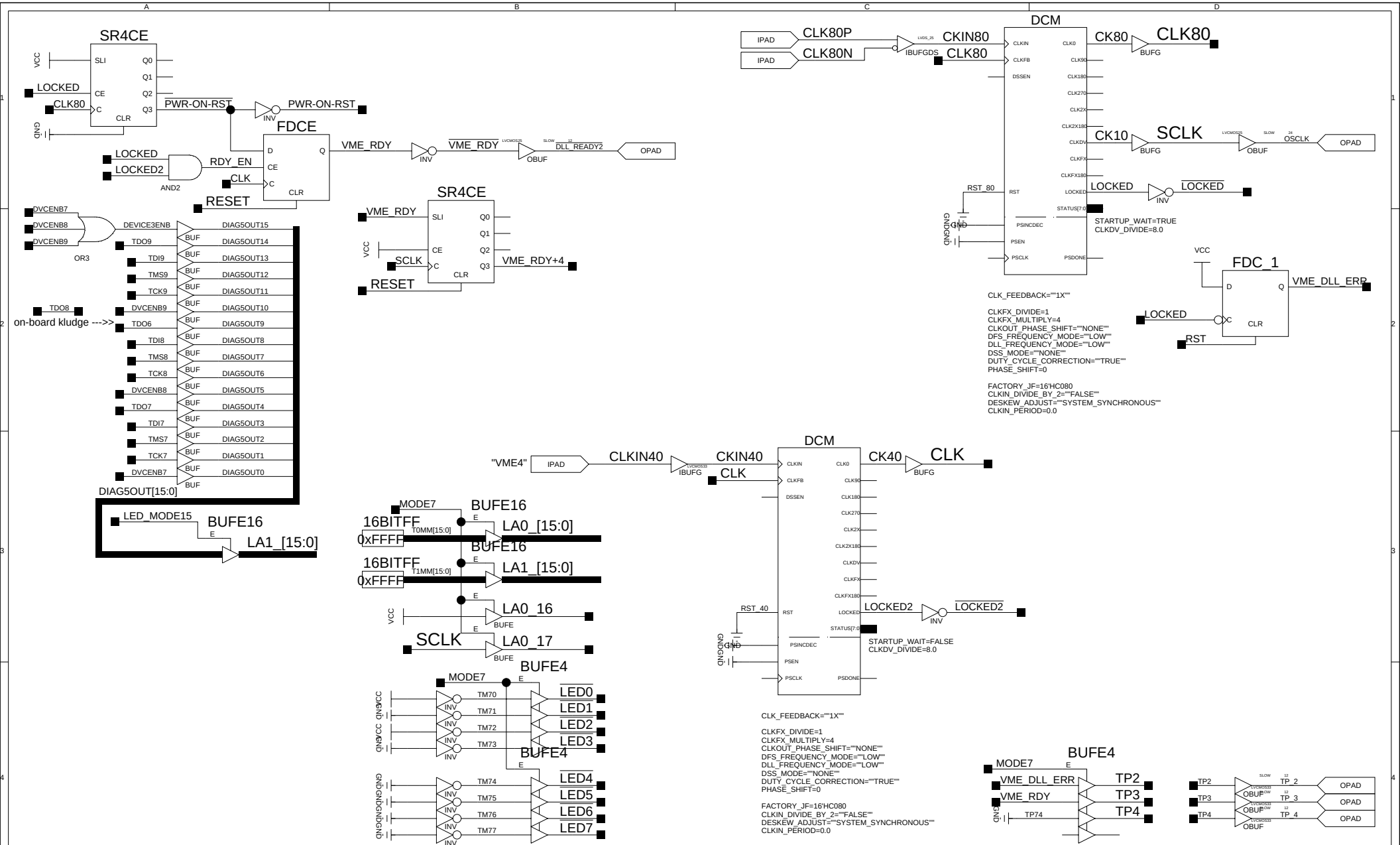
VME-JTAG

Only VME FPGA will drive FPGA1's JTAG line

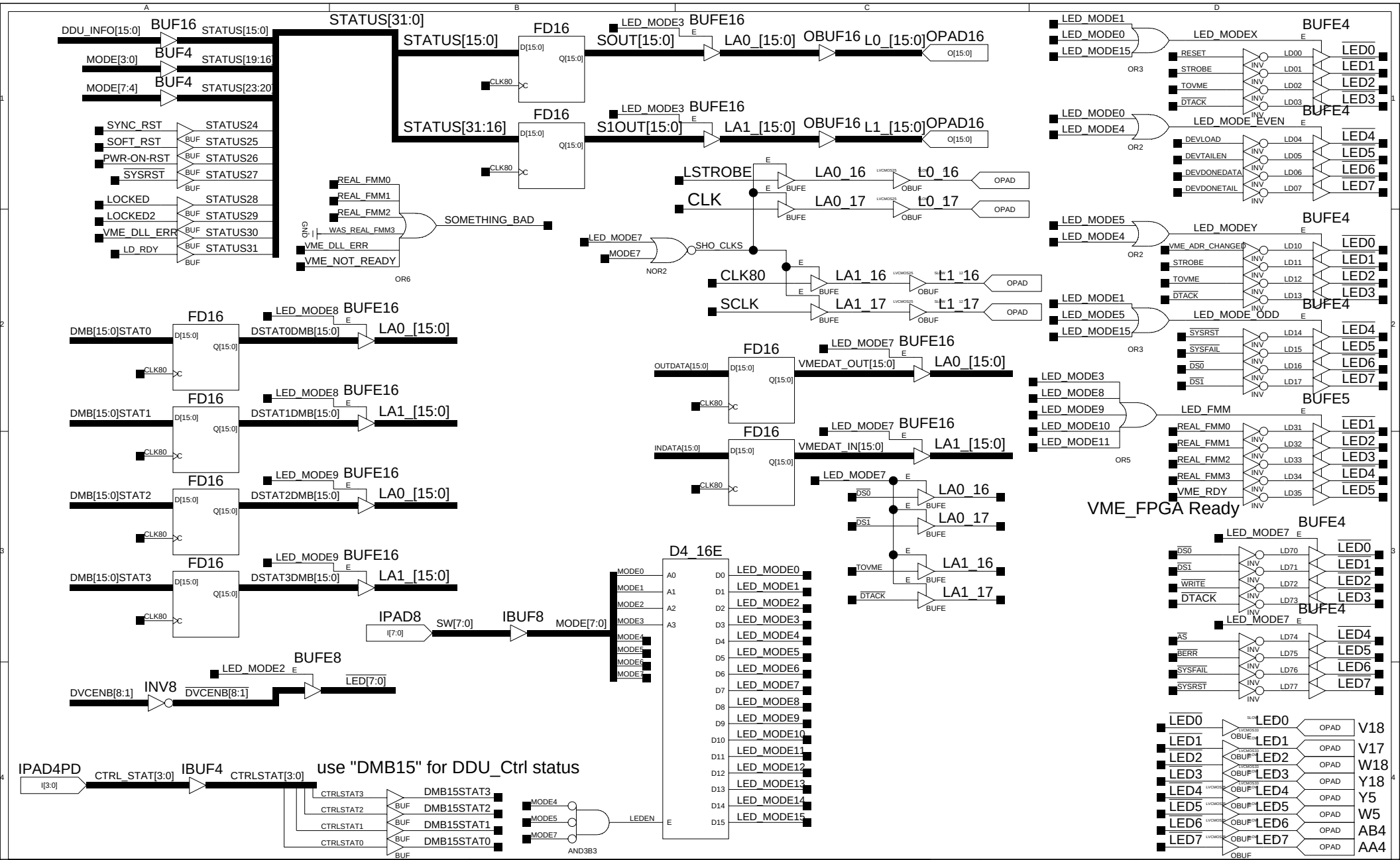


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785
		DATE: 1-18-2005_16:31	FILE: VMECNTRL . 2	PAGE: 2B

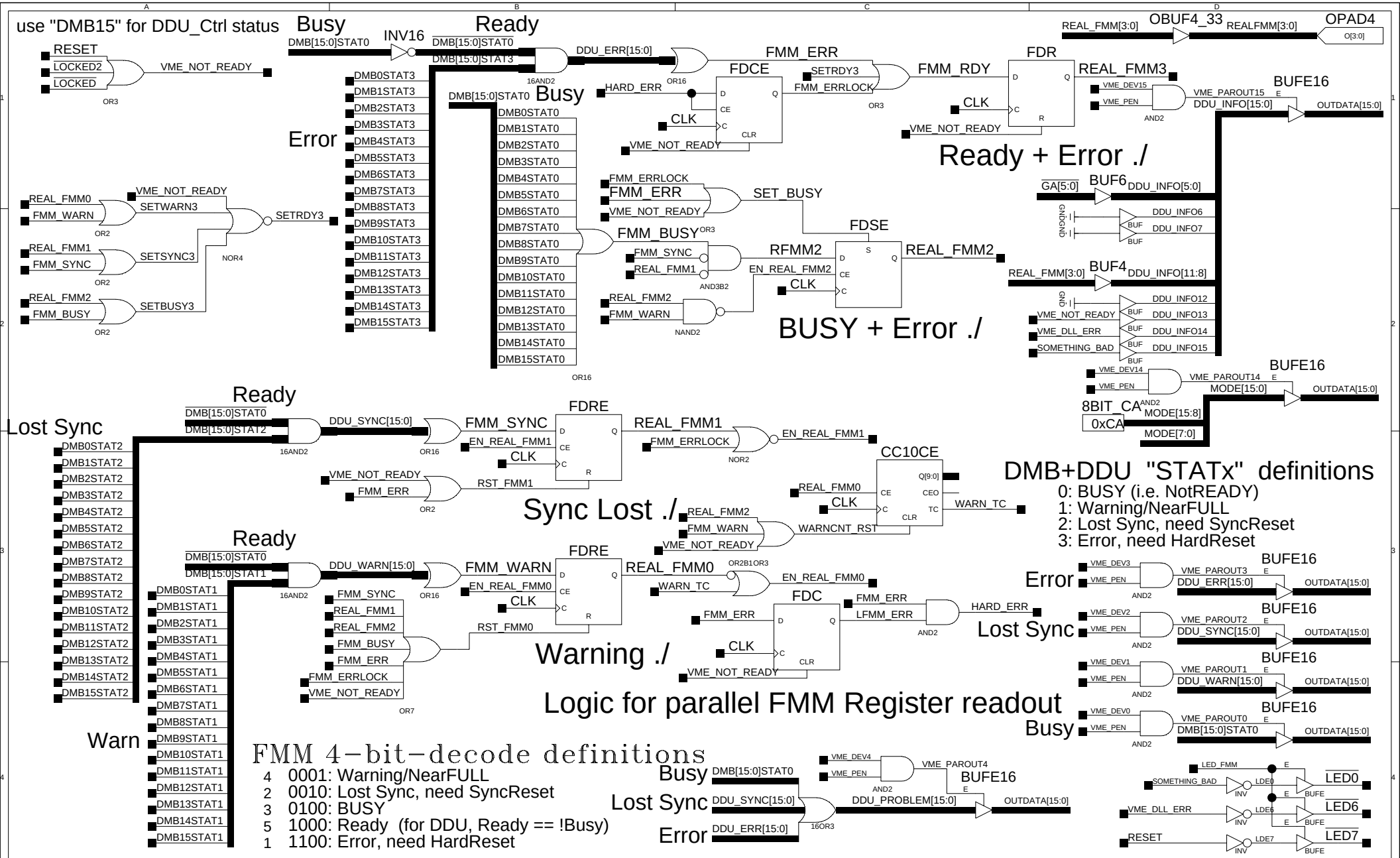

InCtrl PROMs 2 & 1
Only VME FPGA will drive these JTAG lines
VME-JTAG
8+8 bit IR
In FIFOs 0-3
4+4+4+4 bit IR
DDU_Ctrl PROM 2 & 1
8+8 bit IR
Output FIFO
4-bit IR
DDU_Ctrl FPGA
10 bit IR
On-board kludge requires OTDI8 HIGH when DVC6 is active (for BYPASS)
On-board kludge requires OTDI6 HIGH when DVC8 is active (for BYPASS)
BUFE4
AND2
OR2
OR3
SOP4
OBUF
IBUF
OPAD
on-board kludge --->>
DIAG4OUT[15:0]
BUFE16
LA0_[15:0]
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics
JRG
1
D785
4-28-2004_8:12
VMECNTRL . 3
2C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-18-2005_16:31	PARENT PAGE: 1 FILE: VMECNTRL . 4
		PROJECT: D785	PAGE: 2D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-10-2004_17:10	PARENT PAGE: 1 FILE: VMECNTRL . 5
		PROJECT: D785	PAGE: 2E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 12-27-2004_17:11	PARENT PAGE: 1 FILE: VMECNTRL . 6
		PROJECT: D785	PAGE: 2F

Serial Device List (12 device functions, SEN = Serial Load)

0x 00: Read InFIFO 0
01: Read InFIFO 1
02: Read InFIFO 2
03: Read InFIFO 3
04: R/W Flash SRAM

Non-VME!! Auto Load Only

0x 08: W Load DDR InFIFO 0
09: W Load DDR InFIFO 1
0A: W Load DDR InFIFO 2
0B: W Load DDR InFIFO 3

VME_SDEV>=8 or ==4 are Writeable; others are Read Only.

0C: W Load GBE Output FIFO (SEN=LD, set HI during MRST) --test?
0D: W Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.) --test?
0E: W Load DDU_Ctrl FPGA (Board ID) --test?
0F: W Load all 4 DDR InFIFOs

9 VME Reads, 4 VME Writes, 7 Auto commands

Flash <--> Serial
Auto Load After MRST

VME <--> Serial-Rd Only, No Flash SRAM (dev,FMpage=VMEcmd)

vmedev 00 --ToVME=1
01 --ToVME=1
02 --ToVME=1
03 --ToVME=1

SLDcmd 02: (all 4 in parallel) 08,04 09,04 0A,04 0B,04 DDR

SLDcmd 03: 0C,05 GbE

SLDcmd 00: 0D,01 (on DDU_Ctrl request) Kill-Ch

SLDcmd 01: 0E,07 (after 0D,01) Board-ID

VME <--> Flash SRAM, No Serial Dev

vmedev04/cmd 00 --ToVME=1
09 --ToVME=0
0C --ToVME=0
0D --ToVME=0
0F --ToVME=0

Flash Memory Access (9 VME-Serial commands on Dev4)

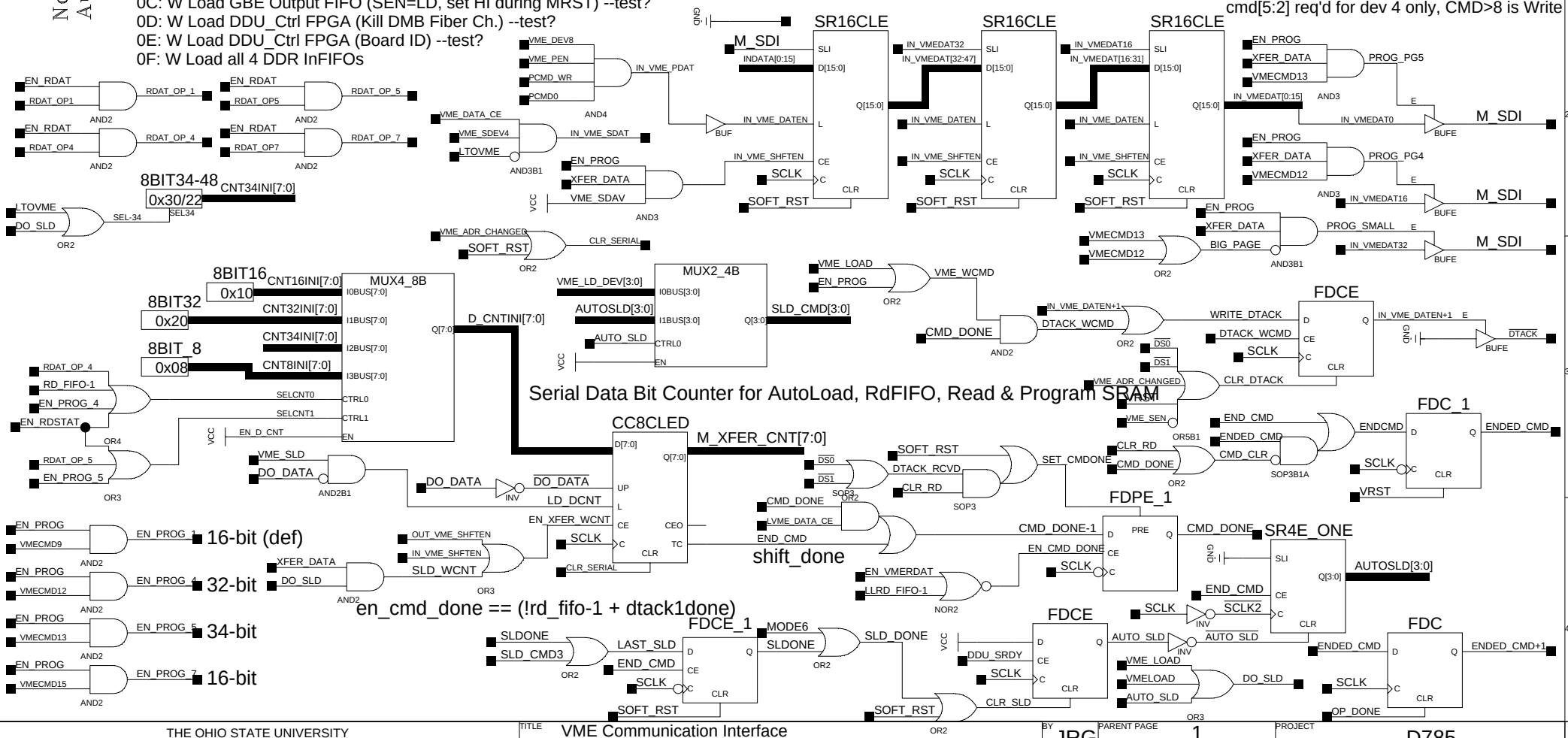
CMD<9 is Read Only. CMD>=9 is Write Only.

0x 00: Read Status Register
01: Read page 1 (Kill Ch.) to DDU_Ctrl
04: Read page 4 (DDR offsets) to In DDR FIFO
05: Read page 5 (GBE offsets) to GBE Out FIFO
07: Read page 7 (Board ID) to DDU_Ctrl

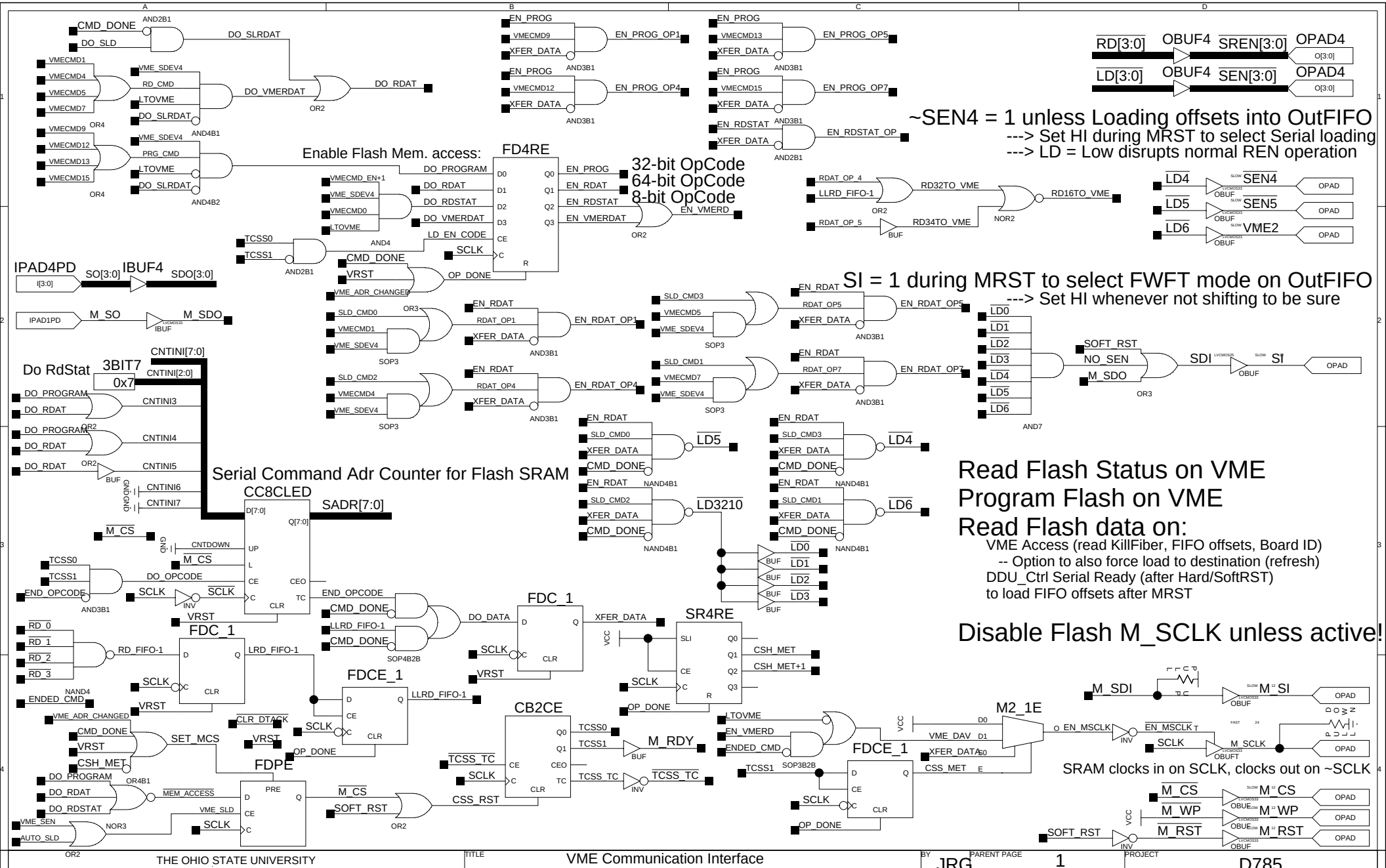
0x 09: W Program page 1 (Kill Ch.) [16 bit data]
0C: W Program page 4 (DDR offsets) [32 bit data]
0D: W Program page 5 (GBE offsets) [34 bit data]
0F: W Program page 7 (Board ID) [16 bit data]

Serial VME_ADR: slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]

cmd[5:2] req'd for dev 4 only, CMD>8 is Write

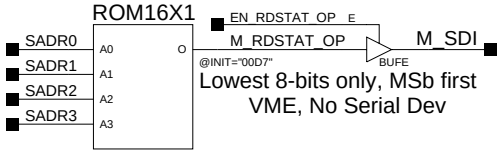


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-27-2005_13:48	PARENT PAGE: 1 FILE: VMECNTRL . 7	PROJECT: D785 PAGE: 2G

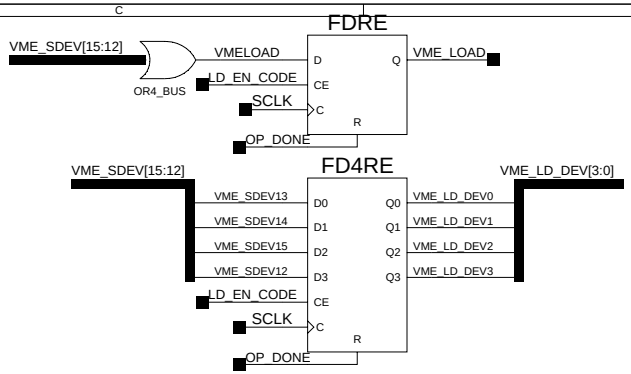


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-6-2005_14:56	PARENT PAGE: 1 FILE: VMECNTRL . 8
		PROJECT: D785	PAGE: 2H

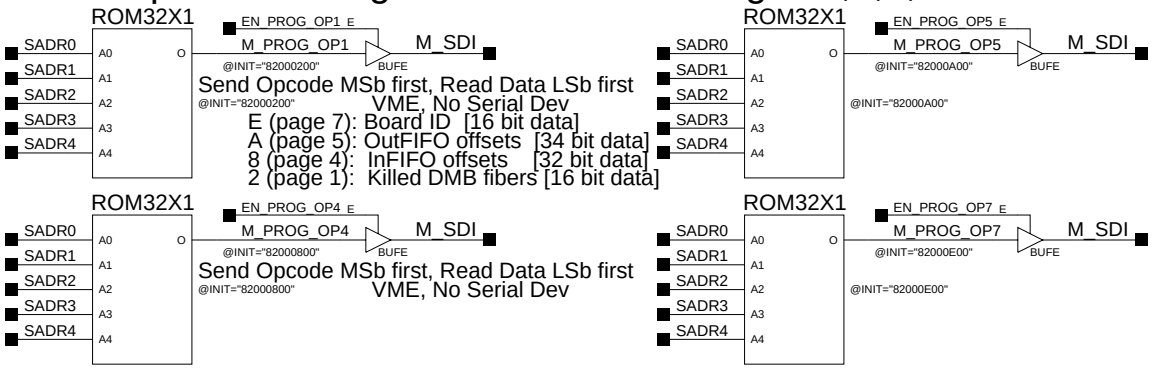
8-bit Opcode: Read Flash SRAM Status



Lowest 8-bits only, MSb first
VME, No Serial Dev

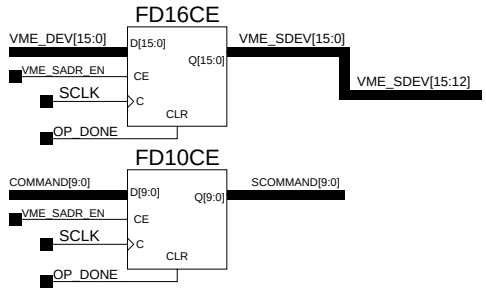


32-bit Opcodes: Program Flash SRAM Pages 1,4,5,7

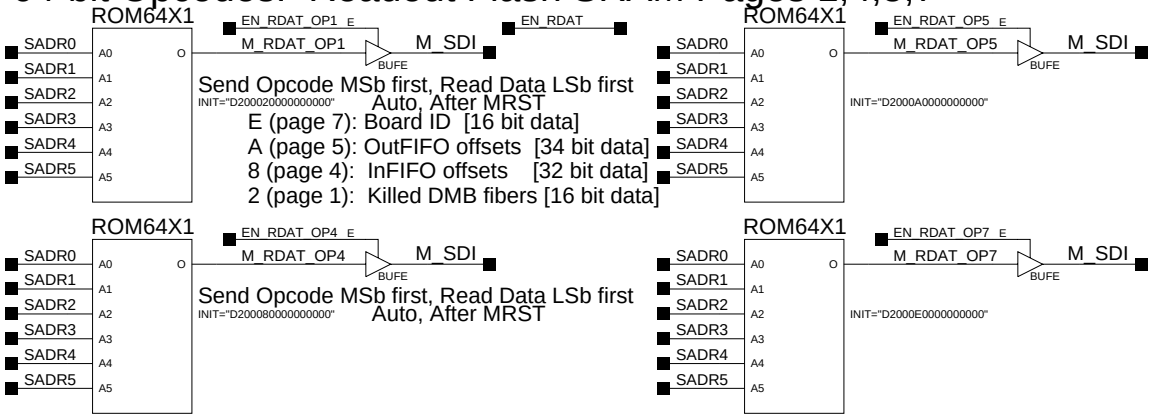


Send Opcode MSb first, Read Data LSb first
@INIT="82000200" VME, No Serial Dev
E (page 7): Board ID [16 bit data]
A (page 5): OutFIFO offsets [34 bit data]
8 (page 4): InFIFO offsets [32 bit data]
2 (page 1): Killed DMB fibers [16 bit data]

Send Opcode MSb first, Read Data LSb first
@INIT="82000800" VME, No Serial Dev



64-bit Opcodes: Readout Flash SRAM Pages 1,4,5,7



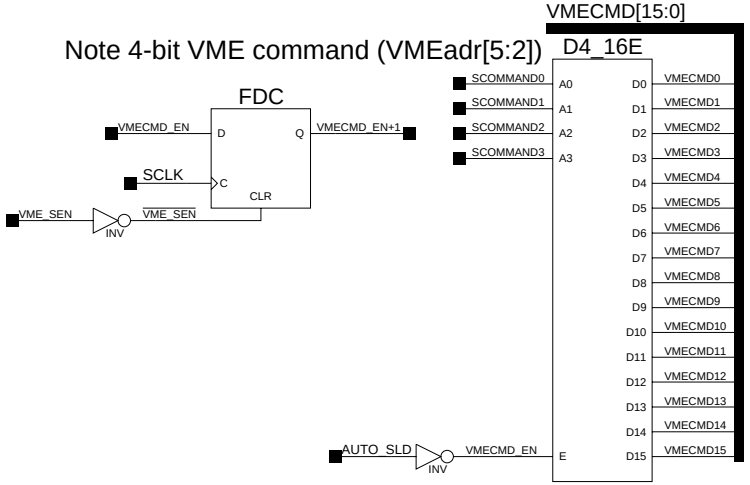
Send Opcode MSb first, Read Data LSb first
INIT="D200020000000000" Auto, After MRST
E (page 7): Board ID [16 bit data]
A (page 5): OutFIFO offsets [34 bit data]
8 (page 4): InFIFO offsets [32 bit data]
2 (page 1): Killed DMB fibers [16 bit data]

Send Opcode MSb first, Read Data LSb first
INIT="D200080000000000" Auto, After MRST

INIT="D2000A0000000000"

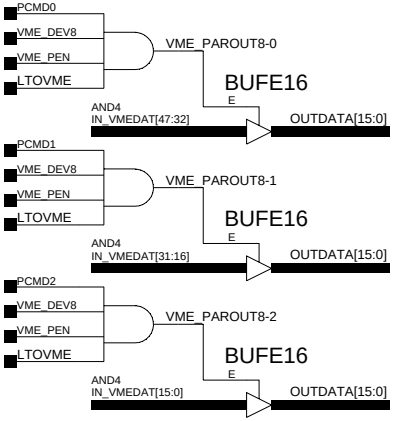
INIT="D2000E0000000000"

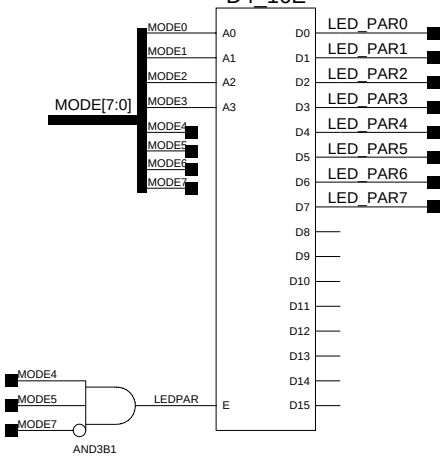
Note 4-bit VME command (VMEadr[5:2])

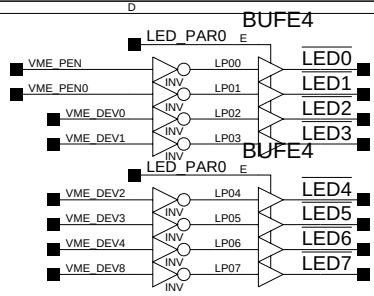


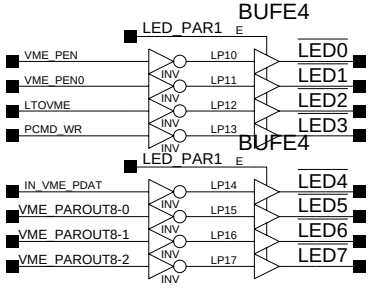
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785
		DATE: 1-4-2005_17:12	FILE: VMECNTRL . 9	PAGE: 2I

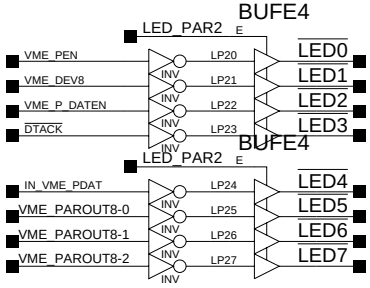
Parallel Register Readout







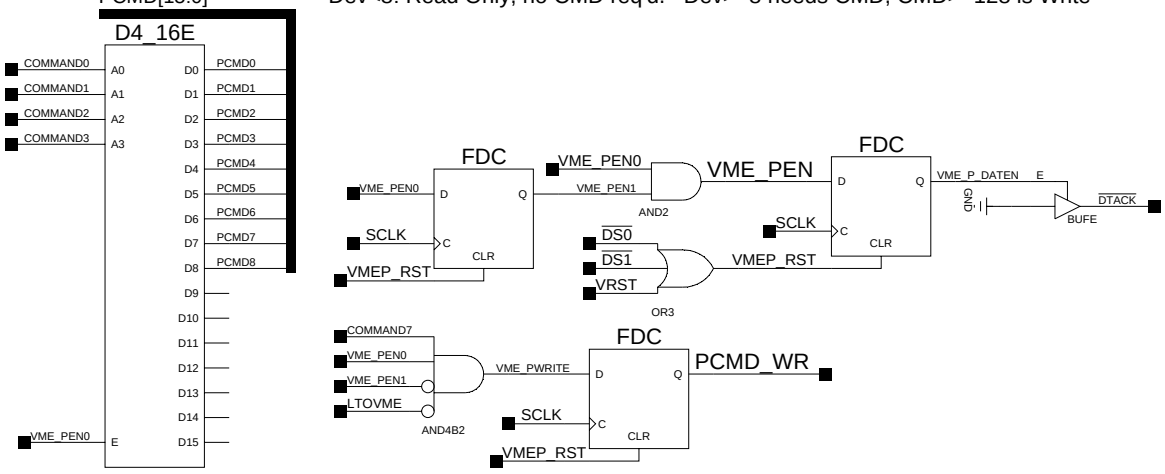


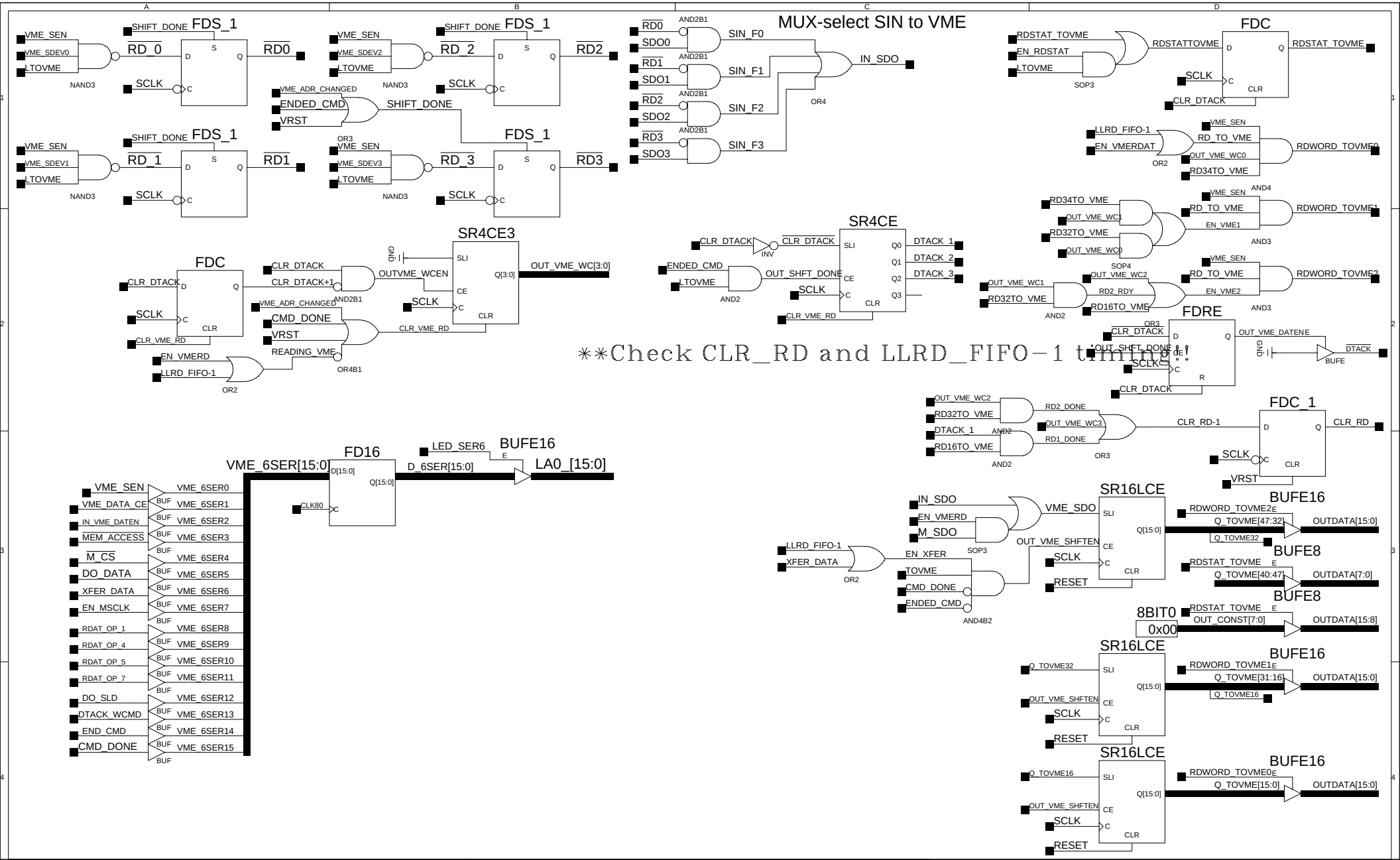


Parallel VME_ADR: slot[23-19]typ[18-16]dev[15-12]free[11-10]cmd[9-2]res[1-0]

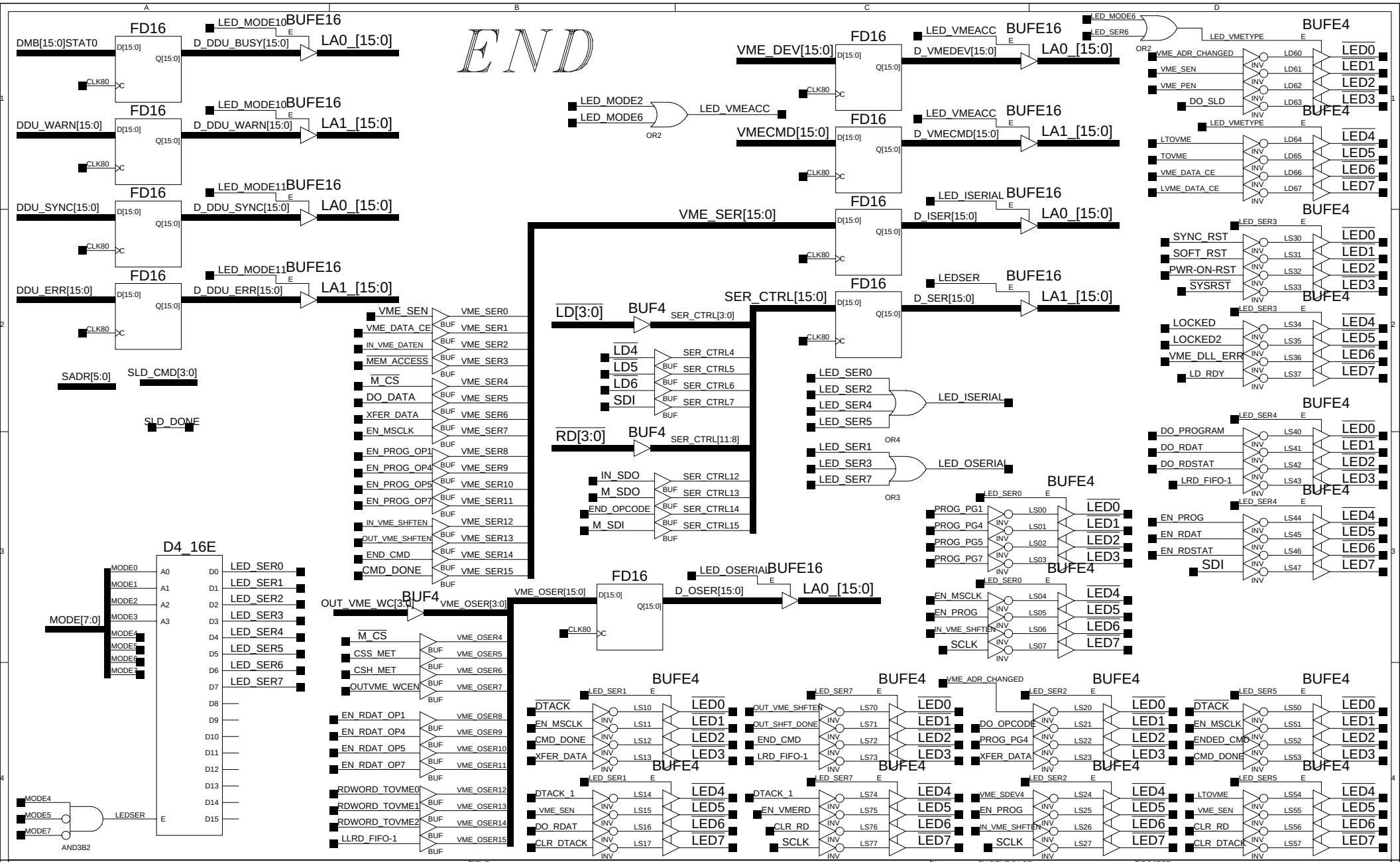
PCMD[15:0]

Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write



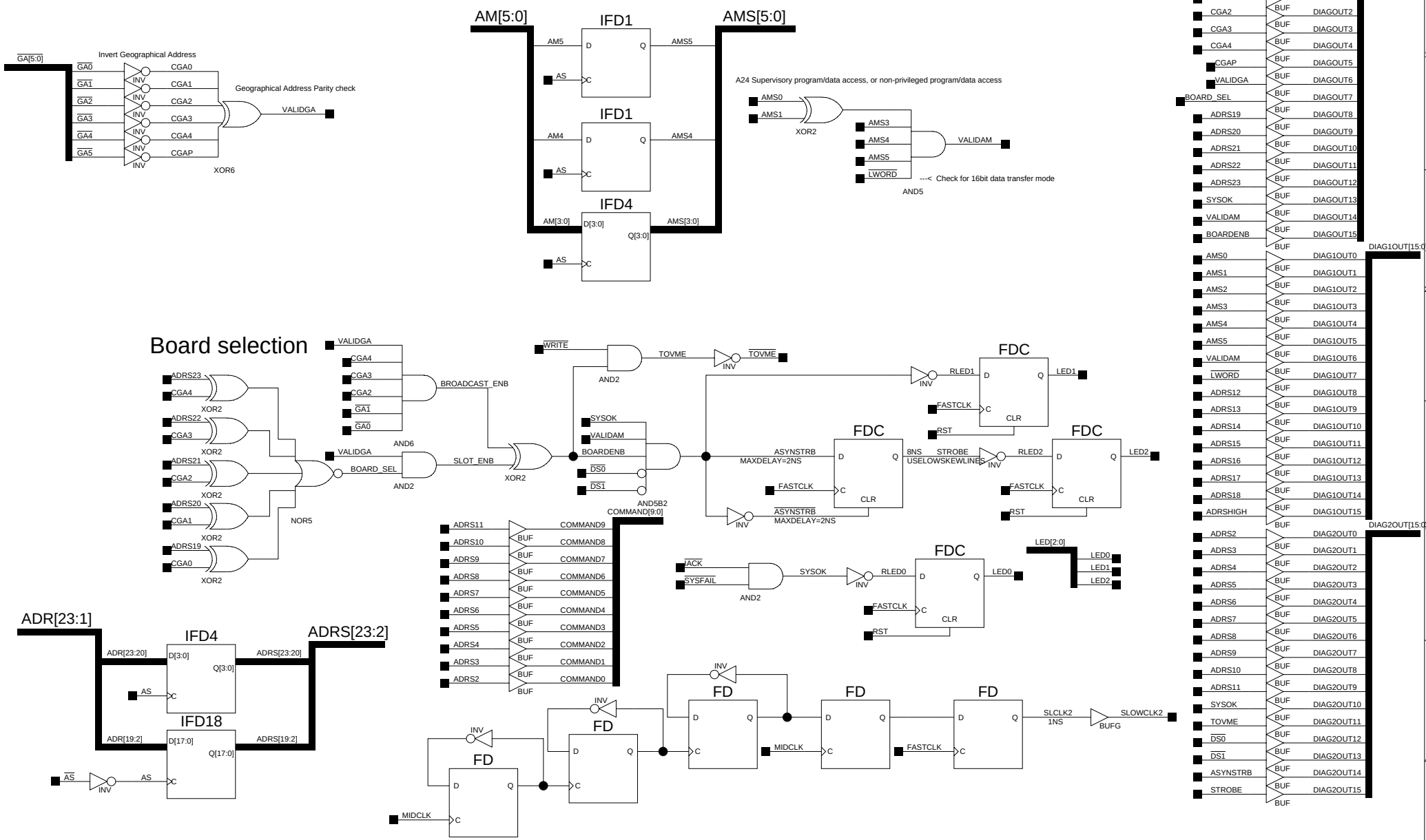


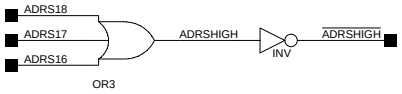
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 2-7-2005_9:36	PARENT PAGE: 1 FILE: VMECNTRL . 11
		PROJECT: D785	PAGE: 2K



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 2-7-2005_9:36	PARENT PAGE: 1 FILE: VMECNTRL . 12
		PROJECT: D785	PAGE: 2L

DDU Broadcast Address = 28 = 0x1C = 11100b





Slot Selection: ADR[23:19] ADR[1:0]=Not Used

Device: ADR[15:12] sets device ID

Type: ADR[18:16]=000b for VME-JTAG

COMMAND[9:0] { ADR[11:8]=bit count
ADR[7:2]=JTAG command

slot[23-19]typ[18-16]dev[15-12]bitcnt[11-8]cmd[7-2]res[1-0]

ADR[18:16]=100b for VME-Serial

COMMAND[9:0] { ADR[11:6]=Not Used
ADR[5:2]=serial command (req'd for dev 4 only)

slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]

Dev>=8: Write Only. Dev=4 needs CMD, CMD>=9 is Write. Otherwise Read

ADR[18:16]=011b for VME-Parallel

Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write

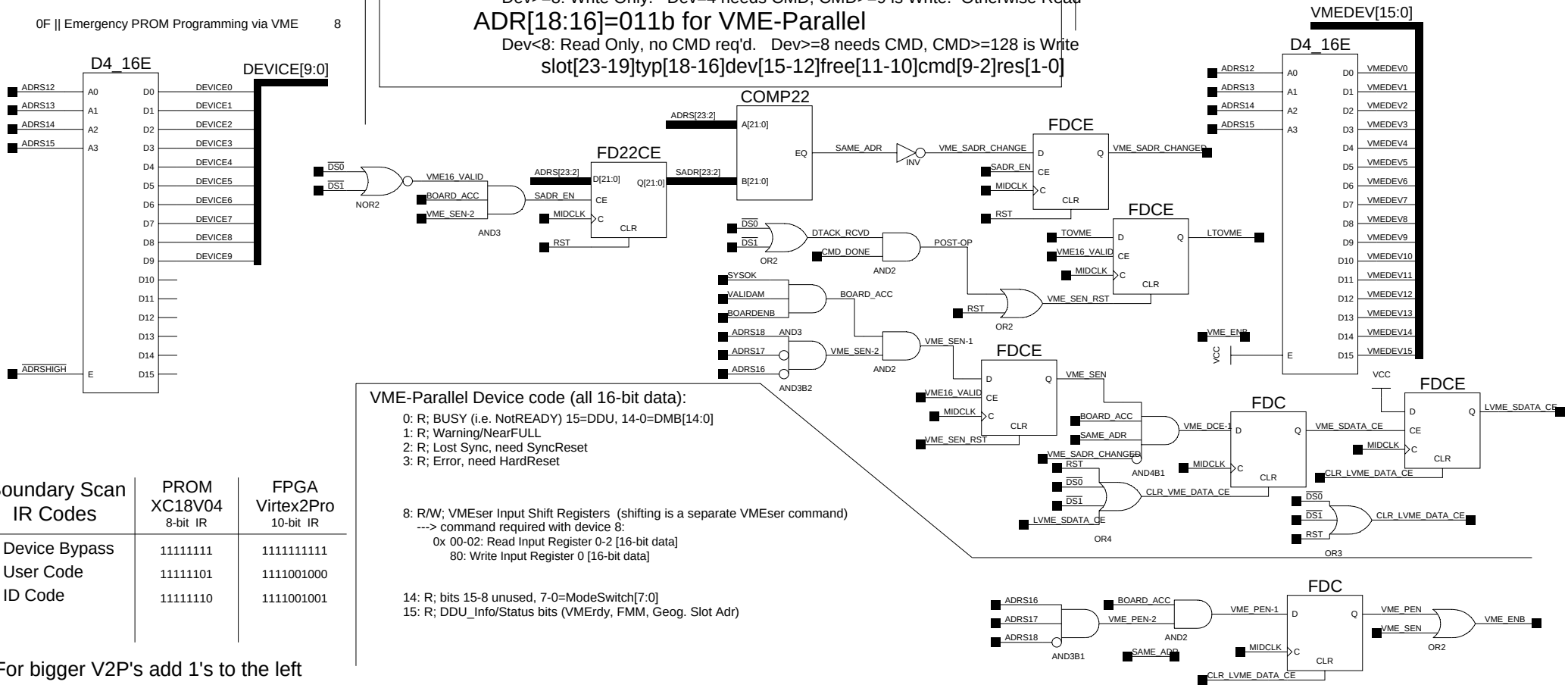
slot[23-19]typ[18-16]dev[15-12]free[11-10]cmd[9-2]res[1-0]

VME-JTAG Device code: Path IR bit length

00 ||	
01 || Output FIFO **FIX**	4
02 || VME_Ctrl PROM (all PROMs=XC18V04)	8
03 || DDU_Ctrl PROMs 1 & 0	8+8
04 || InCtrl PROMs 1 & 0	8+8
05 || DDU_Ctrl FPGA (V2P7)	10
06 || InCtrl FPGA 0 (V2P20)	14
07 || InCtrl FPGA 1 (V2P20)	14
08 || Input FIFOs 0-3	4+4+4+4
0F || Emergency PROM Programming via VME	8

VME-Serial Device code:

00 || Read Input FIFO 0 (32-bit data, no Command req'd)
01 || Read Input FIFO 1 (32-bit data, no Command req'd)
02 || Read Input FIFO 2 (32-bit data, no Command req'd)
03 || Read Input FIFO 3 (32-bit data, no Command req'd)
04 || Flash SRAM (RdStat or Program Page), NEEDS COMMAND
---> command required with device 4:
0x 00: Read Status Register [8-bit data]
09: Program page 1 (Kill Ch.) [16 bit data]
0C: Program page 4 (DDR offsets) [32 bit data]
0D: Program page 5 (GBE offsets) [34 bit data]
0F: Program page 7 (Board ID) [16 bit data]
0C || Load GBE Output FIFO (SEN=LD, set HI during MRST)--N/A
0D || Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.)--N/A
0E || Load DDU_Ctrl FPGA (Board ID)--N/A
0F || Load all 4 DDR InFIFOs



VME-Parallel Device code (all 16-bit data):

0: R; BUSY (i.e. NotREADY) 15=DDU, 14-0=DMB[14:0]
1: R; Warning/NearFULL
2: R; Lost Sync, need SyncReset
3: R; Error, need HardReset

8: R/W; VMEser Input Shift Registers (shifting is a separate VMEser command)
---> command required with device 8:
0x 00-02: Read Input Register 0-2 [16-bit data]
80: Write Input Register 0 [16-bit data]

14: R; bits 15-8 unused, 7-0=ModeSwitch[7:0]
15: R; DDU_Info/Status bits (VMErdy, FMM, Geog. Slot Adr)

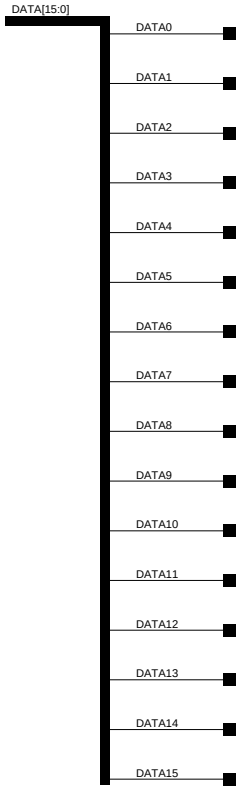
Boundary Scan IR Codes	PROM XC18V04 8-bit IR	FPGA Virtex2Pro 10-bit IR
Device Bypass	11111111	1111111111
User Code	11111101	1111001000
ID Code	11111110	1111001001

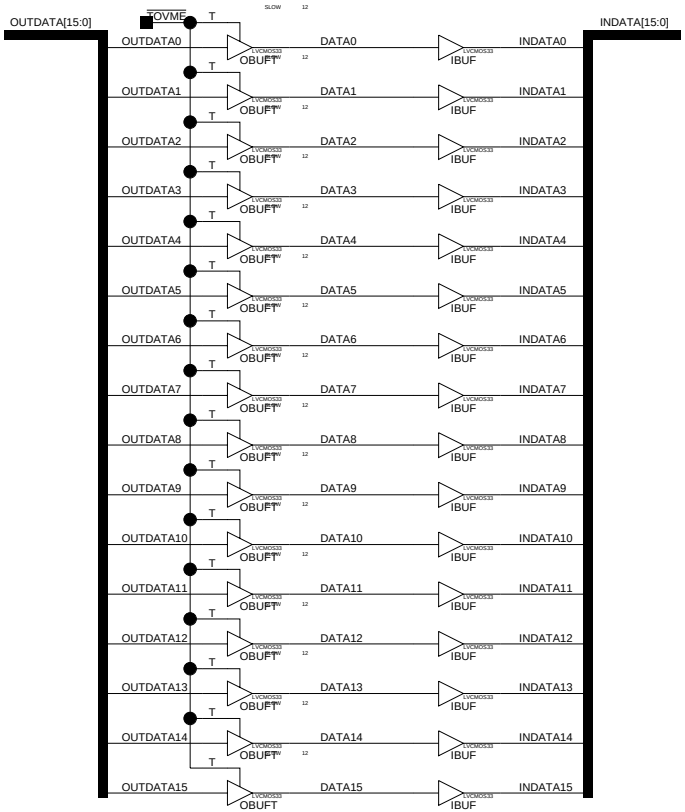
For bigger V2P's add 1's to the left

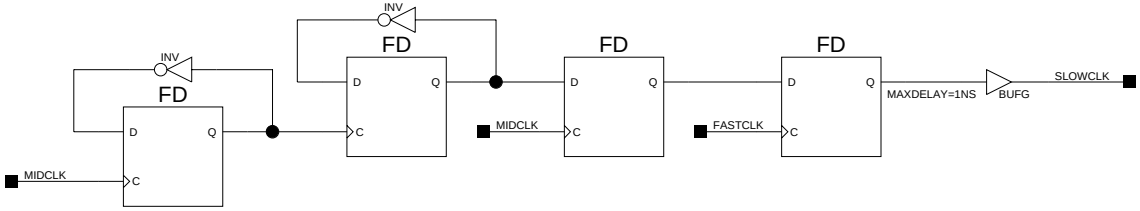
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: VME-Read Command Decoder
DDU VME Controller Logic
CMS CSC Electronics

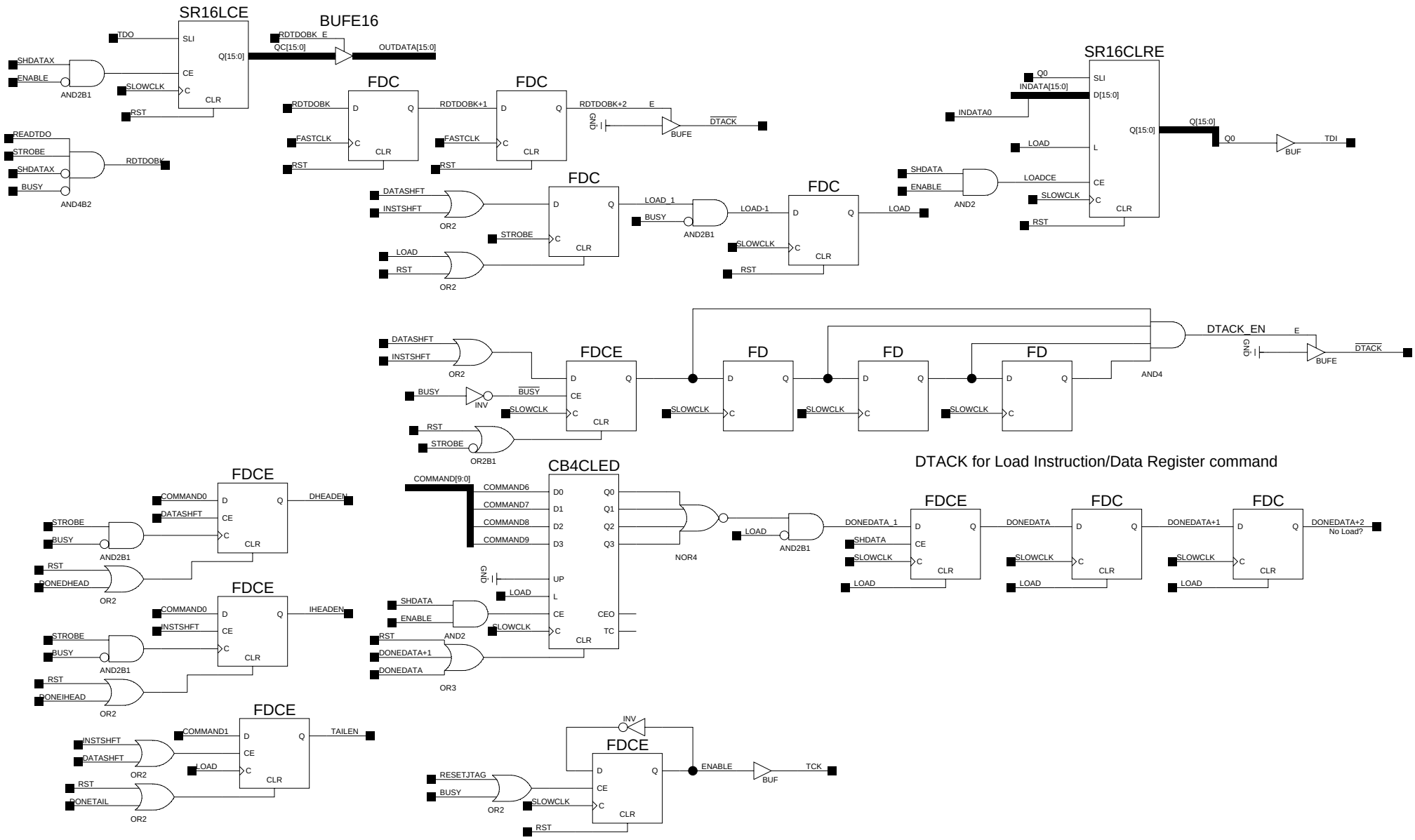
BY: JRG | PARENT PAGE: 2A | PROJECT: D785B
DATE: 1-10-2005_10:43 | FILE: COMMAND . 2 | PAGE: 3B



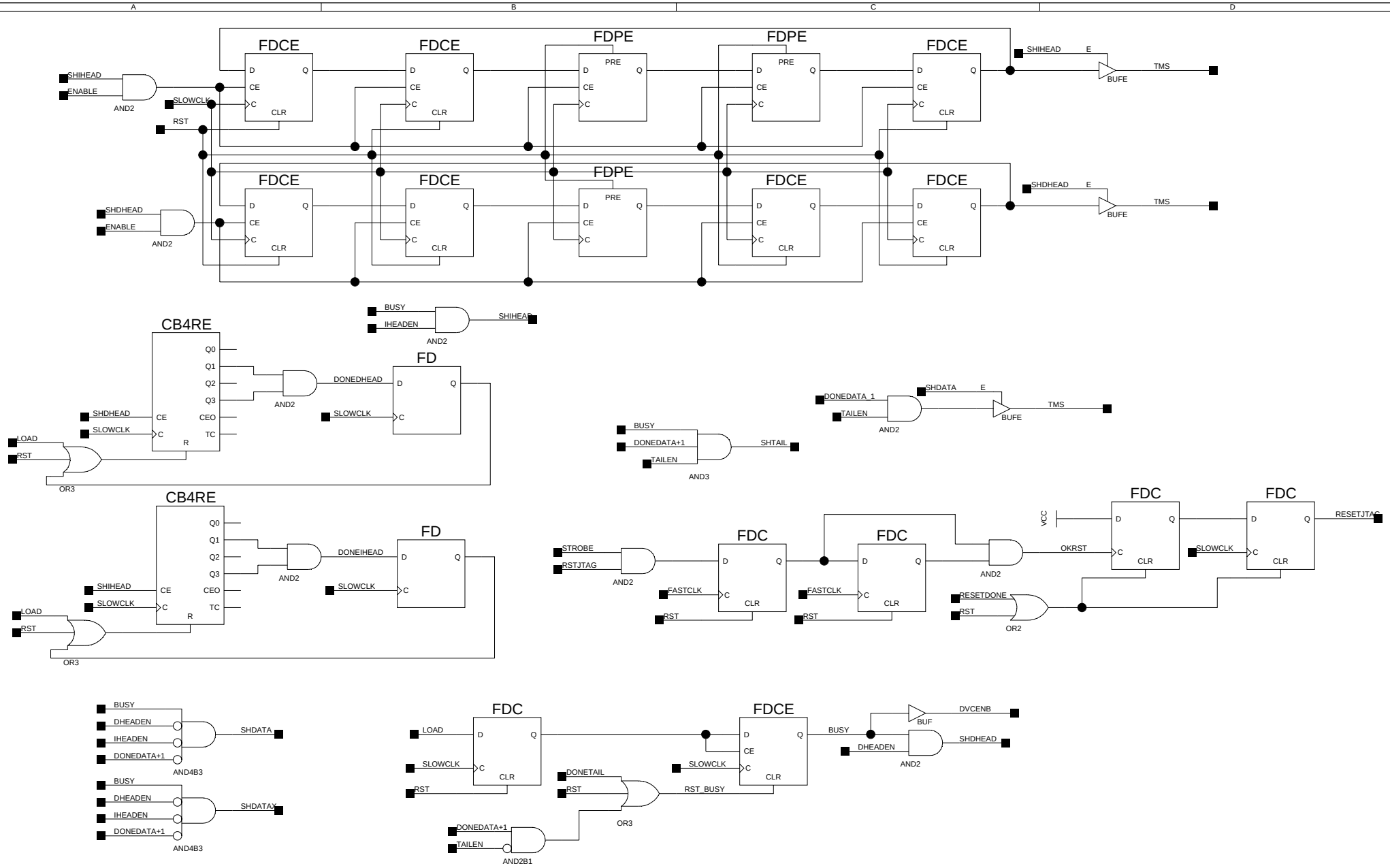




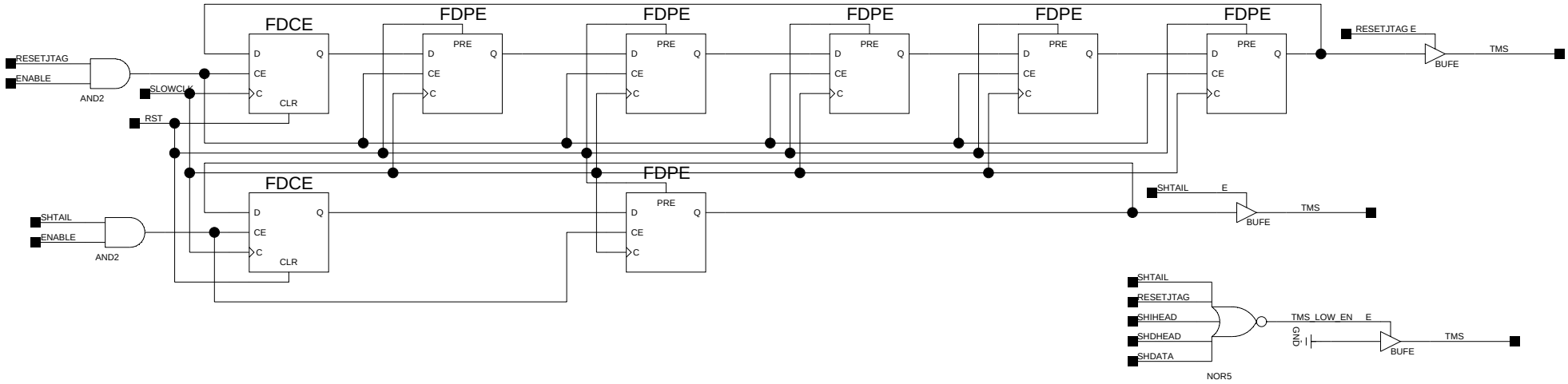
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME-Write Command Decoder DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2A	PROJECT: D785B
		DATE: 4-22-2004_7:48	FILE: COMMAND . 3	PAGE: 3C

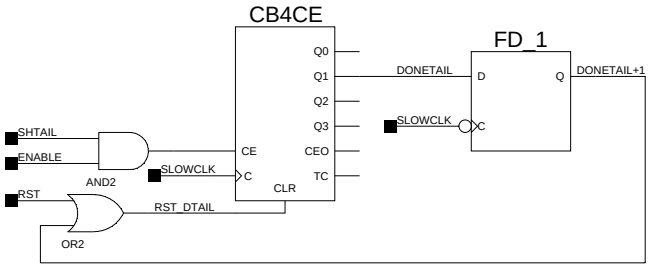


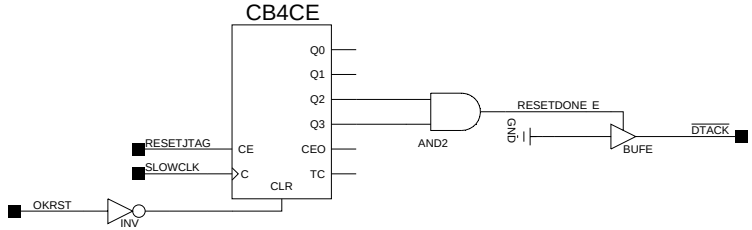
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785B
		DATE: 2-7-2005_9:32	FILE: VME-JTAG . 1	PAGE: 4A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785B
		DATE: 2-7-2005_9:32	FILE: VME-JTAG . 2	PAGE: 4B

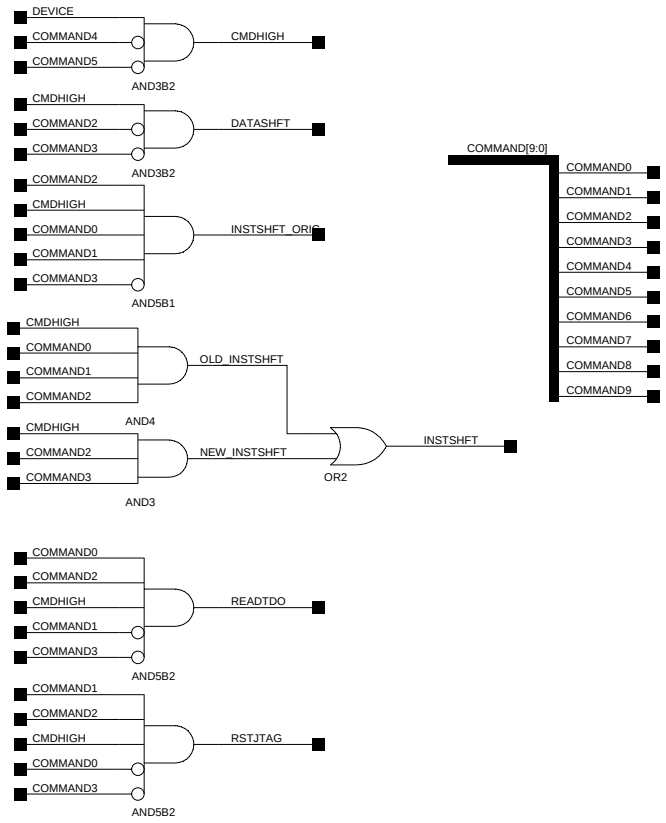






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 2-7-2005_9:32	PARENT PAGE: 2 FILE: VME-JTAG . 3
		PROJECT: D785B	PAGE: 4C

CFEB JTAG command decode



CFEB JTAG commands:

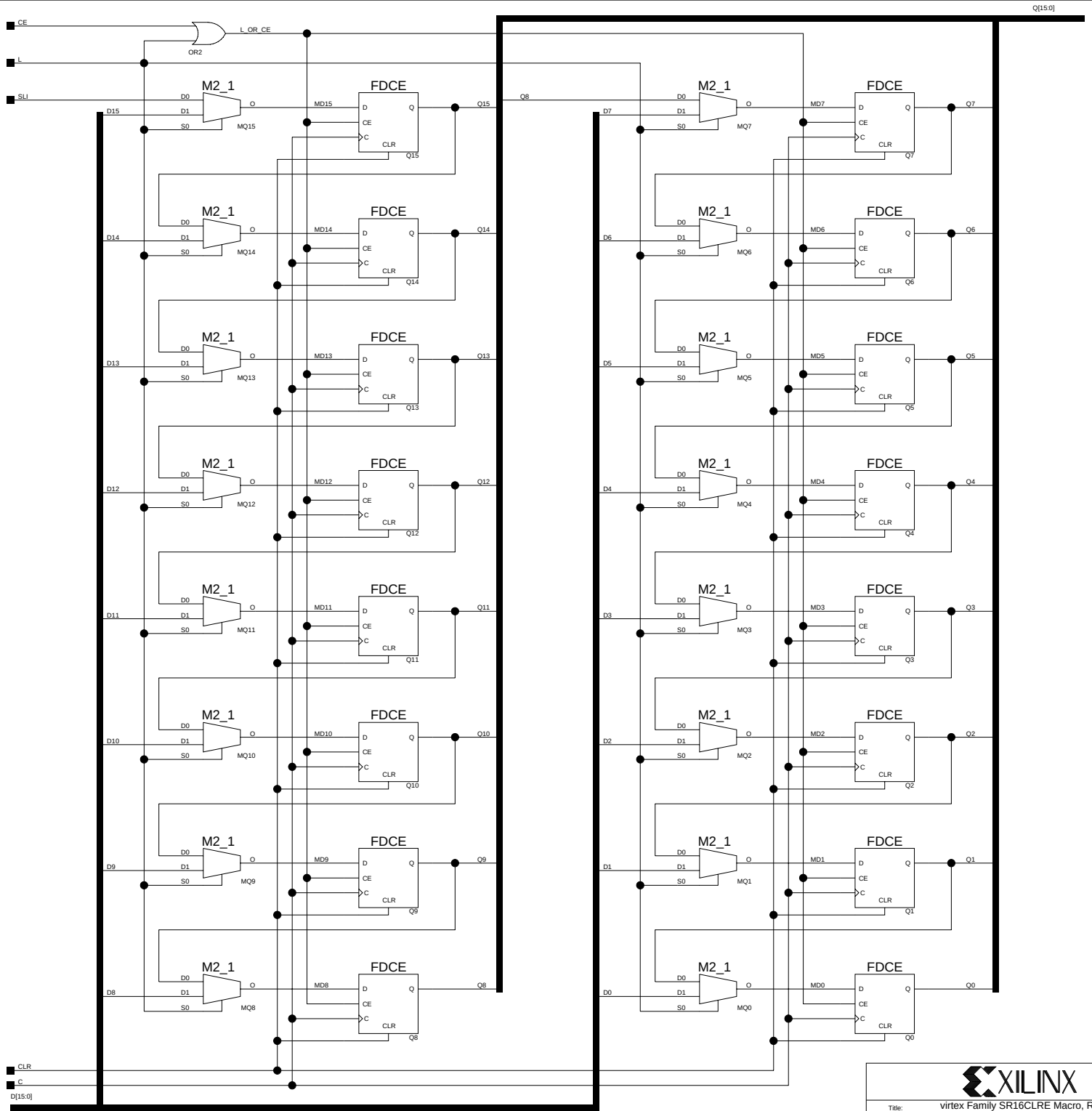
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register with header and tailer

0C || Shift IR, no header, no tailer
0D || Shift IR with header only
0E || Shift IR with tailer only
0F || Shift Instruction register with header and tailer

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: VME Interface-JTAG Converter
DDU VME Controller Logic
CMS CSC Electronics

BY: JRG | PARENT PAGE: 2 | PROJECT: D785B
DATE: 2-7-2005_9:32 | FILE: VME-JTAG . 4 | PAGE: 4D



drawn by KS

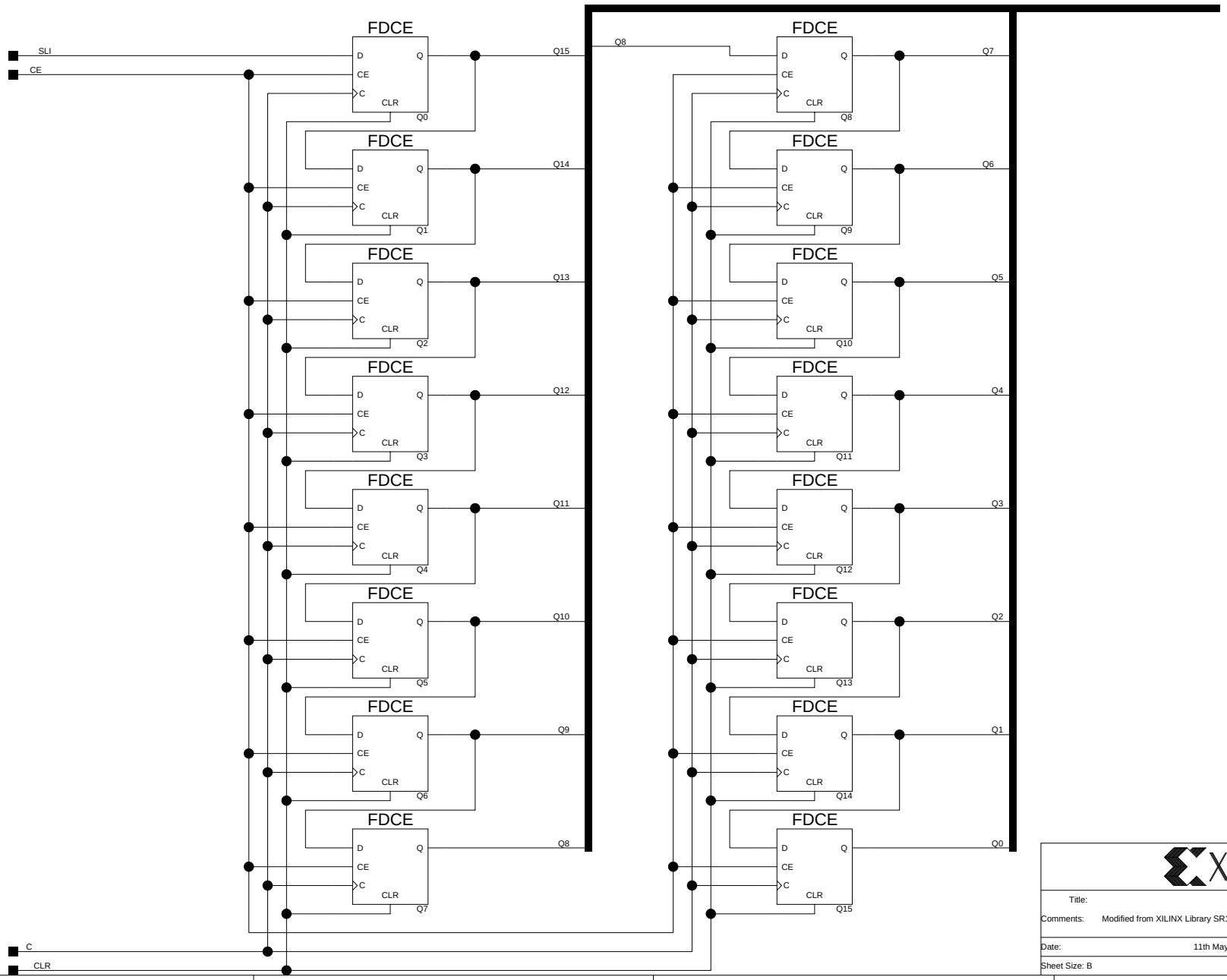
XILINX J. Gu

Title: virtex Family SR16CLRE Macro, Right Shift

Comments: 16-Bit Loadable Ser/Para-In, right shift
Para-Out Shift Reg w/ Enable & Async Clr

Date: 13th January 1993 | Ver: 1, Modified from XILINX, SR16CLE

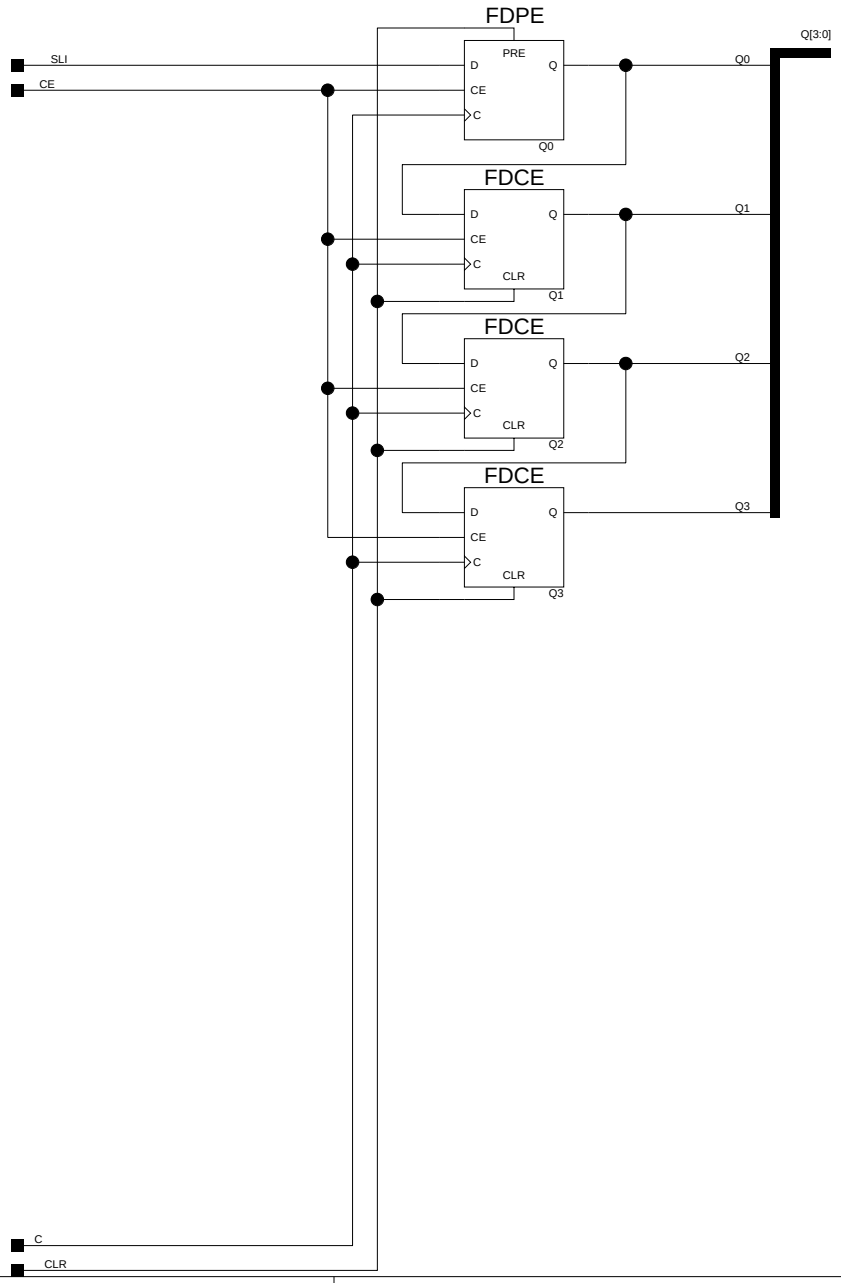
Sheet Size: C | Rev: A



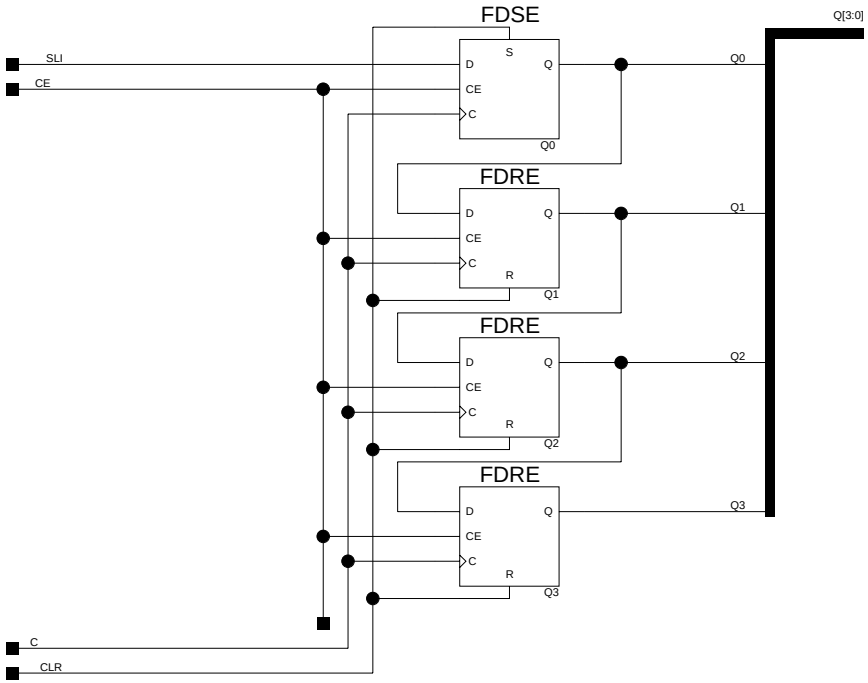
XILINX J. Gu

Title:	virtex Family SR16LCE Macro
Comments:	Modified from XILINX Library SR16CE, shift right 16-bit Serial-In Parallel-Out Shift Register w/ Enable and Async Clr
Date: 11th May 2001	Ver: 1
Sheet Size: B	Rev:

drawn by KS



Title:	VIRTEX Family SR4CE3 Macro (Set 1, Clear 3)	JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/Enable, 1 Preset & 3 Async Clr	
Date:	13th October 2003	Ver: 1
Sheet Size: B		Rev: A



drawn by KS

XILINX

Title: VIRTEX Family SR4RE Macro (SR4E_ONE)

Comments: 4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset

JRG

Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A