New Ideas:
Add new WEN I/O pin for SLINK
Store & check DMB source ID's from each fiber?
Decode serialized DMB status info
--> 6 full, 6 half, 8-bit count
--> deserialize sync check

D785C: DDU4CTRL (file 0dductrl)

2-2-2005_14:01
CF028A02 Version 28

CMS CSC DDU, Central Control FPGA

SWITCHES REVERSED ON BOARD
LED0 "on top"

v24: add DCC_STOP/SlinkWAIT logic
v25: locked 3 BUFGs, add KillCh serial load logic, add JTAG SoftRST on F33
---> It would be better to add FOK info to HDR3 rather than KillCh Mask...
...must come from InFPGA Hdr/Tr, maybe later?
v26: add debug for SD_LOAD on LEDmodes 11,7
v27: add DDU/C.D.F. CRC logic
v28: add VME_L1A, tune DDUCRC timing

Set 1 Bank to 3.3V I/O (bank 1)

PART=XC2VP7-6-FF672
PROM=2*XC18V04-VQ44 (PARALLEL)

D785C\ddu4_ctrl\ddu4ctrl

DDUCNTRL

RST_1=Asynchronus Reset for FPGA1 and ALL FIFOs
old-BXR Pulse: Dump Data Mode (no L1A needed)
Mode 1 Switch Block (reversed switch labels on board)
1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: Send FakeData (counter) on GBE link
7: Set L1A Fake mode
8: FPGA version on LEDs

VME Broadcast Addresses:
24=OSU-TCB "Test Control Board"
25=DMB
26=TMB
27=Both DMB and TMB
28=DDU
29=DCC

TST	Clock	BUFGMUX		
0P	drck1	5P	*4P	-TR
2P	2clk	5S	*1S	
3S	clk	7S	*7S	
0S	clk625	2S-	*2S	
7P	ck125	1P	*0S	-BL
5P	clk40	0S	*3P	
4S-	clk156	4S-	*4S	
1S	drck2	3P	*5S	
6S-	sclk	6S-	*6S	

* denotes LOCed position

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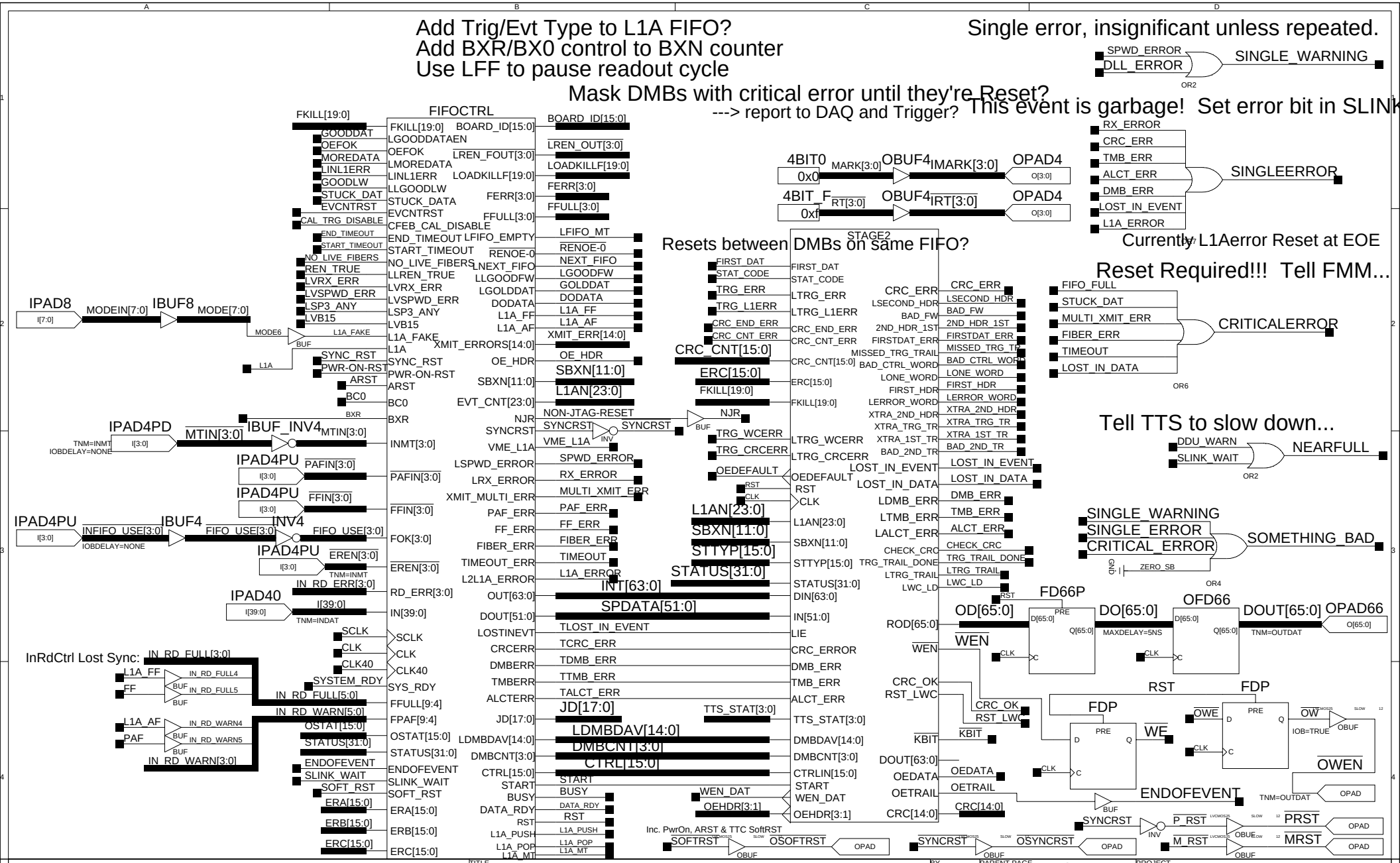
To Do:
- COMPARE L1NUM & BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Connect and drive FMM signals
  ---> Verify correct default state on board.
- DMB Monitor: Active-DAV mismatch warn, MOVLP bad evt, BXN match err
- Determine correct values to store in Flash Mem
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case

BOE1 type L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK
64-bit unique constant
H2: 0x/8000/0001/8000/8000
DDU Status Error DMB-DAV const DMBcnt
H3/T-1: 0x/SSSS.SSSS/ZZZZ/000Y
v40+
64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000
EOE WordCount CRCword EvtStat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUTK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount

mojo

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes


Add Trig/Evt Type to L1A FIFO?
Add BXR/BX0 control to BXN counter
Use LFF to pause readout cycle
Mask DMBs with critical error until they're Reset?
---> report to DAQ and Trigger?
Single error, insignificant unless repeated.
SPWD_ERROR
DLL_ERROR
OR2
SINGLE_WARNING
This event is garbage! Set error bit in SLINK
RX_ERROR
CRC_ERR
TMB_ERR
ALCT_ERR
DMB_ERR
LOST_IN_EVENT
L1A_ERROR
SINGLEERROR
Currently L1Aerror Reset at EOE
Reset Required!!! Tell FMM...
FIFO_FULL
STUCK_DAT
MULTI_XMIT_ERR
FIBER_ERR
TIMEOUT
LOST_IN_DATA
OR6
CRITICALERROR
Tell TTS to slow down...
DDU_WARN
SLINK_WAIT
OR2
NEARFULL
SINGLE_WARNING
SINGLE_ERROR
CRITICAL_ERROR
OR4
SOMETHING_BAD
ZERO_SB
FIFOCTRL
STAGE2
Resets between DMBs on same FIFO?
4BIT0
0x0
MARK[3:0]
OBUF4
IMARK[3:0]
OPAD4
4BIT_F
0xf
RT[3:0]
IRT[3:0]
IPAD8
MODEIN[7:0]
IBUF8
MODE[7:0]
MODE6
L1A_FAKE
L1A
IPAD4PD
MTIN[3:0]
IBUF_INV4
IPAD4PU
PAFIN[3:0]
FFIN[3:0]
IPAD4PU
INFIFO_USE[3:0]
IBUF4
FIFO_USE[3:0]
INV4
FOK[3:0]
IPAD4PU
EREN[3:0]
IPAD40
I[39:0]
TNM=INDAT
IN_RD_ERR[3:0]
RD_ERR[3:0]
IN[39:0]
SCLK
CLK
CLK40
SYSTEM_RDY
SYS_RDY
InRdCtrl Lost Sync:
IN_RD_FULL[3:0]
L1A_FF
FF
IN_RD_FULL4
IN_RD_FULL5
BUF
IN_RD_FULL[5:0]
FFULL[9:4]
IN_RD_WARN[5:0]
L1A_AF
PAF
IN_RD_WARN4
IN_RD_WARN5
FPAF[9:4]
OSTAT[15:0]
STATUS[31:0]
ENDOFEVENT
SLINK_WAIT
SOFT_RST
ERA[15:0]
ERB[15:0]
ERC[15:0]
FKILL[19:0]
GOODDAT
OEFOK
MOREDATA
LINL1ERR
GOODLW
STUCK_DAT
EVCNTRST
CAL_TRG_DISABLE
END_TIMEOUT
START_TIMEOUT
NO_LIVE_FIBERS
REN_TRUE
LVRX_ERR
LVSPWD_ERR
LSP3_ANY
LVB15
L1A_FAKE
L1A
SYNC_RST
PWR-ON-RST
ARST
BC0
BXR
INMT[3:0]
LGOODDATAEN
LMOREDATA
LLGOODLW
STUCK_DATA
CFEB_CAL_DISABLE
LLREN_TRUE
LVRX_ERR
LVSPWD_ERR
LSP3_ANY
LVB15
XMIT_ERRORS[14:0]
BOARD_ID[15:0]
LREN_FOUT[3:0]
LOADKILLF[19:0]
FERR[3:0]
FFULL[3:0]
LFIFO_EMPTY
LNEXT_FIFO
LLGOODFW
LGOLDDAT
DODATA
L1A_FF
L1A_AF
OE_HDR
SBXN[11:0]
EVT_CNT[23:0]
NON-JTAG-RESET
SYNCRST
INV
VME_L1A
LSPWD_ERROR
LRX_ERROR
XMIT_MULTI_ERR
PAF_ERR
FF_ERR
FIBER_ERR
TIMEOUT_ERR
L2L1A_ERROR
OUT[63:0]
DOUT[51:0]
LOSTINEVT
TCRC_ERR
TDMB_ERR
TTMB_ERR
TALCT_ERR
JD[17:0]
LDMBDAV[14:0]
DMBCNT[3:0]
CTRL[15:0]
START
BUSY
DATA_RDY
RST
L1A_PUSH
L1A_POP
L1A_MT
LOADKILLF[19:0]
LREN_OUT[3:0]
RENOE-0
NJR
BUF
L1AN[23:0]
INT[63:0]
SPDATA[51:0]
STATUS[31:0]
STTYP[15:0]
TRG_WCERR
TRG_CRCERR
OEDEFAULT
CRC_CNT[15:0]
ERC[15:0]
FKILL[19:0]
FIRST_DAT
STAT_CODE
TRG_ERR
TRG_L1ERR
CRC_END_ERR
CRC_CNT_ERR
TTS_STAT[3:0]
WEN_DAT
OEHDR[3:1]
LTRG_ERR
LTRG_L1ERR
LTRG_WCERR
LTRG_CRCERR
LSECOND_HDR
BAD_FW
2ND_HDR_1ST
FIRSTDAT_ERR
MISSED_TRG_TRAIL
BAD_CTRL_WORD
LONE_WORD
FIRST_HDR
LERROR_WORD
XTRA_2ND_HDR
XTRA_TRG_TR
XTRA_1ST_TR
BAD_2ND_TR
LOST_IN_EVENT
LOST_IN_DATA
DMB_ERR
TMB_ERR
ALCT_ERR
LALCT_ERR
CHECK_CRC
TRG_TRAIL_DONE
LTRG_TRAIL
LWC_LD
RST
CLK
LIE
CRC_ERROR
DMB_ERR
TMB_ERR
ALCT_ERR
DIN[63:0]
IN[51:0]
ROD[65:0]
WEN
CRC_OK
RST_LWC
KBIT
DOUT[63:0]
OEDATA
OETRAIL
CRC[14:0]
FD66P
OD[65:0]
DO[65:0]
MAXDELAY=5NS
OFD66
DOUT[65:0]
OPAD66
TNM=OUTDAT
FDP
RST
OWE
OW
IOB=TRUE
OBUF
OWEN
OPAD
ENDOFEVENT
SYNCRST
P_RST
PRST
M_RST
MRST
Inc. PwrOn, ARST & TTC SoftRST
SOFTRST
OSOFTRST
OSYNCRST
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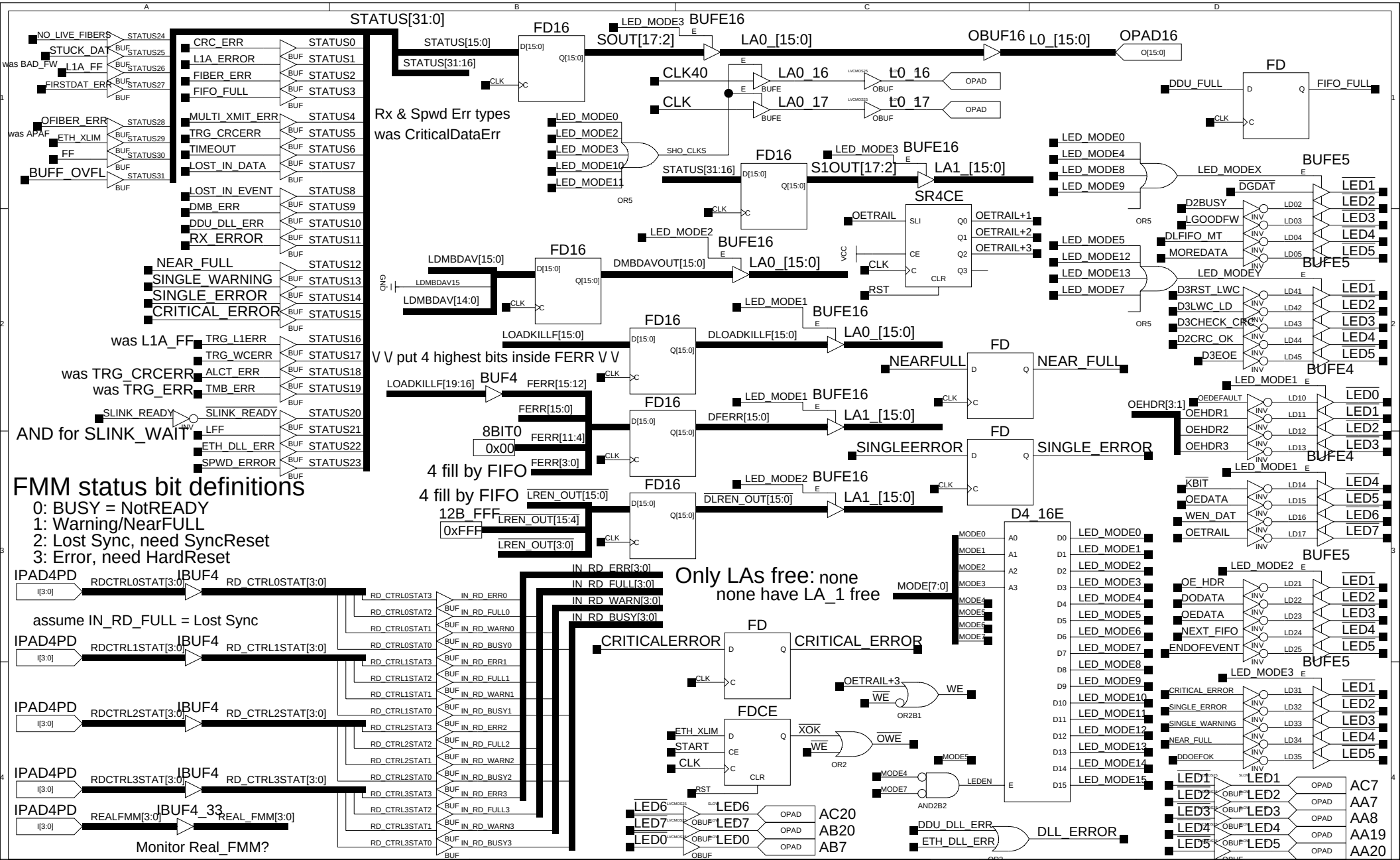
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
DDU Control
DDU Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
1
PROJECT
D785C
DATE
1-26-2005_12:28
FILE
DDUCNTRL . 1
PAGE
2


STATUS[31:0]
NO_LIVE_FIBERS
STUCK_DAT
was BAD_FW
L1A_FF
FIRSTDAT_ERR
OFIBER_ERR
was APAF
ETH_XLIM
FF
BUFF_OVFL
CRC_ERR
L1A_ERROR
FIBER_ERR
FIFO_FULL
MULTI_XMIT_ERR
TRG_CRCERR
TIMEOUT
LOST_IN_DATA
LOST_IN_EVENT
DMB_ERR
DDU_DLL_ERR
RX_ERROR
NEAR_FULL
SINGLE_WARNING
SINGLE_ERROR
CRITICAL_ERROR
was L1A_FF
was TRG_CRCERR
was TRG_ERR
TRG_L1ERR
TRG_WCERR
ALCT_ERR
TMB_ERR
SLINK_READY
AND for SLINK_WAIT
LFF
ETH_DLL_ERR
SPWD_ERROR
STATUS[15:0]
STATUS[31:16]
FD16
LED_MODE3
BUFE16
SOUT[17:2]
LA0_[15:0]
OBUF16
L0_[15:0]
OPAD16
CLK40
CLK
LA0_16
LA0_17
L0_16
L0_17
Rx & Spwd Err types
was CriticalDataErr
LED_MODE0
LED_MODE2
LED_MODE3
LED_MODE10
LED_MODE11
OR5
SHO_CLKS
S1OUT[17:2]
LA1_[15:0]
SR4CE
OETRAIL
OETRAIL+1
OETRAIL+2
OETRAIL+3
LED_MODE4
LED_MODE8
LED_MODE9
LED_MODE5
LED_MODE12
LED_MODE13
LED_MODE7
LED_MODEX
LED_MODEY
BUFE5
DGDAT
D2BUSY
LGOODFW
DLFIFO_MT
MOREDATA
D3RST_LWC
D3LWC_LD
D3CHECK_CRC
D2CRC_OK
D3EOE
LED1
LED2
LED3
LED4
LED5
LDMBDAV[15:0]
LDMBDAV15
LDMBDAV[14:0]
DMBDAVOUT[15:0]
LED_MODE2
LED_MODE1
LOADKILLF[15:0]
DLOADKILLF[15:0]
NEARFULL
NEAR_FULL
FD
DDU_FULL
FIFO_FULL
LOADKILLF[19:16]
BUF4
FERR[15:12]
FERR[15:0]
FERR[11:4]
FERR[3:0]
8BIT0
0x00
4 fill by FIFO
DFERR[15:0]
SINGLEERROR
SINGLE_ERROR
LREN_OUT[15:0]
LREN_OUT[15:4]
LREN_OUT[3:0]
12B_FFF
0xFFF
DLREN_OUT[15:0]
BUFE4
OEHDR[3:1]
OEDEFAULT
OEHDR1
OEHDR2
OEHDR3
KBIT
OEDATA
WEN_DAT
OETRAIL
OE_HDR
DODATA
OEDATA
NEXT_FIFO
ENDOFEVENT
LED0
LED6
LED7
V V put 4 highest bits inside FERR V V
FMM status bit definitions
0: BUSY = NotREADY
1: Warning/NearFULL
2: Lost Sync, need SyncReset
3: Error, need HardReset
IPAD4PD
IBUF4
RDCTRL0STAT[3:0]
RD_CTRL0STAT[3:0]
assume IN_RD_FULL = Lost Sync
RDCTRL1STAT[3:0]
RD_CTRL1STAT[3:0]
RDCTRL2STAT[3:0]
RD_CTRL2STAT[3:0]
RDCTRL3STAT[3:0]
RD_CTRL3STAT[3:0]
IBUF4_33
REALFMM[3:0]
REAL_FMM[3:0]
Monitor Real_FMM?
IN_RD_ERR[3:0]
IN_RD_FULL[3:0]
IN_RD_WARN[3:0]
IN_RD_BUSY[3:0]
Only LAs free: none
none have LA_1 free
CRITICALERROR
CRITICAL_ERROR
OETRAIL+3
WE
OR2B1
FDCE
ETH_XLIM
START
CLK
XOK
OWE
OR2
MODE[7:0]
MODE4
MODE7
AND2B2
LEDEN
D4_16E
DDU_DLL_ERR
ETH_DLL_ERR
DLL_ERROR
AC20
AB20
AB7
AC7
AA7
AA8
AA19
AA20
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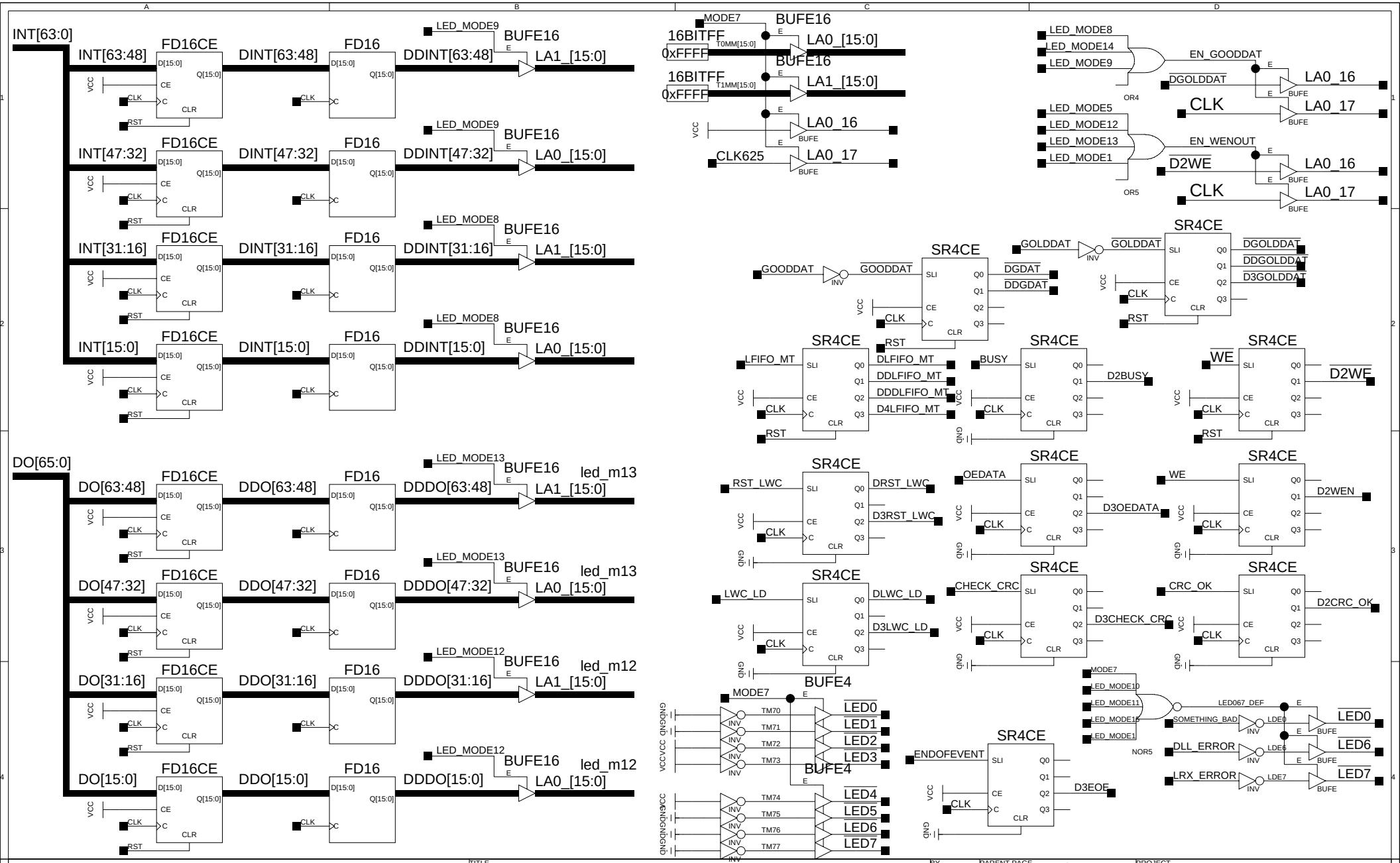
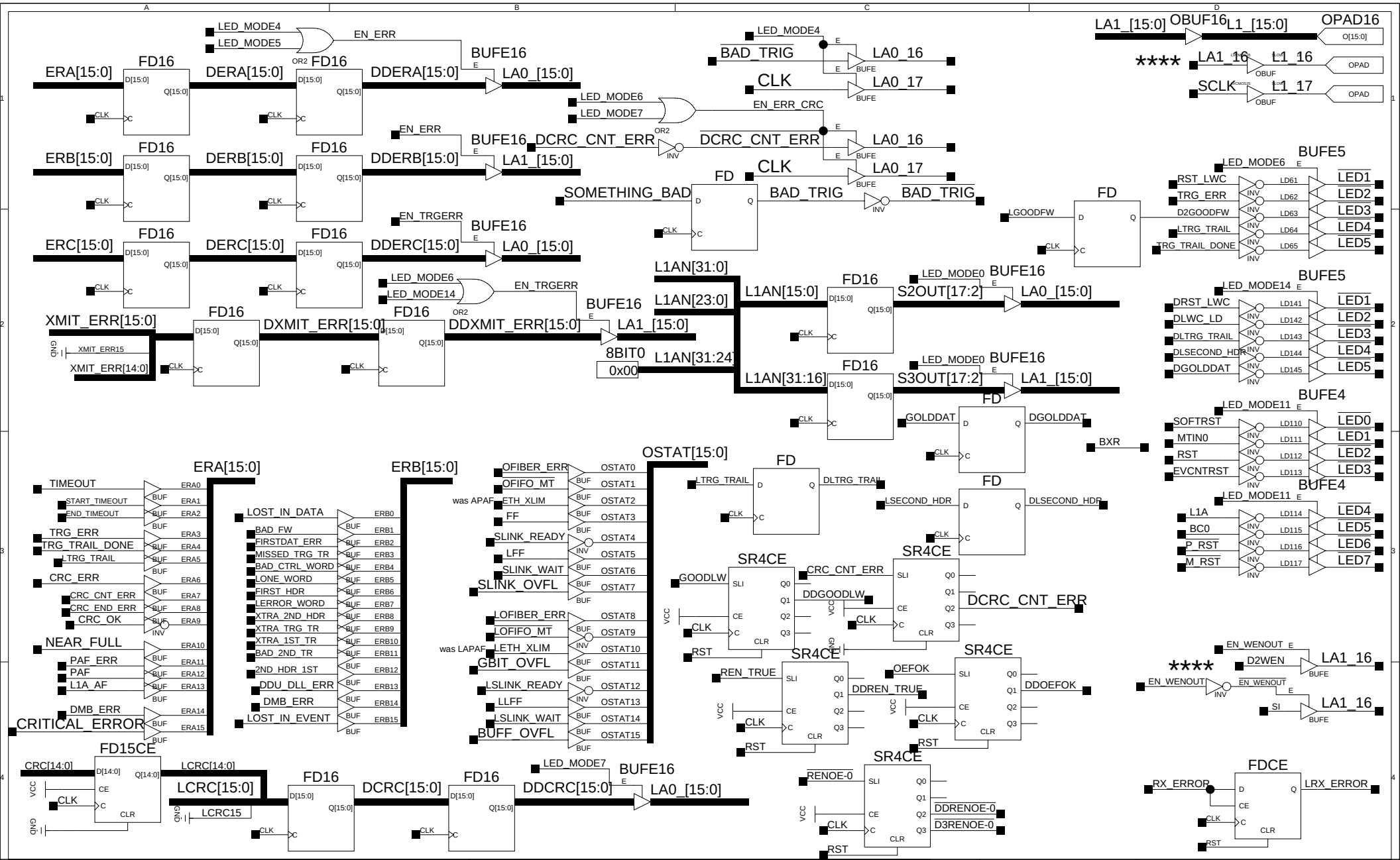
TITLE
DDU Control
DDU Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
1
PROJECT
D785C
DATE
1-24-2005_13:51
FILE
DDUCNTRL . 2
PAGE
2A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Control DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 1	PROJECT D785C
		DATE 1-24-2005_12:04	FILE DDUCNTRL . 3	PAGE 2B



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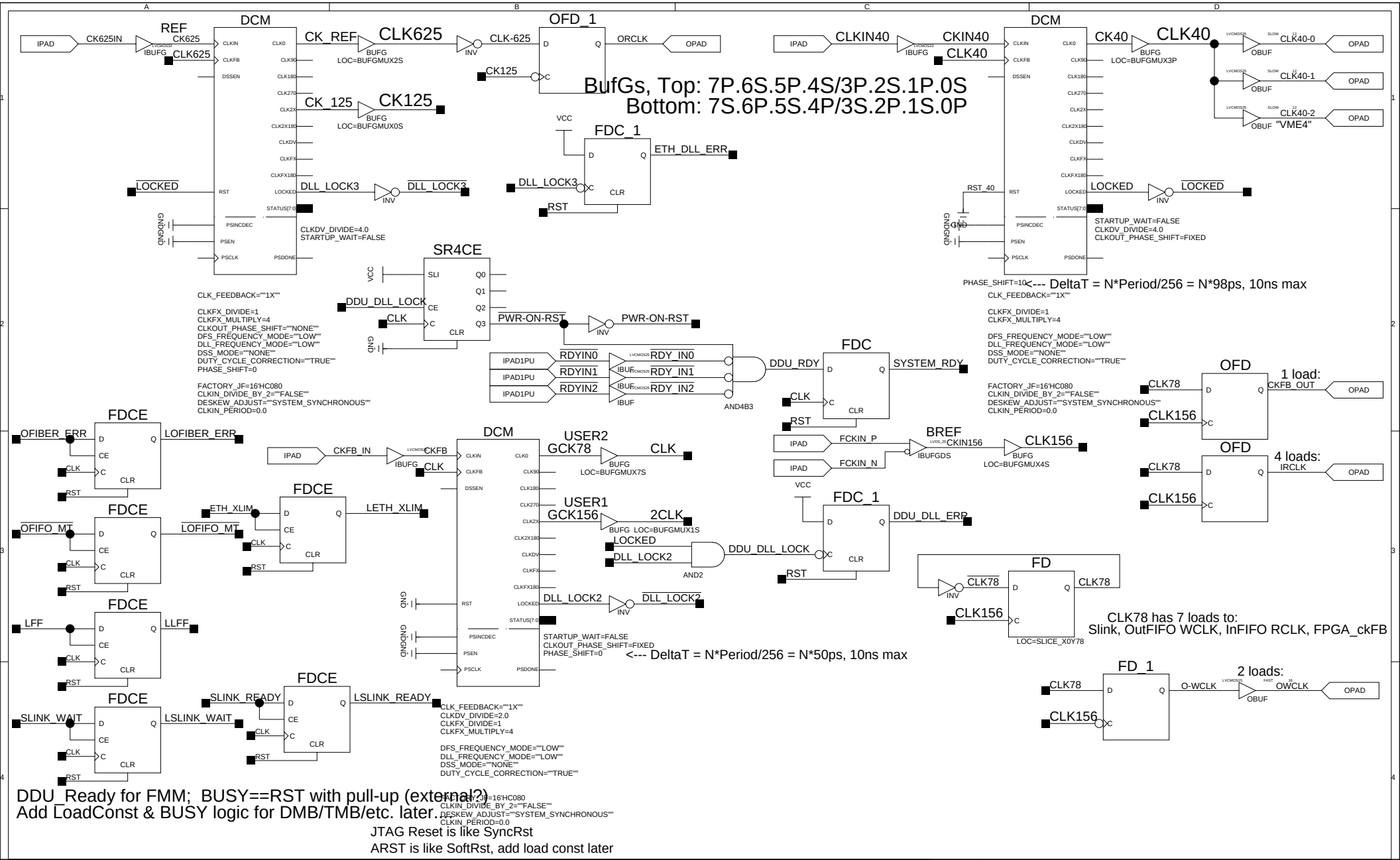

DDU_Ready for FMM; BUSY==RST with pull-up (external?)
Add LoadConst & BUSY logic for DMB/TMB/etc. later.

JTAG Reset is like SyncRst
ARST is like SoftRst, add load const later

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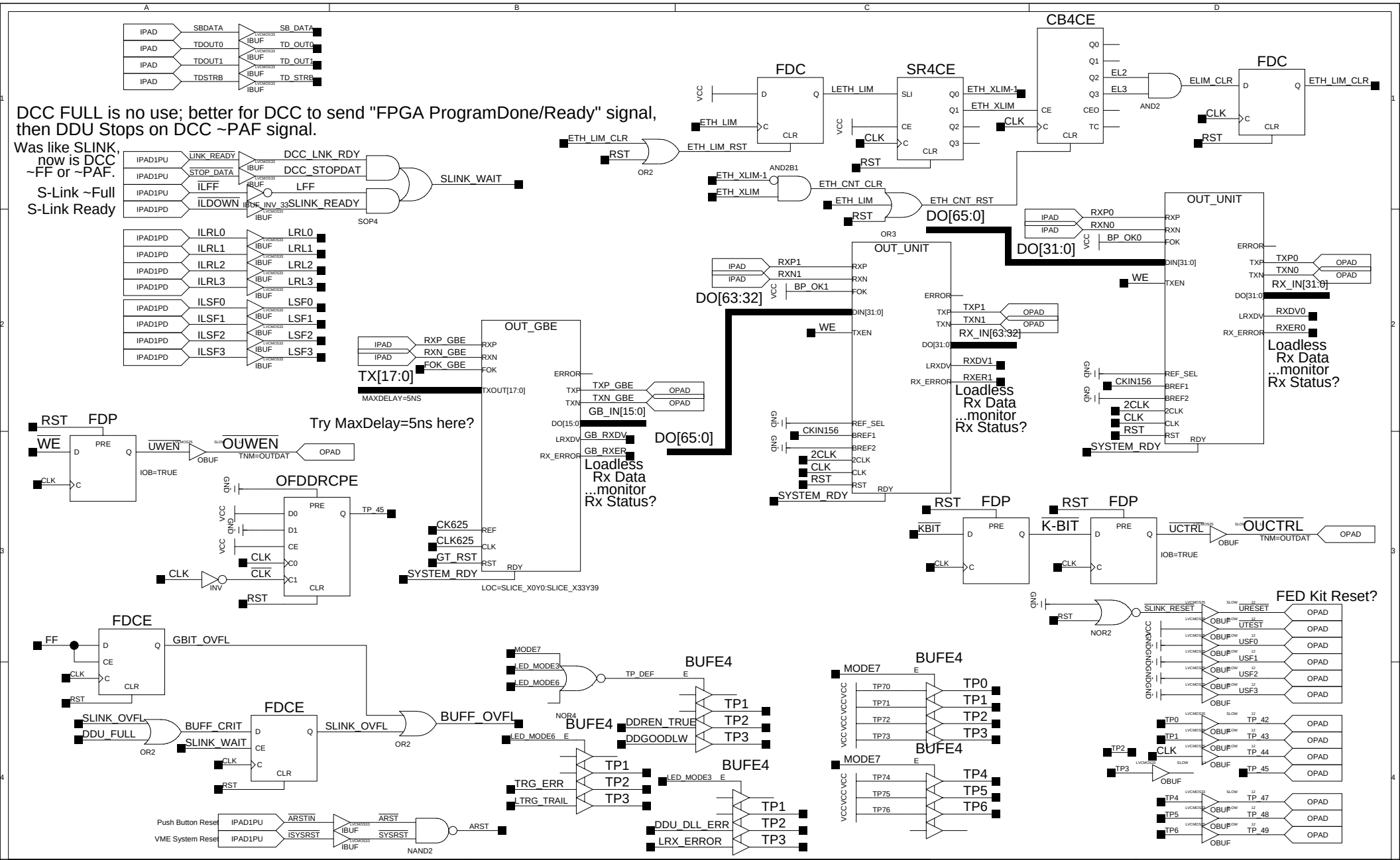
		DATE 1-14-2005_16:24		FILE DDUCNTRL . 5	PAGE 2D


DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal, then DDU Stops on DCC ~PAF signal.
Was like SLINK, now is DCC ~FF or ~PAF.
S-Link ~Full
S-Link Ready
Try MaxDelay=5ns here?
Loadless Rx Data ...monitor Rx Status?
FED Kit Reset?
TX[17:0]
MAXDELAY=5NS
DO[65:0]
DO[63:32]
DO[31:0]
LOC=SLICE_X0Y0:SLICE_X33Y39
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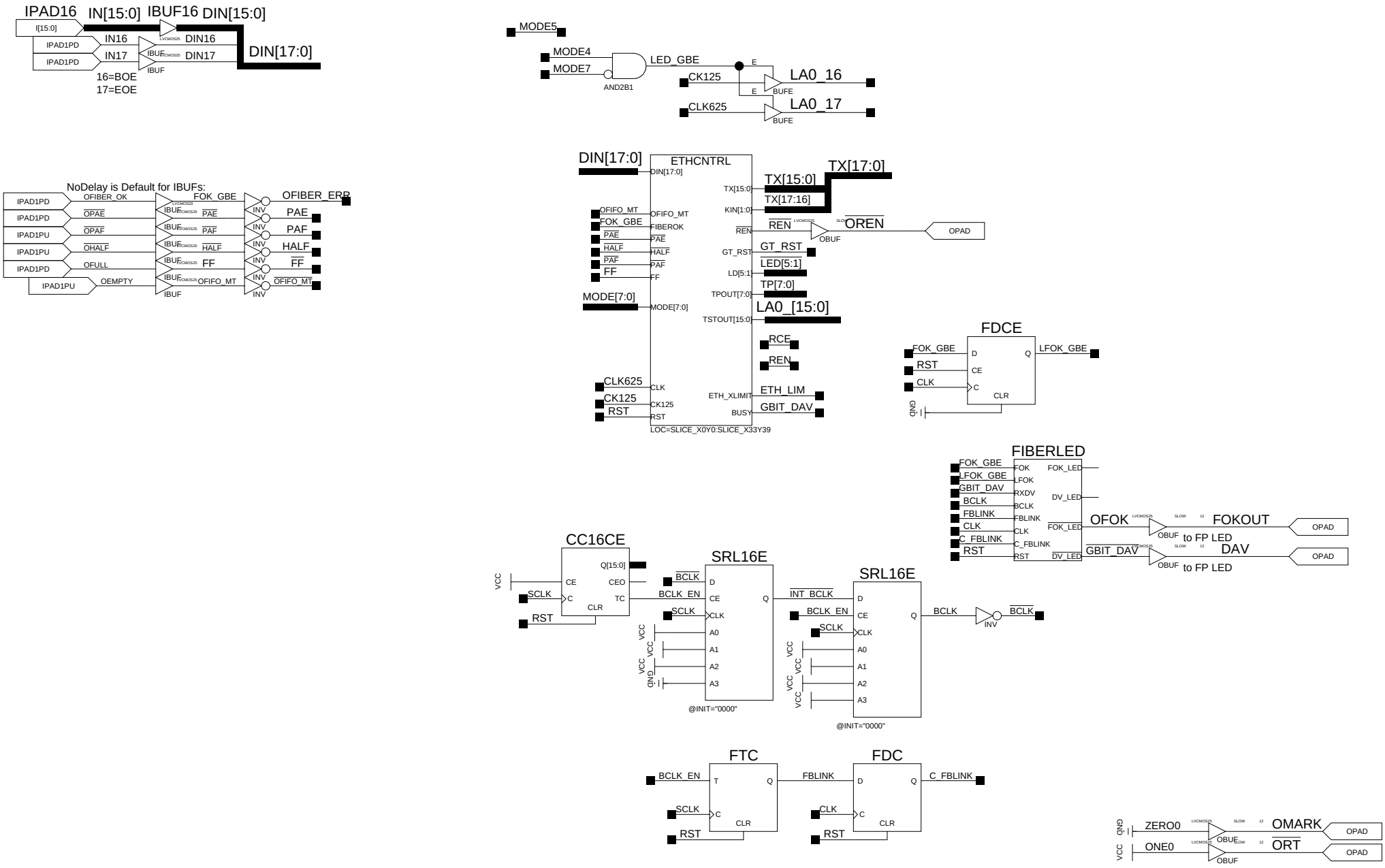
DDU Control
DDU Controller Logic
CMS CSC Electronics
JRG
1
D785C
1-26-2005_10:32
DDUCNTRL . 6
2E



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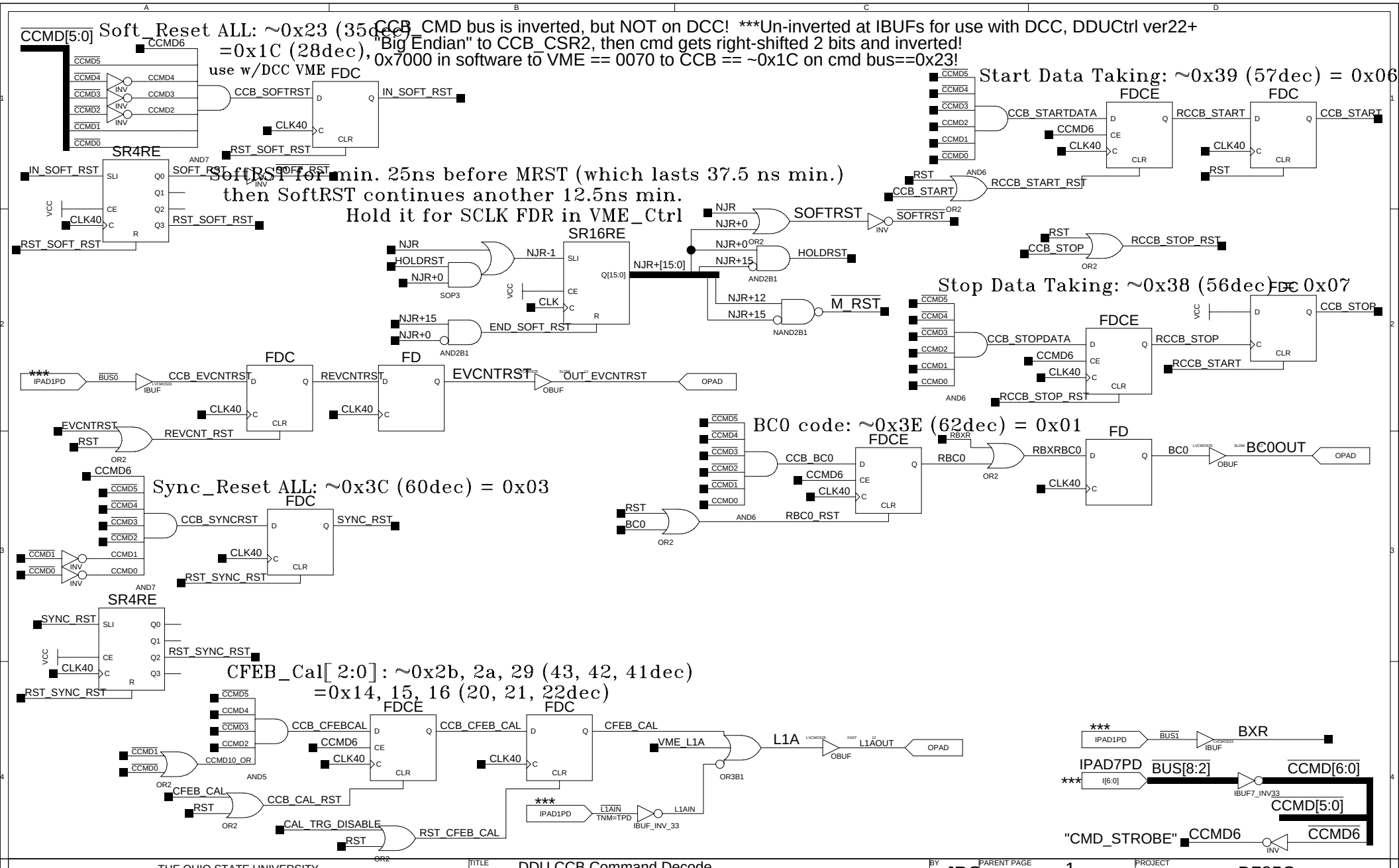
		PROJECT: D785C	PAGE: 2F


CCMD[5:0]
Soft_Reset ALL: ~0x23 (35dec) =0x1C (28dec), use w/DCC VME
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
"Big Endian" to CCB_CSR2, then cmd gets right-shifted 2 bits and inverted!
0x7000 in software to VME == 0070 to CCB == ~0x1C on cmd bus==0x23!
CCB_SOFTRST
IN_SOFT_RST
RST_SOFT_RST
SOFT_RST
SoftRST for min. 25ns before MRST (which lasts 37.5 ns min.)
then SoftRST continues another 12.5ns min.
Hold it for SCLK FDR in VME_Ctrl
Start Data Taking: ~0x39 (57dec) = 0x06
CCB_STARTDATA
RCCB_START
CCB_START
RCCB_START_RST
Stop Data Taking: ~0x38 (56dec) = 0x07
CCB_STOPDATA
RCCB_STOP
CCB_STOP
RCCB_STOP_RST
SOFTRST
HOLDRST
M_RST
END_SOFT_RST
EVCNTRST
REVCNTRST
REVCNT_RST
OUT_EVCNTRST
BC0 code: ~0x3E (62dec) = 0x01
CCB_BC0
RBC0
RBXRBC0
BC0OUT
RBC0_RST
Sync_Reset ALL: ~0x3C (60dec) = 0x03
CCB_SYNCRST
SYNC_RST
RST_SYNC_RST
CFEB_Cal[2:0]: ~0x2b, 2a, 29 (43, 42, 41dec)
=0x14, 15, 16 (20, 21, 22dec)
CCB_CFEBCAL
CCB_CFEB_CAL
CFEB_CAL
VME_L1A
L1A
L1AOUT
CCB_CAL_RST
CAL_TRG_DISABLE
RST_CFEB_CAL
BXR
IPAD7PD
BUS[8:2]
CCMD[6:0]
CCMD[5:0]
"CMD_STROBE"
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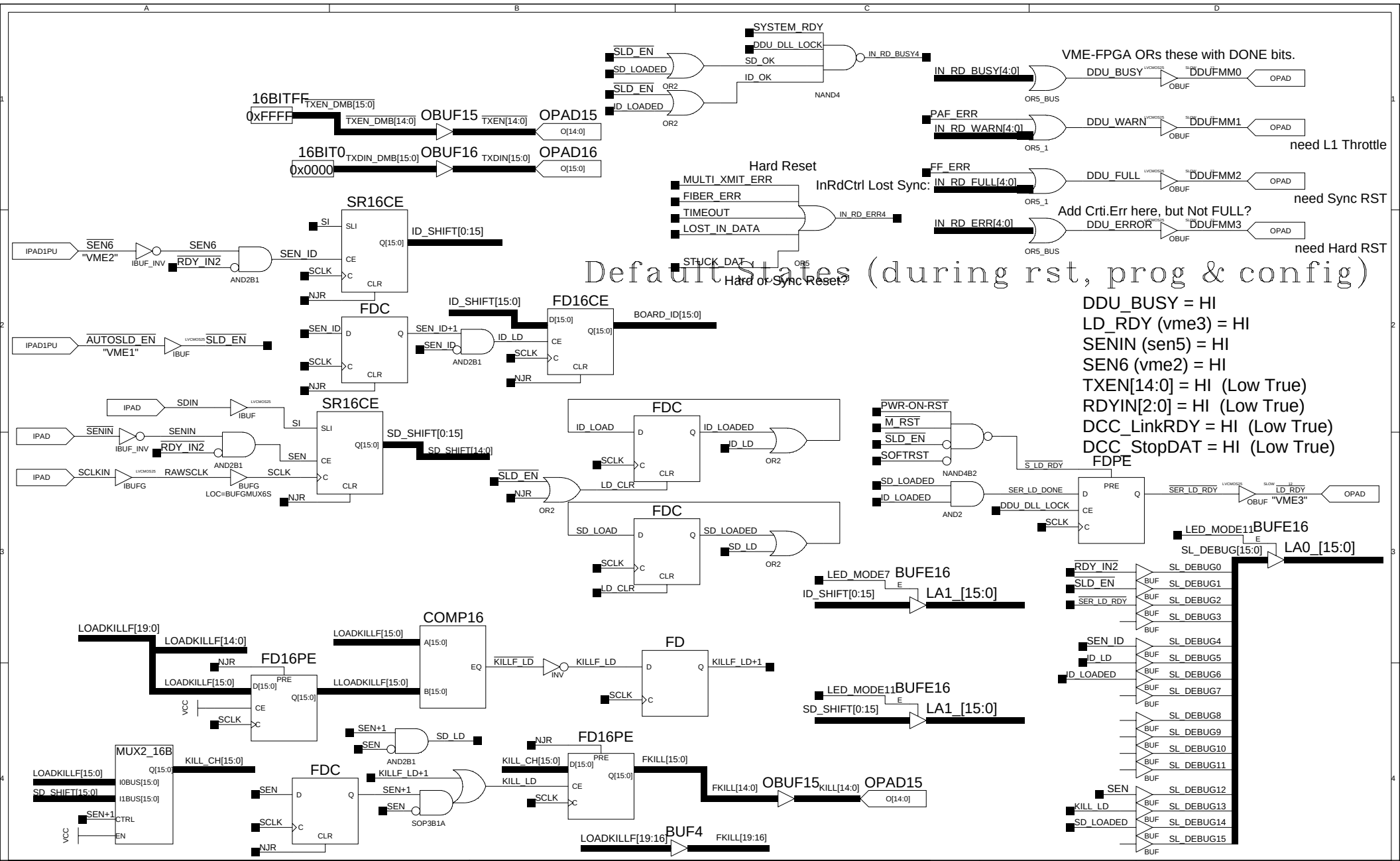
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
DDU CCB Command Decode
DDU Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 1
PROJECT D785C
DATE 1-26-2005_10:27
FILE DDUCNTRL . 8
PAGE 2G



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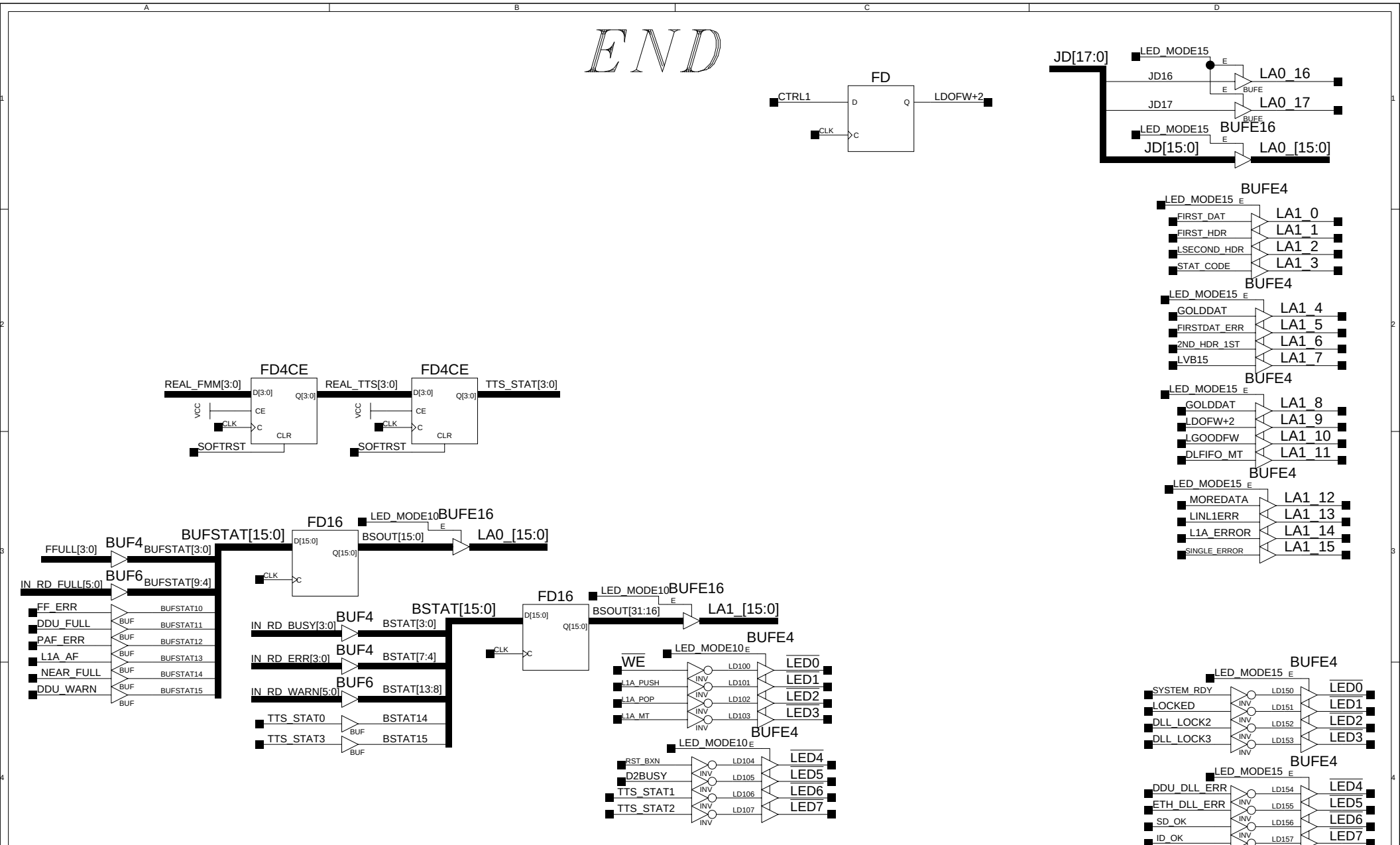

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		PROJECT: D785C	PAGE: 2I

CLK/\ -- IN[39:0] -- CLK\/ -- RDAT[39:0] IN[79:40] -- CLK/\ -- RDAT[79:40] DAT[39:0]

Use these busses for CFEB CRC and Special Word checks-->>

DAT[79:0]

4 * 13-bit SCA data bus

Use NEW DMB logic here (old L1AN was [51:40] & [31:20])

Lowest 5 RDAT bytes synched to falling edge of CLK

(next-to-last word bits) come with E-codes of last DMB only, followed by C-codes

"FILL Flag"

LFIFO_EMPTY TRUE means next DAT word is not GoldDat

~EREN/Echo_REN true says there is fresh data on the bus, timed to LFIFO_MT false

synched w/DoFW+1,2

Like LREN_TRUE.and.FIFOnotEMPTY?

FEND appears at end:
sometimes
always
never
never

set for first 2 E-codes from each DMB

should be always zero

synched w/GoodDat

Valid E-Code detected

(exclude DMB_Err case?)

DMB_END=DMBEND

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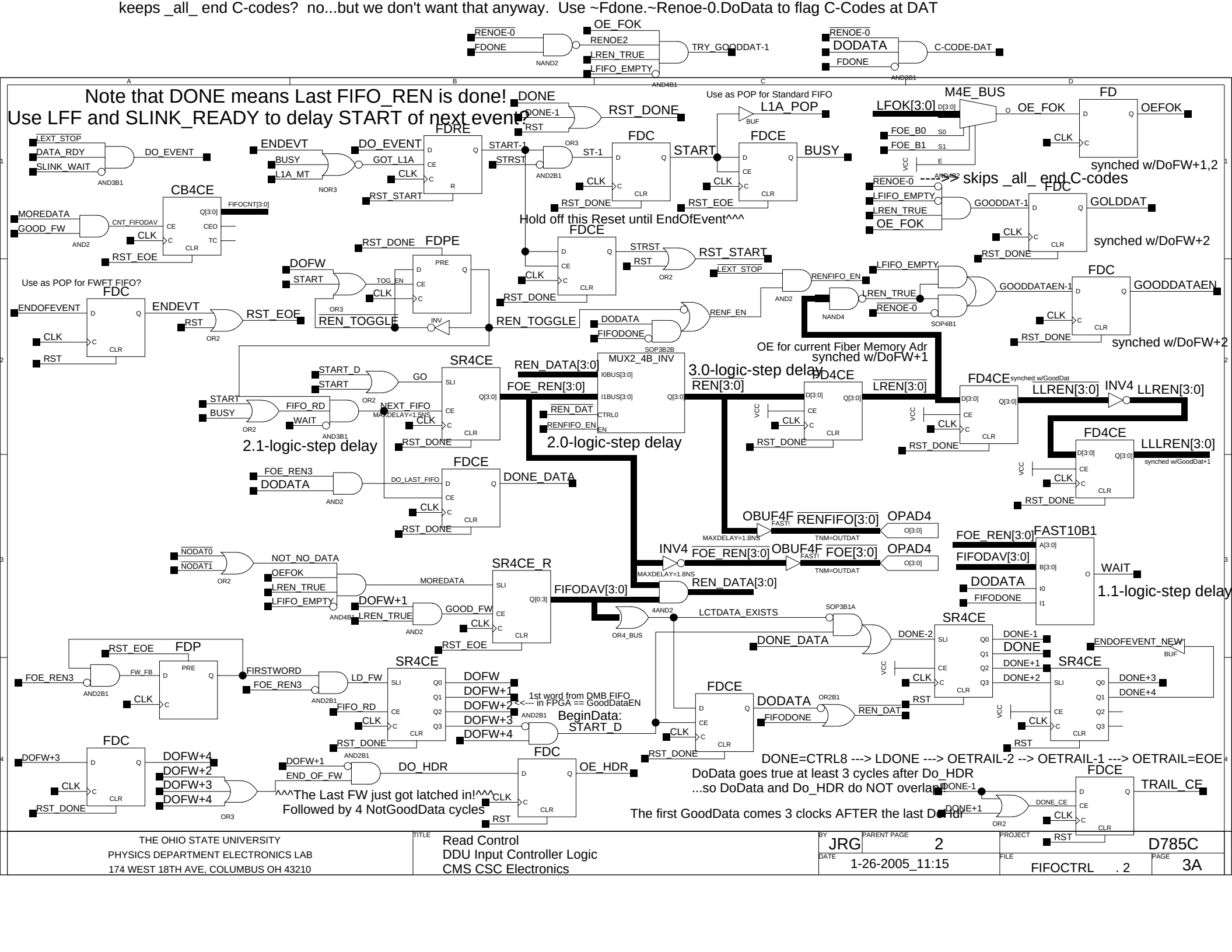
TITLE: DDU Input FIFO Control
DDU Controller
CMS CSC Electronics

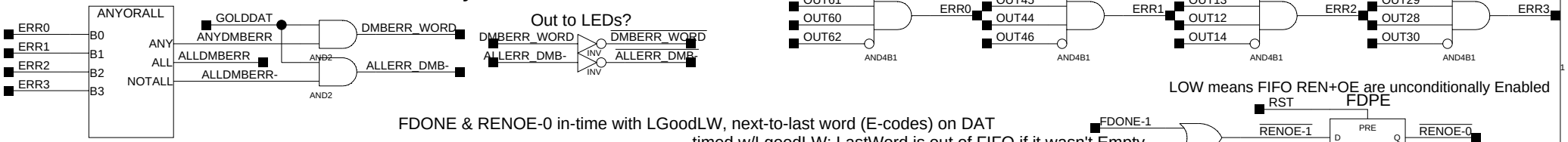
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
1-27-2005_10:57	FIFOCTRL . 1	3

keeps _all_ end C-codes? no...but we don't want that anyway. Use ~Fdone.~Renoe-0.DoData to flag C-Codes at DAT



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:15	PARENT PAGE: 2 PROJECT: D785C FILE: FIFOCTRL . 2 PAGE: 3A

Check for DMB Error Word and consistency:

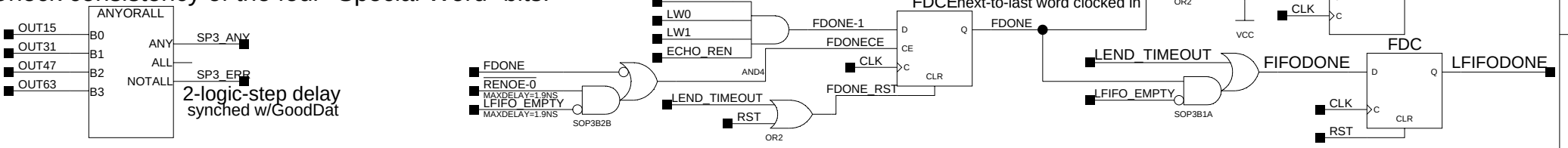


LOW means FIFO REN+OE are unconditionally Enabled

FDONE & RENOE-0 in-time with LGoodLW, next-to-last word (E-codes) on DAT

timed w/LgoodLW; LastWord is out of FIFO if it wasn't Empty

Check consistency of the four "Special Word" bits:

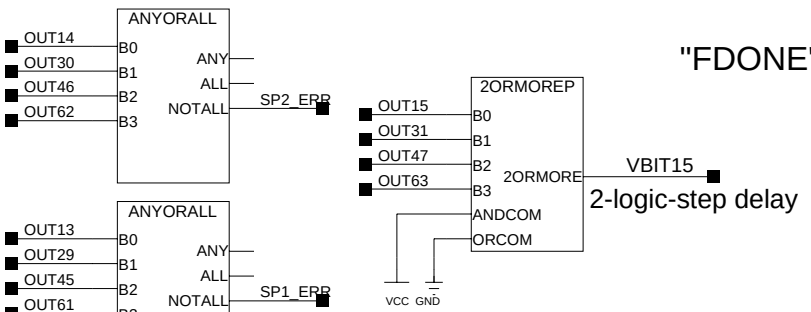


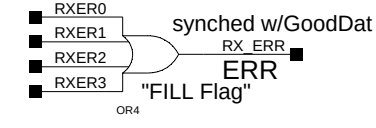
A FIFO ends at 1st false "LFIFO_EMPTY" after "LGoodLW"

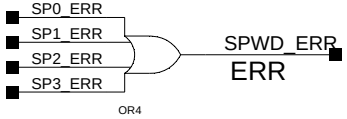
"FDONE" indicates "LGoodLW" was received: waiting for the final NotEmpty word from FIFO

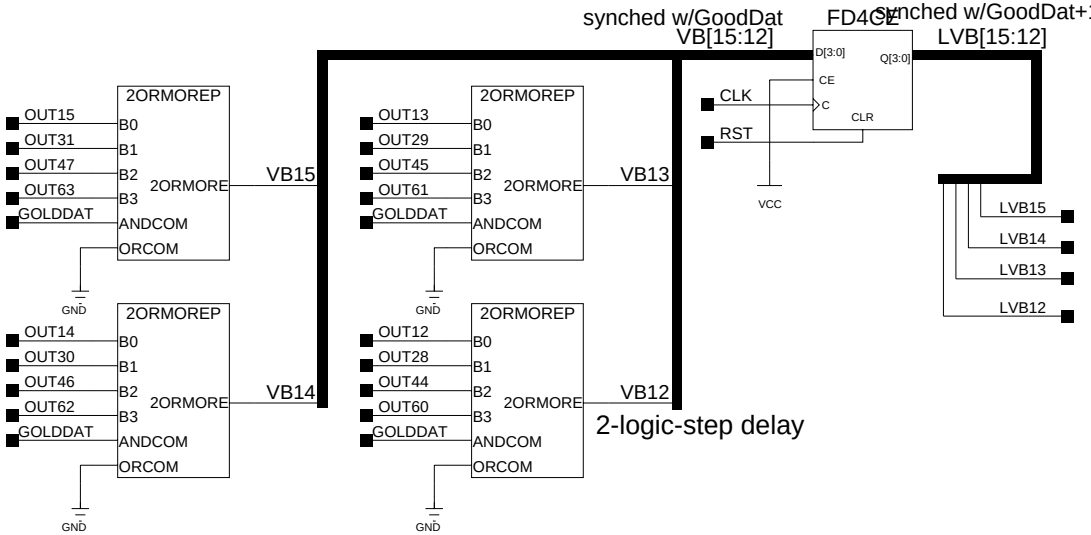
------> Switch FIFOs after next good word!

------> "RENOE-0" holds REN enabled until "FDONE" goes false









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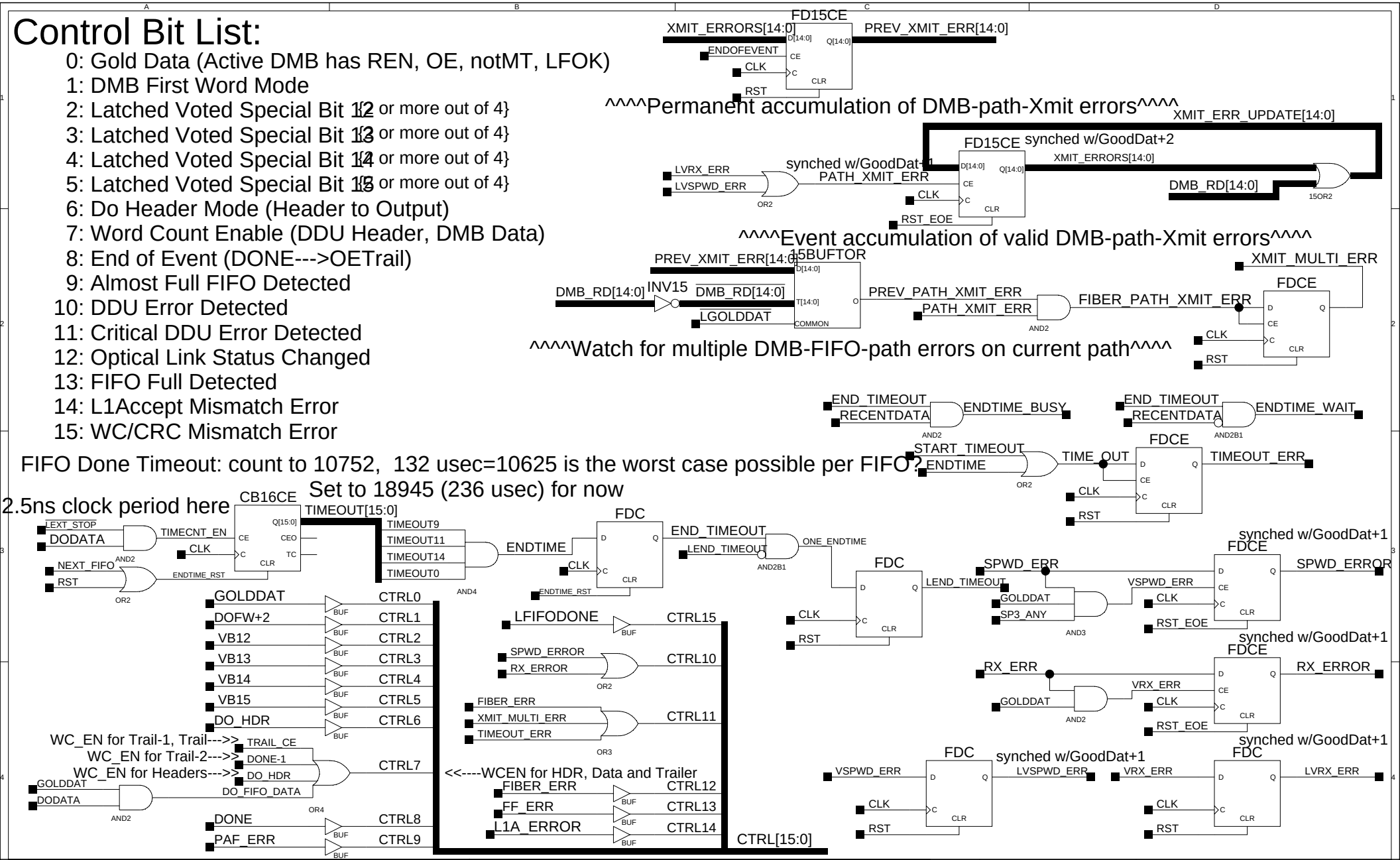
TITLE: Read Control
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
1-27-2005_10:59	FIFOCTRL . 3	3B

Control Bit List:

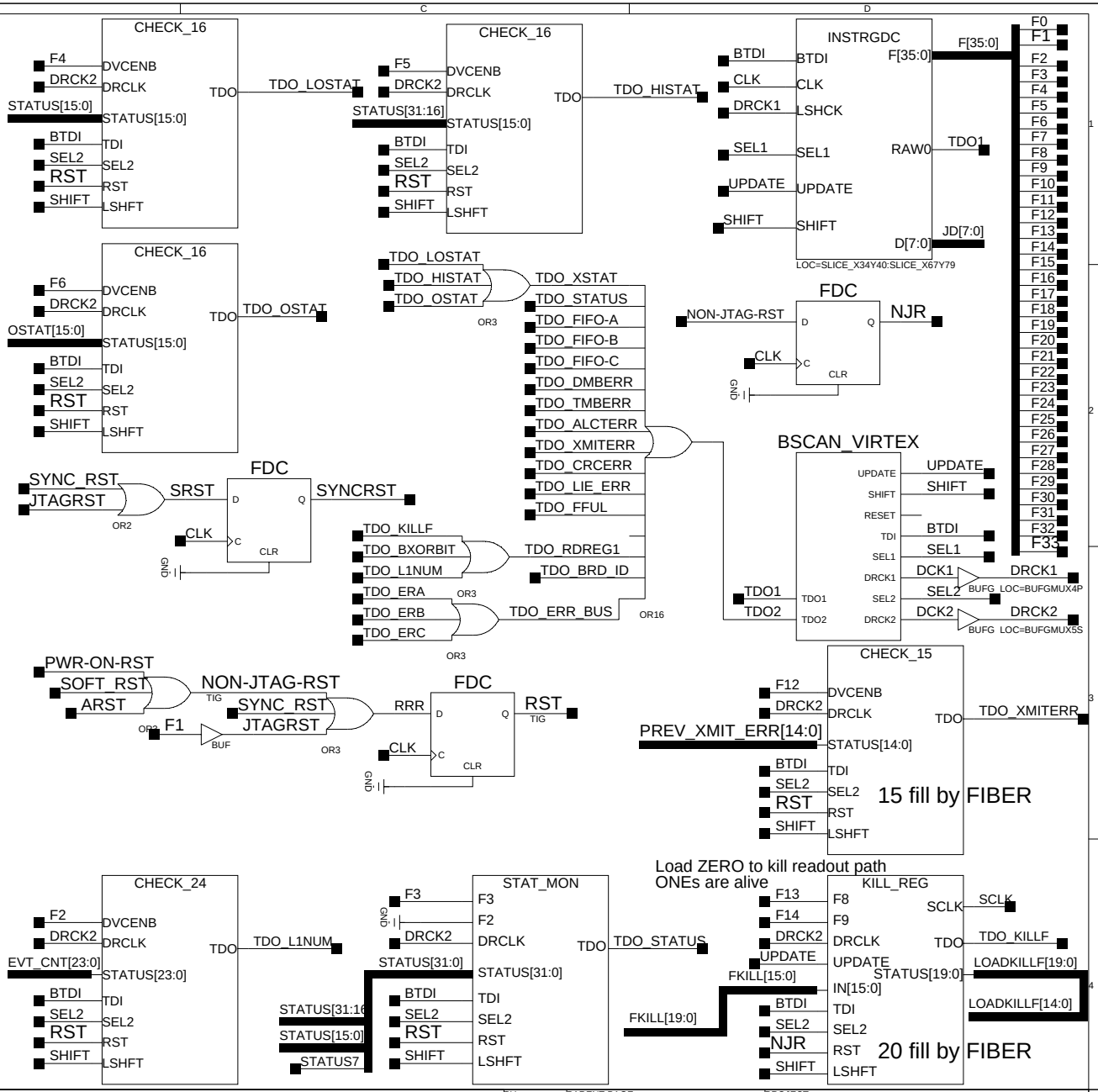
0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE--->OETrail)
9: Almost Full FIFO Detected
10: DDU Error Detected
11: Critical DDU Error Detected
12: Optical Link Status Changed
13: FIFO Full Detected
14: L1Accept Mismatch Error
15: WC/CRC Mismatch Error



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 1-26-2005_11:15	FILE: FIFOCTRL . 4	PAGE: 3C

JTAG Instruction Decode

OpCode		Function [OpName]
	0	No Operation [NOOP]
old code	1	FPGA Reset [toggle]
	2	Read Current DDU L1A Number (24-bit scaler)
	3	Check status (capture and shift) [32 bits]
	4	Check status, low-word [16 bits]
	5	Check status, high-word [16 bits]
27	6	Output Path Status [16-bits]
7	7a	Check FOK (active input FIFOs) [lowest4 bits]
11	7b	L1A Mismatch (FIFO headers) [4-bits] check FIFO-A
6	7c	Check FIFO Err (active FIFO change) [4 bits]
26	7d	Stuck Data Errors (input FIFOs) [highest4-bits]
20	8a	Almost Full FIFOs [lowest 10-bits] check FIFO-B
25	8b	FIFO Empty Status [highest 6-bits]
21	9	Full FIFOs [10-bits]
	10	CRC Errors [15-bits]
19	11a	Lost In Data [lowest 4-bits] check FIFO-C
8	11b	Timeout: start [4-bits]
9	11c	Timeout: end-wait [4-bits]
15	11d	Timeout: end-active [highest 4-bits]
	12	Data Xmit Errors [15-bits]
13	13	Check KILL_Register [20 bits]
14	14	Load KILL_Register [20 bits]
16	15	DMB Errors [15-bits]
17	16	TMB Errors [15-bits]
28	17	ALCT Errors [15-bits]
	18	Lost In Event [15-bits]
		free: 19-21, 25-28
	22	Error Register A [16-bits]
	23	Error Register B [16-bits]
	24	Error Register C [16-bits]
	29	Set BX per Orbit [12-bits]
	30	Read BX per Orbit [12-bits]
	31	Toggle CFEB_Cal Auto_L1 [default enable]
	32	Read DDU Board ID [16-bits]
	33	DDU-only VME_L1A



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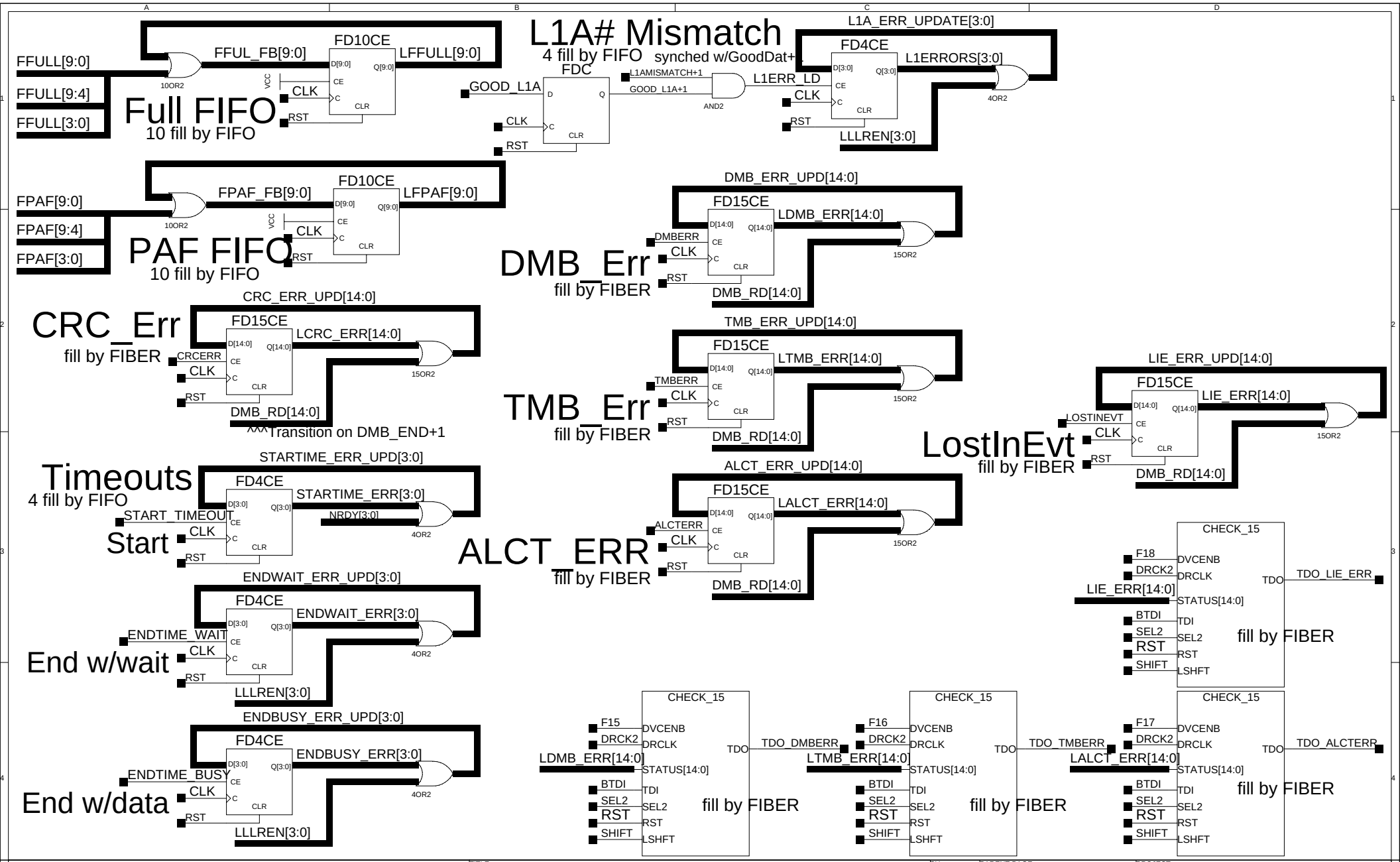
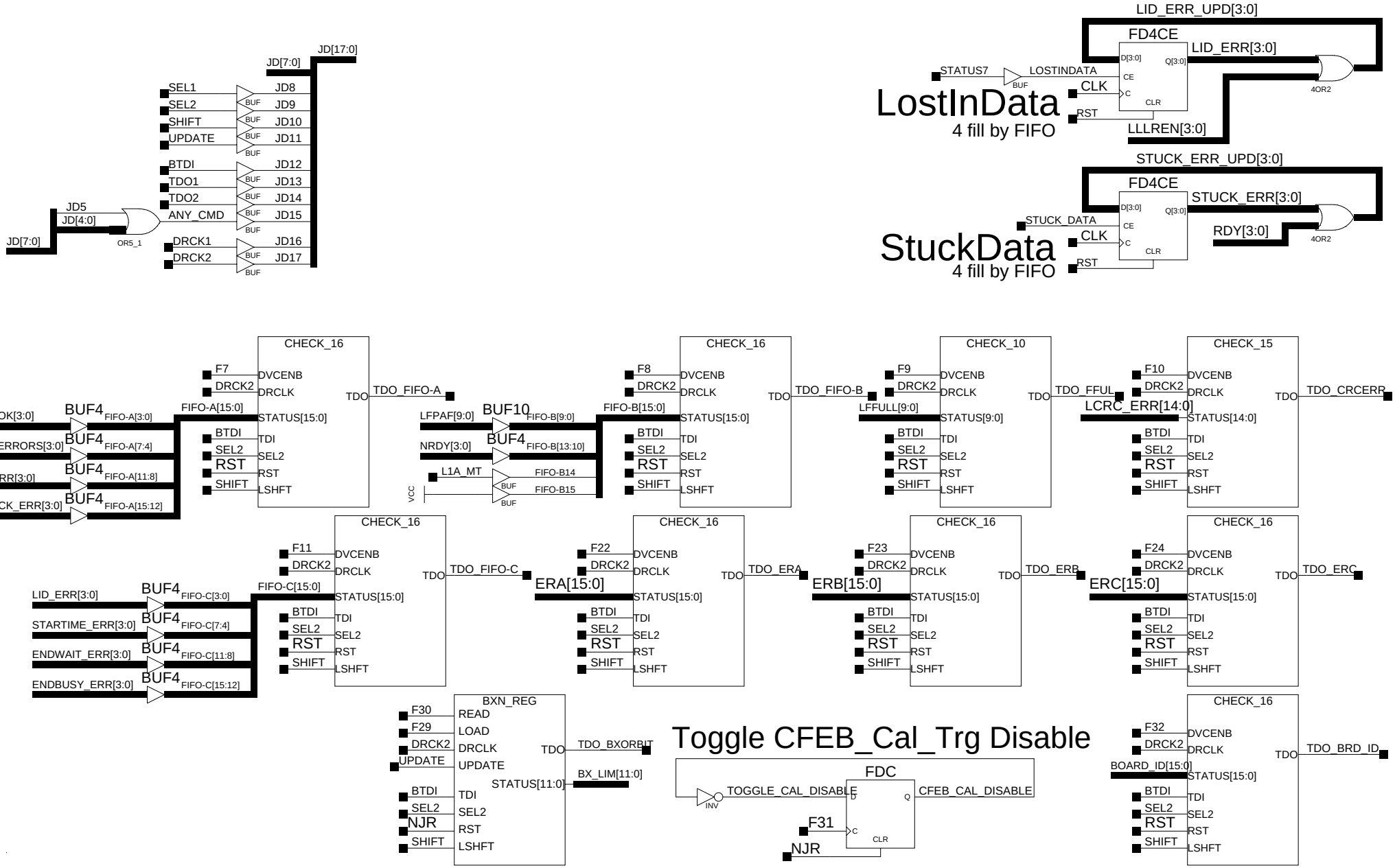
TITLE: JTAG Signals
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 1-26-2005_11:16 | FILE: FIFOCTRL . 5 | PAGE: 3D

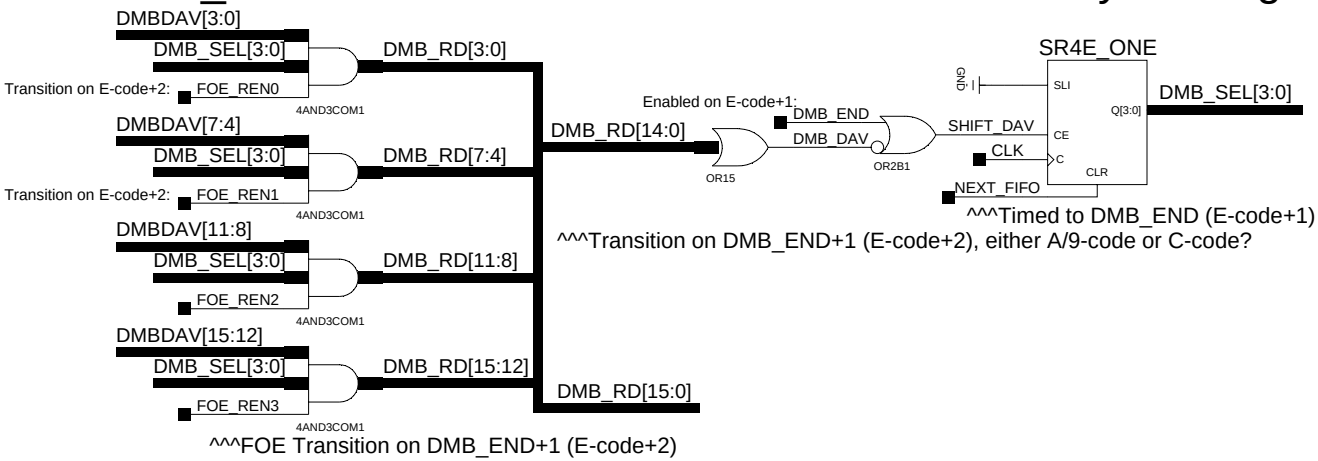


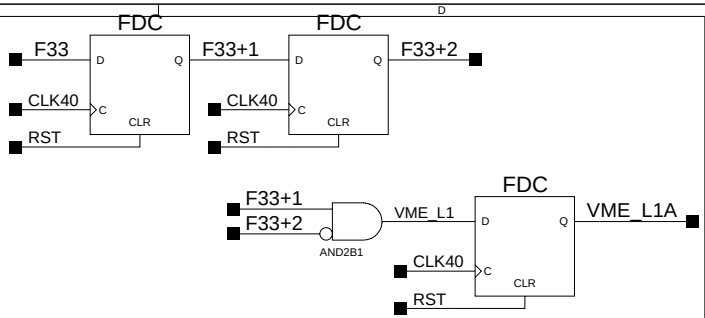
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG · PARENT PAGE: 2 DATE: 1-26-2005_11:16	PROJECT: D785C FILE: FIFOCTRL . 6 · PAGE: 3E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG PARENT PAGE 2 DATE 1-26-2005_11:16	PROJECT D785C FILE FIFOCTRL . 7 PAGE 3F

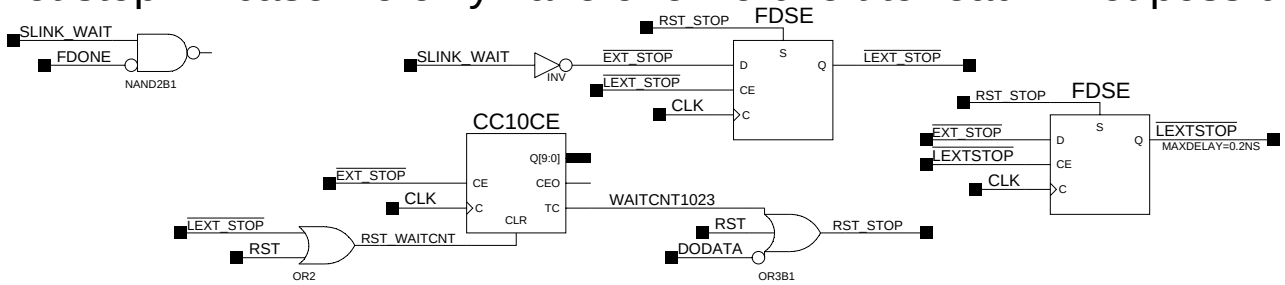
Use DMB_RD to determine which FIBER we're currently reading

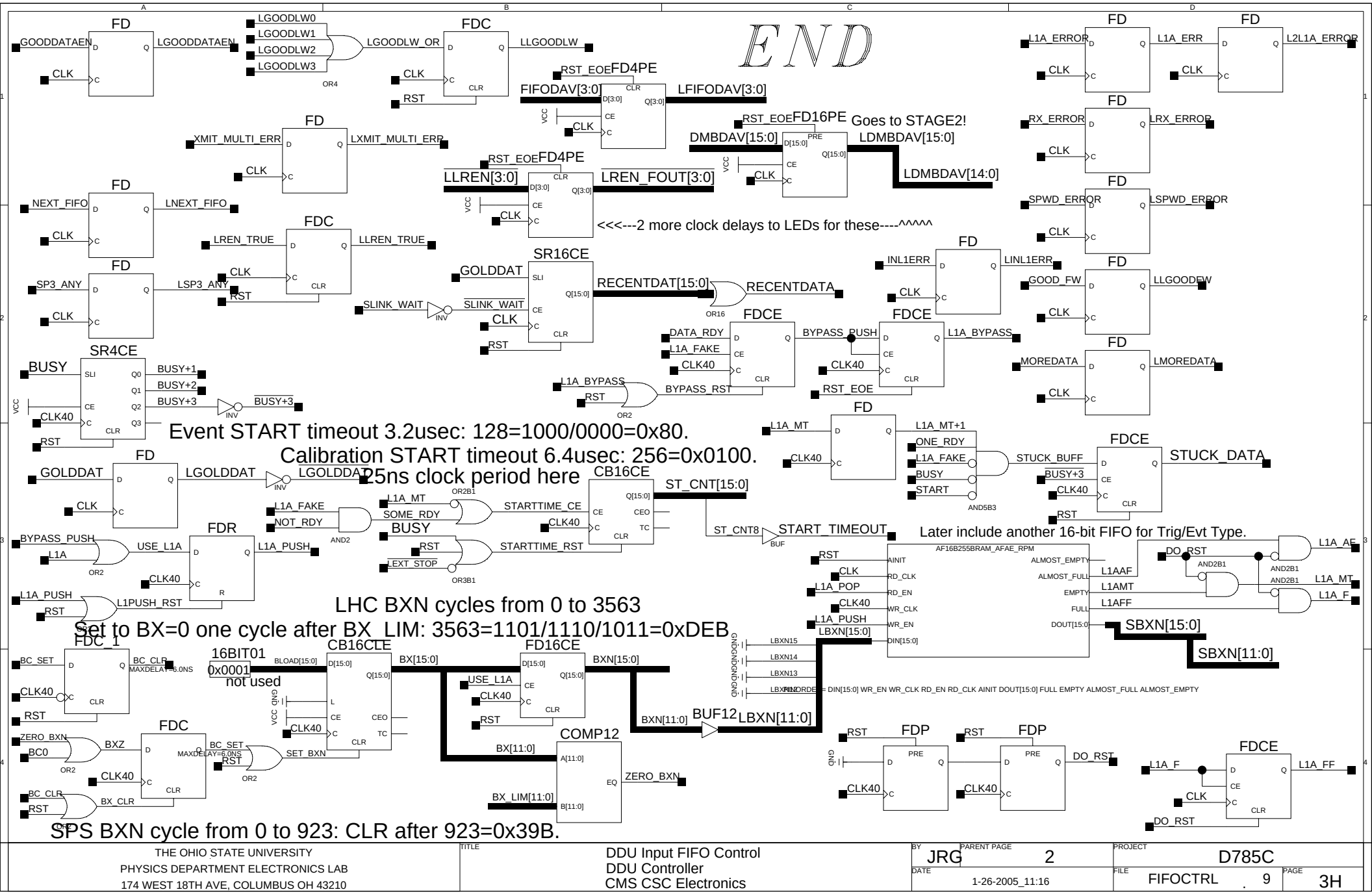




Stop READ cycle on DCC Near Full

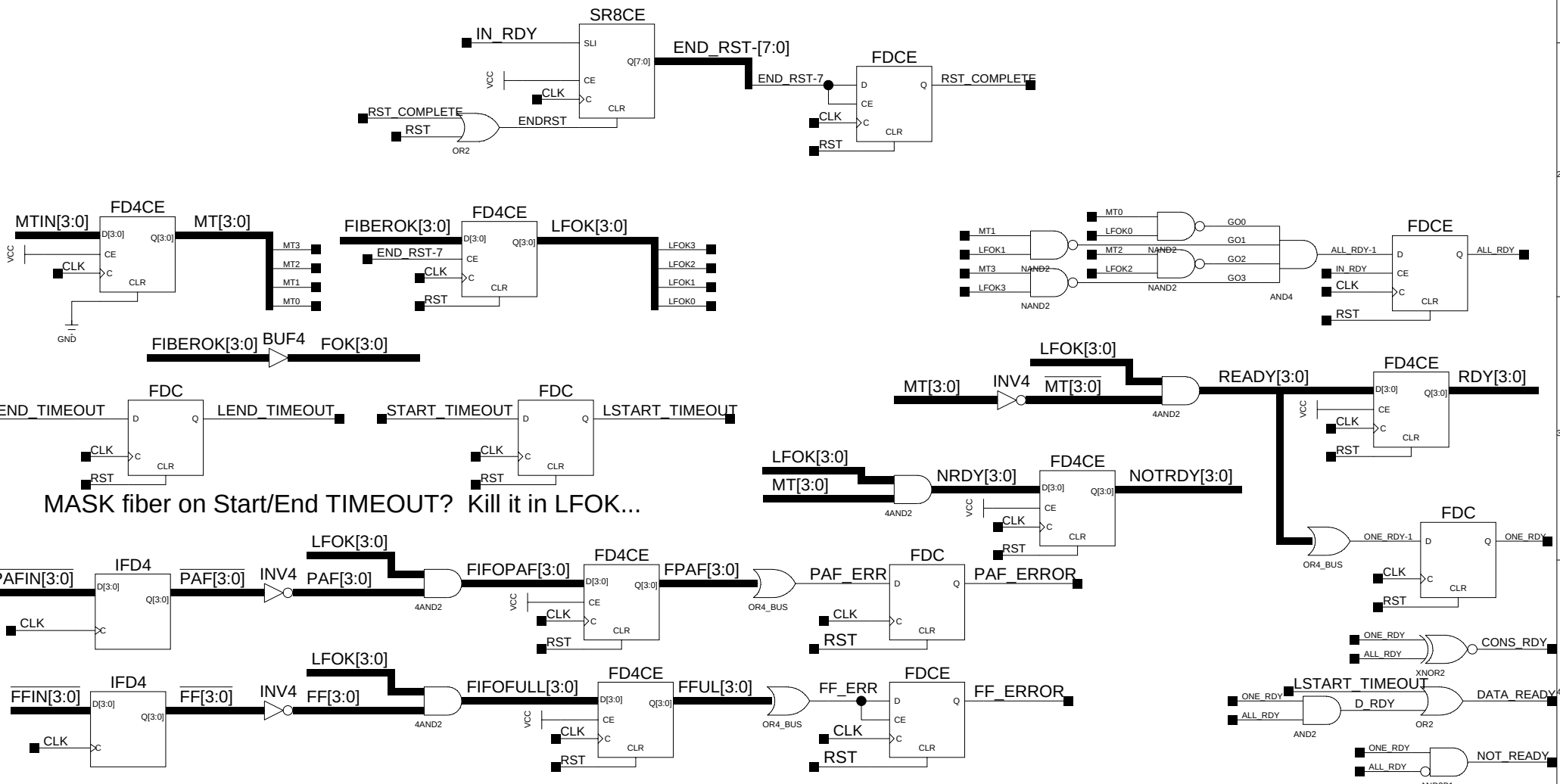
How to "not stop" in case we only have one word left to read? Not possible to do well...



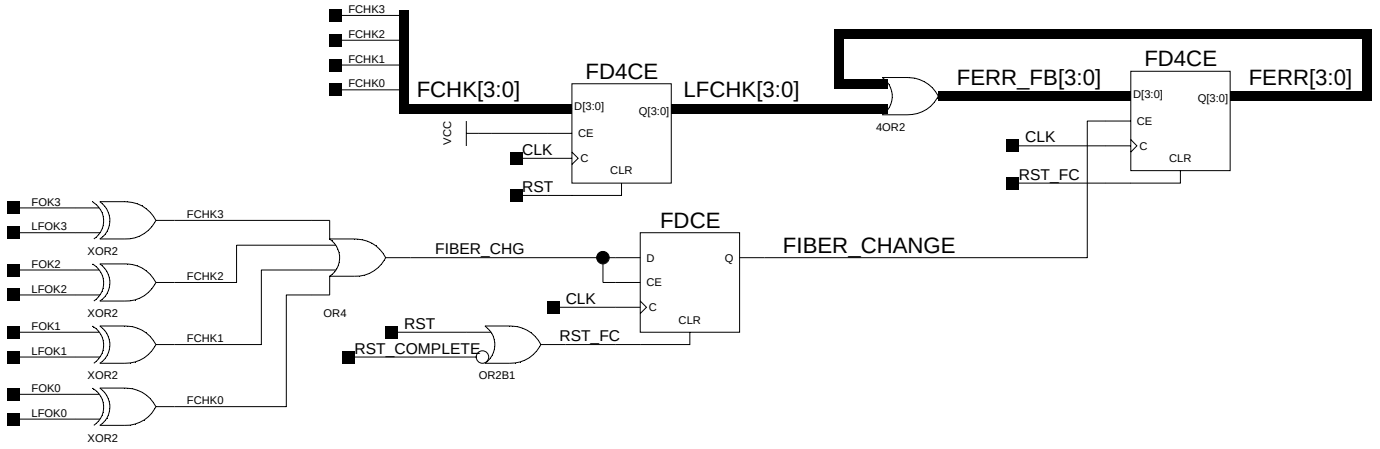


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:16	PARENT PAGE: 2 PROJECT: D785C FILE: FIFOCTRL . 9 PAGE: 3H

Access FIBEROK from JTAG as a fiber check.
---> RESET required after fiber status change for now...
Change in FIBEROK is BAD! Set error code.
...notify FMM and maybe set STATUS bit, but
...data is OK until FIFO read time-out occurs.
...but how to know WHEN the bad-data comes ou
---> timeout will probably occur for that event

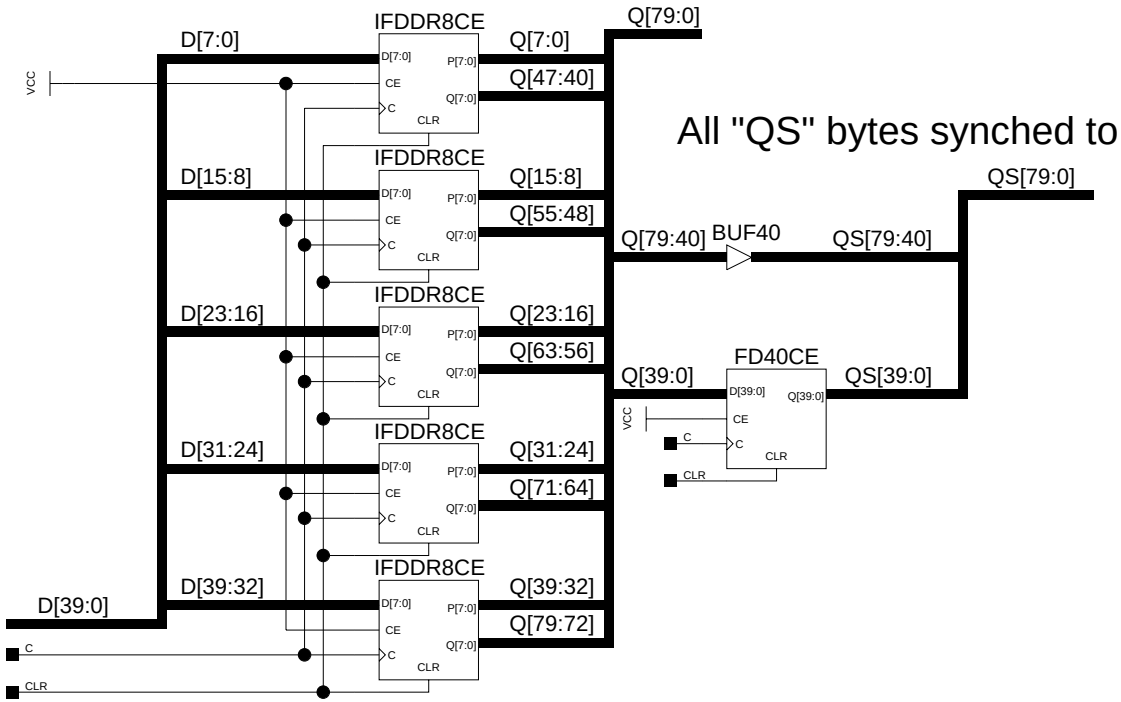


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input FPGAs Available for DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 1-26-2005_11:19	FILE: FIFO_RDY . 1	PAGE: 4



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 1-26-2005_11:19	FILE: FIFO_RDY . 2	PAGE: 4A

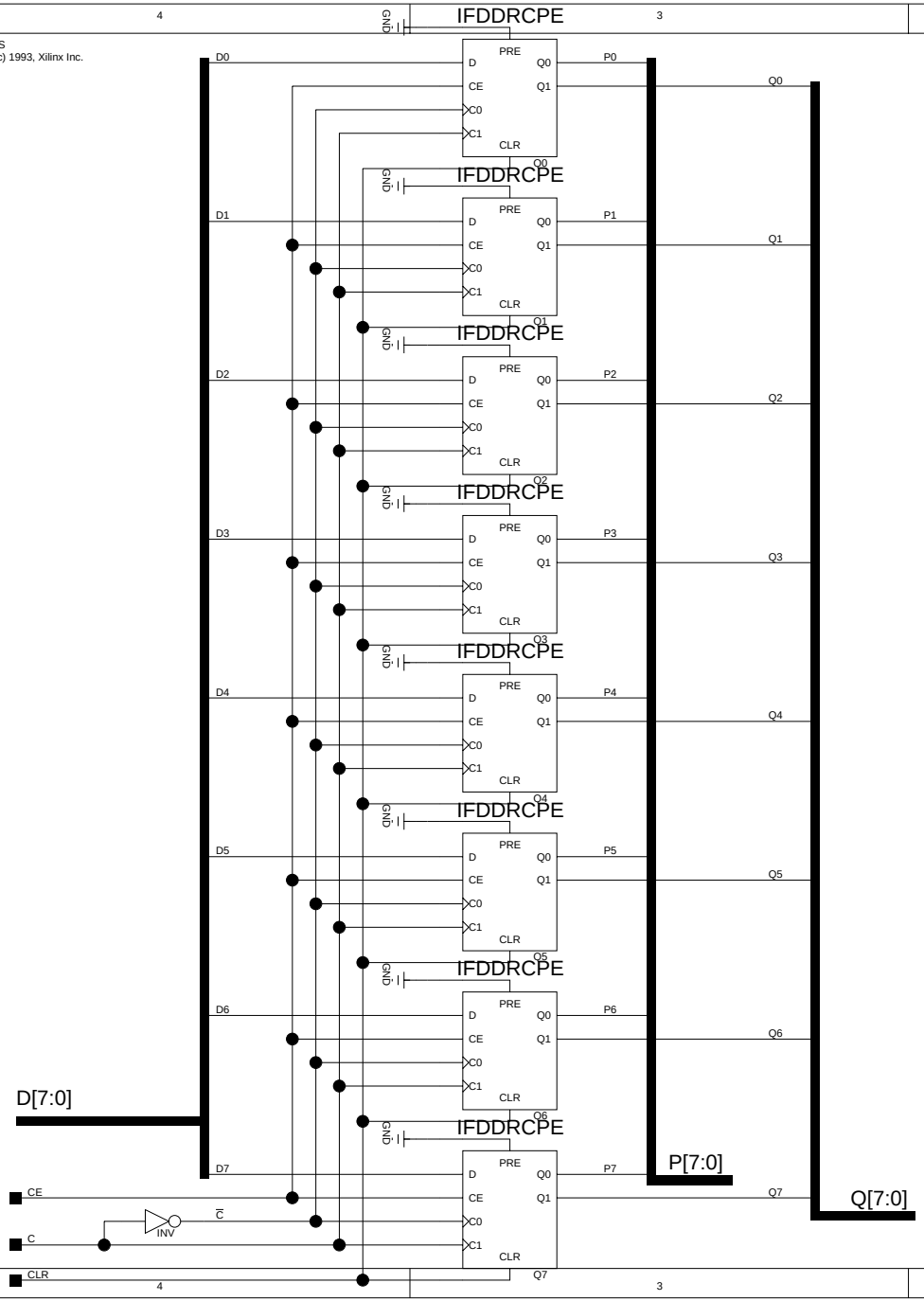
Lowest 5 "Q" bytes synched to falling edge of CLK



All "QS" bytes synched to rising edge of CLK

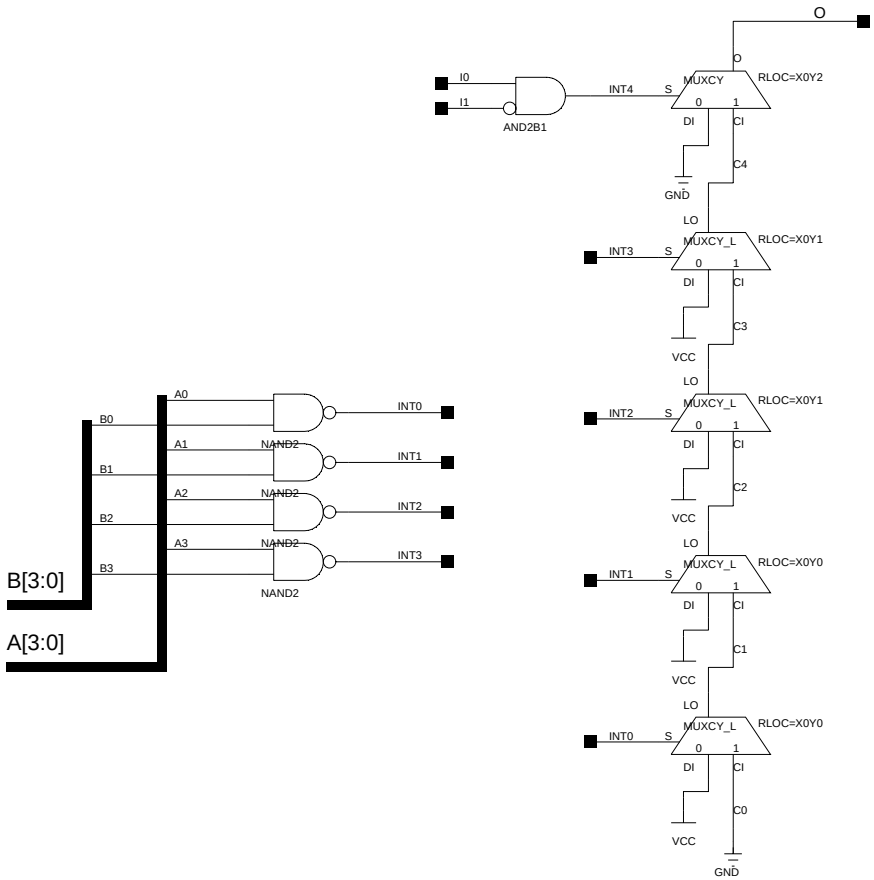
CLK/\ -- DIN[39:0] -- CLK\/ -- Q[39:0] DIN[79:40] -- CLK/\ -- Q[79:40] QS[39:0]

Title:	VIRTEX Family IFDDR40C Macro		
Comments:	40-Bit DDR Input Flip-Flop with asynchronus clear	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A

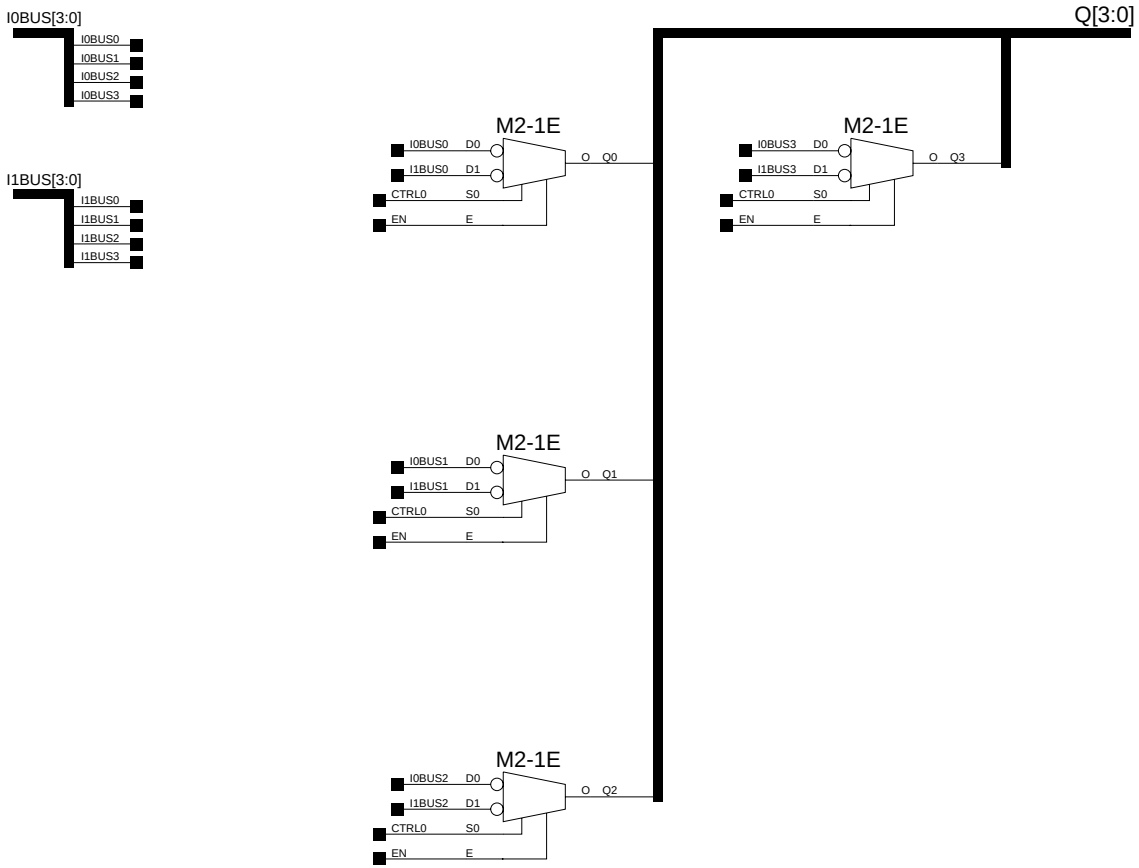


XILINX

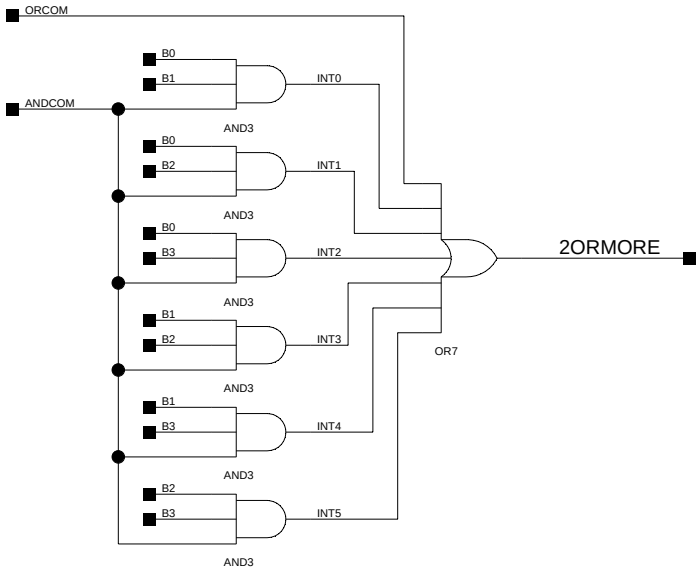
Title:	VIRTEX Family IFDDR8CE Macro		JRG
Comments:	8-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



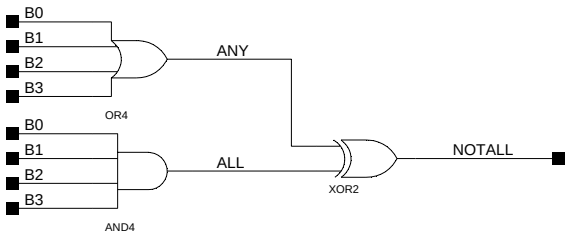
XILINX			JRG
Title:	FAST10B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 .AND. AND2B1		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A



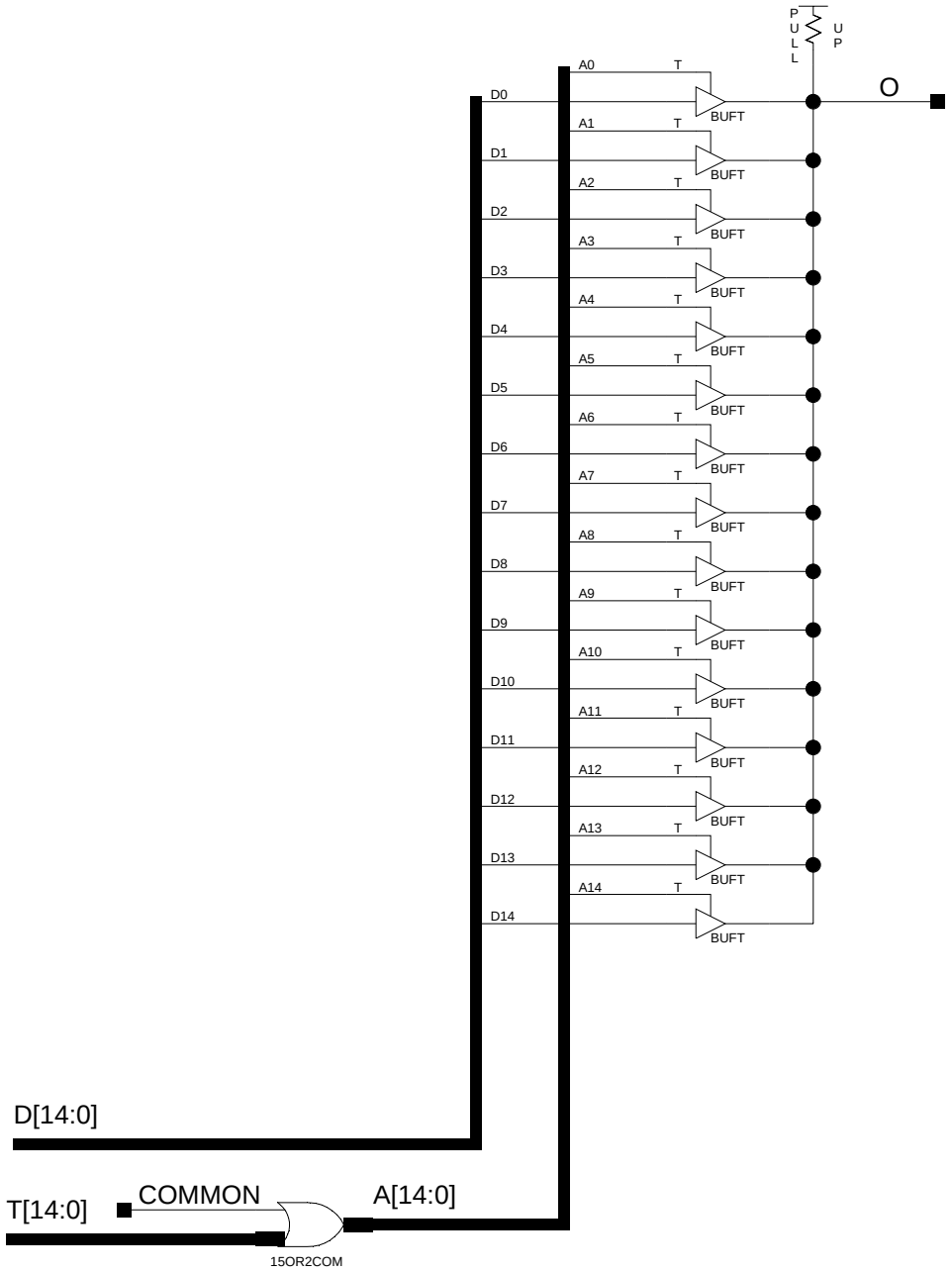
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 4-bit MUX for 2 4-bit Inputs, w/Enable, invert selected DIN DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:23	PARENT PAGE: 3 PROJECT: D785C FILE: MUX2_4B_INV . 1 PAGE: 8



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 1-26-2005_11:26	FILE: 2ORMOREP . 1	PAGE: 9



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Check for ALL bits set, ANY bits set and NOTALL bits set DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3	PROJECT D785C
		DATE 1-26-2005_11:27	FILE ANYORALL . 1	PAGE 10



XILINX

Title: VIRTEX Family 15-BufTOR Macro

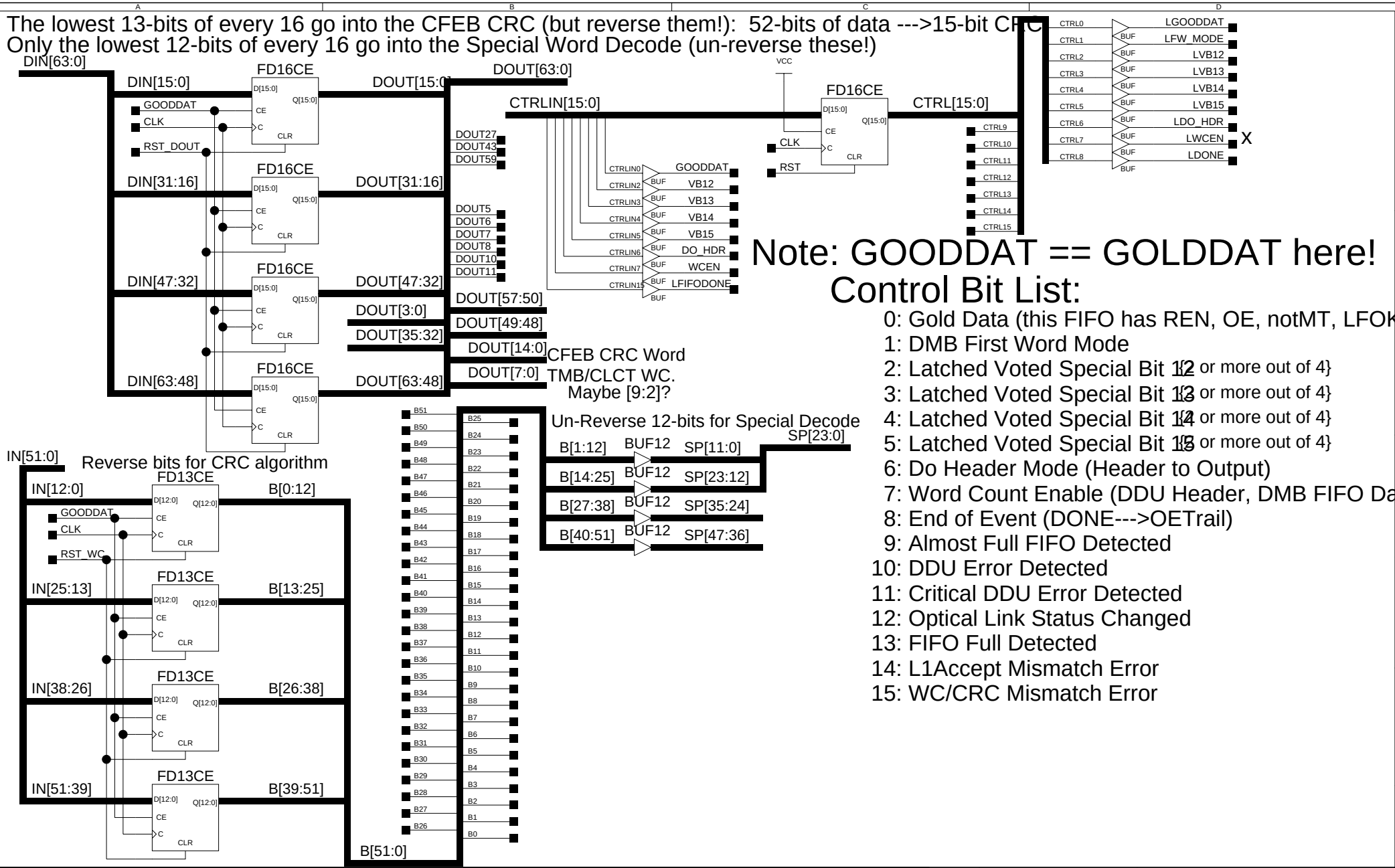
Comments:15-BufT Bus Gate with Bus-OR-Common control

JRG

Date: 27th December 2001 Ver: 1

Sheet Size: A Rev: A

drawn by KS



THE OHIO STATE UNIVERSITY
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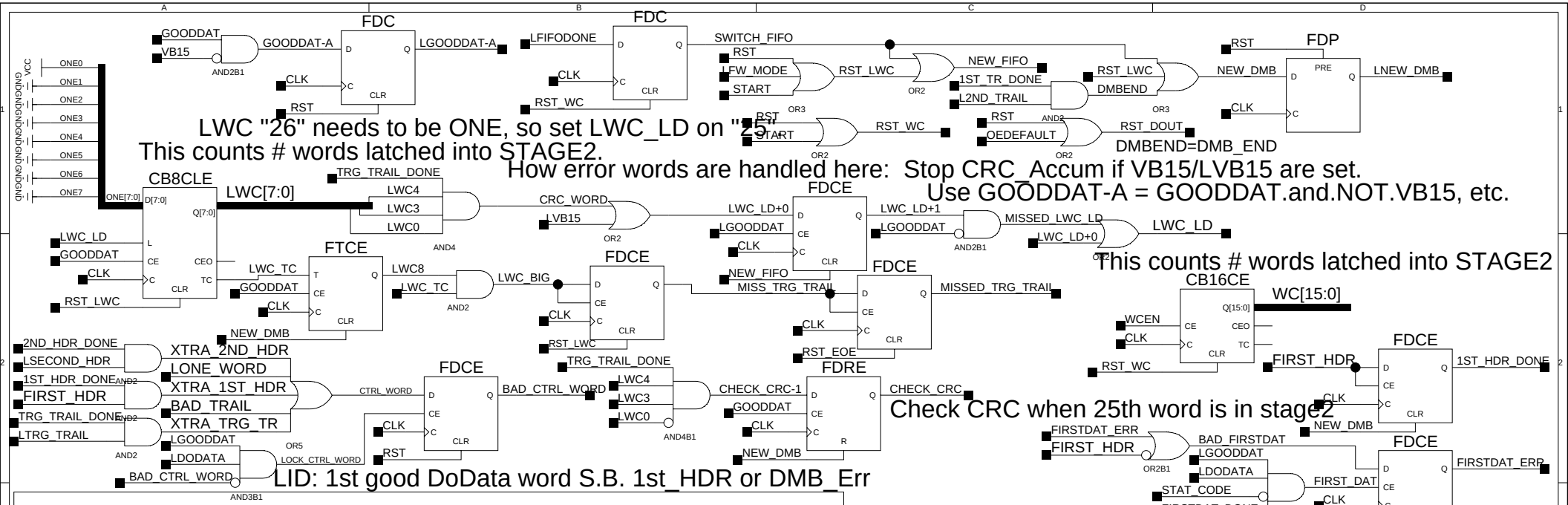
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Stage 2 Logic: WC/CRC Accumulators
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
1-26-2005_11:30	STAGE2 . 1	12



Critical DMB Monitoring Information (DMB rev. 5, Jan. 2003)

*** MOSTLY IMPLEMENTED IN DDU DESIGN! ***

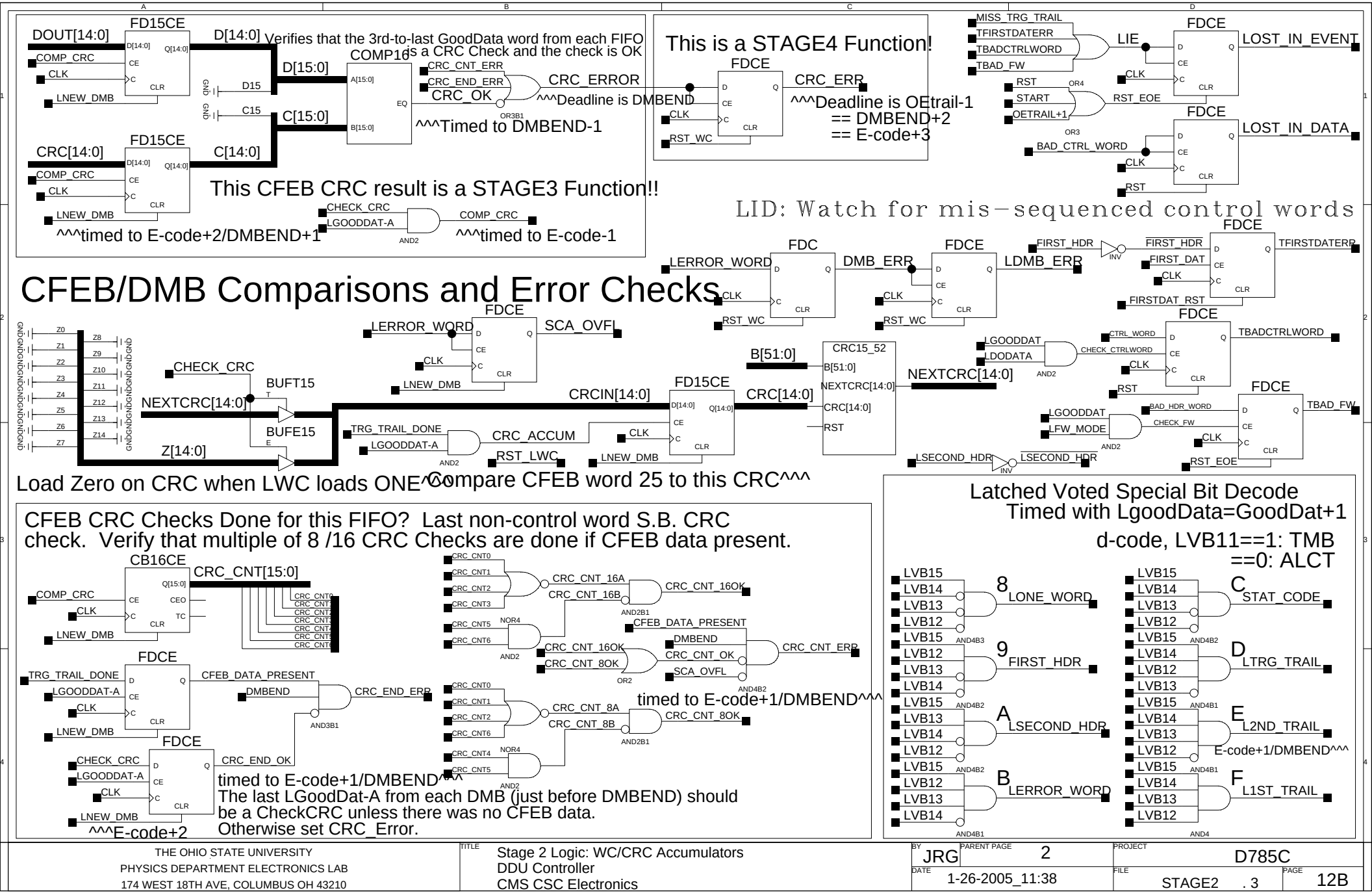
See http://www.physics.ohio-state.edu/~cms/dmb/datafmt_ddu.html

Within each time sample: word100[15:0] = dummy = 0x7FFF <----What about SCA Over-Written Event error?

word97[14:0] = CRC15 result	----->> *DDU Compare*
word98[7:4] = CFEB LCT FIFO # used out of 16	----->> ***DDU Warning***
word98[8] = CFEB LCT_FIFO_Full error	----->> *****DDU Error*****
word99[7:0] = CFEB L1A FIFO # used out of 256	----->> ***DDU Warning***
word98[9] = CFEB L1A_FIFO_Full error	----->> *****DDU Error*****
Trailer3[11:4] = DMB L1A FIFO # used out of 256	----->> ***DDU Warning***
Trailer5[11:6] = DMB External_FIFO_Full_error[TMB:CFEB1]	----->> *****DDU Error*****
TR2[6:0] = DMB Ext_FIFO_Half-Full_Warning[TMB,Overlap:CFEB1] (low-true)	
Header7[11:7] = CFEB_Multi-Overlap[5:1] = Garbage Event	----->> *****DDU Error*****
Trailer6,7,8[11:0] = DMB End/Start Timeout error, 3 repeats	----->> *****DDU Error*****
Header5[11,8,6] = TMB DAV bit, 3 repeats	----->> **DDU Control**
Header1,5[4:0] = CFEB_DAV[CFEB5:1], 2 repeats	=====>> *DDU Compare Together*
Header1[9:5] = CFEB_CLCT[CFEB5:1], 1 repeat /	
L1AN[23:0] = HDR3[11:0],HDR2[11:0]	----->> *DDU Compare*
BXN[11:0] = HDR4[11:0]	----->> *DDU Compare*

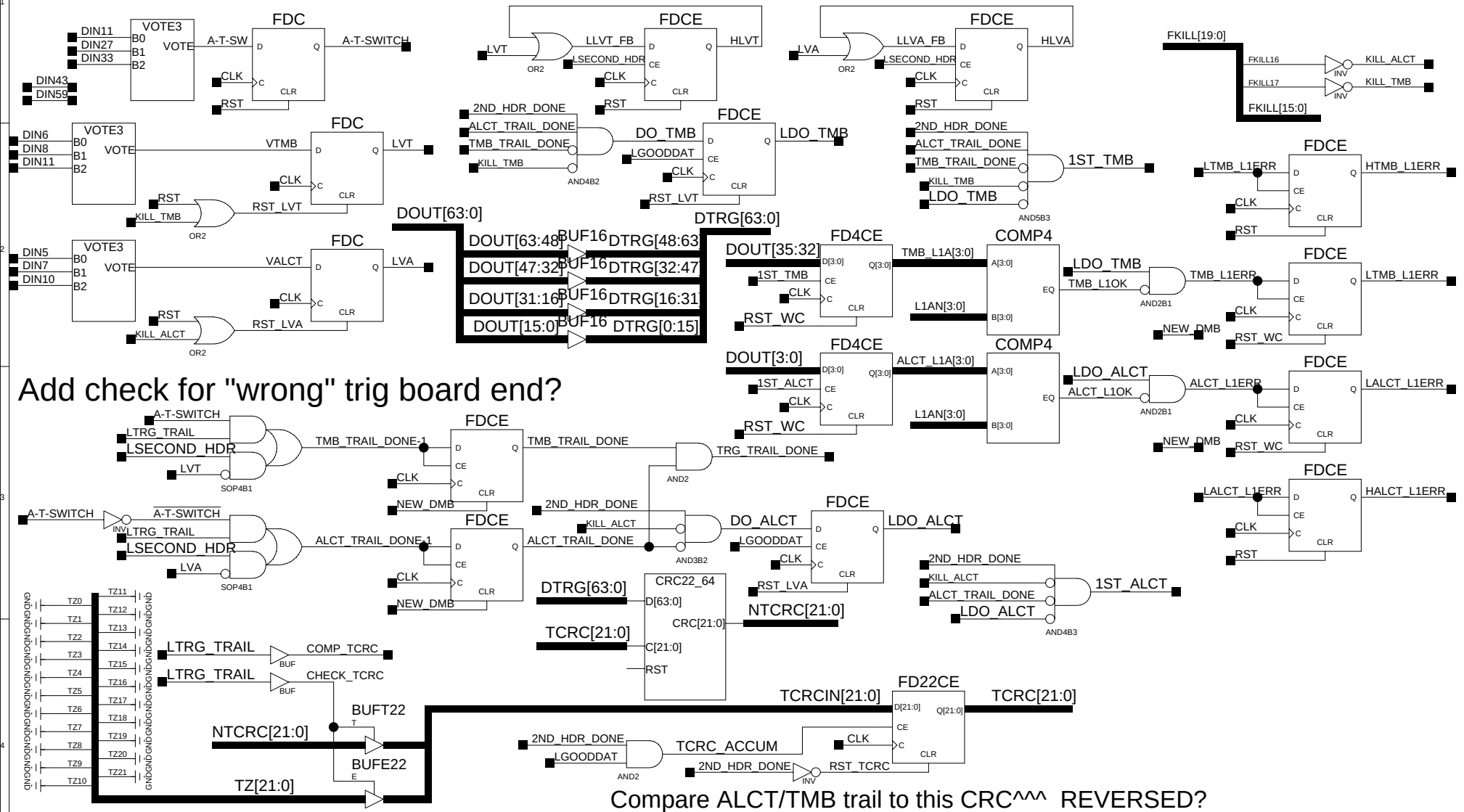
NotUsed?

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
			DATE 1-26-2005_11:30	FILE STAGE2 . 2	PAGE 12A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 1-26-2005_11:38	PROJECT: D785C FILE: STAGE2 . 3 PAGE: 12B

Trigger CRC Check Control: assume that TMB comes after ALCT!



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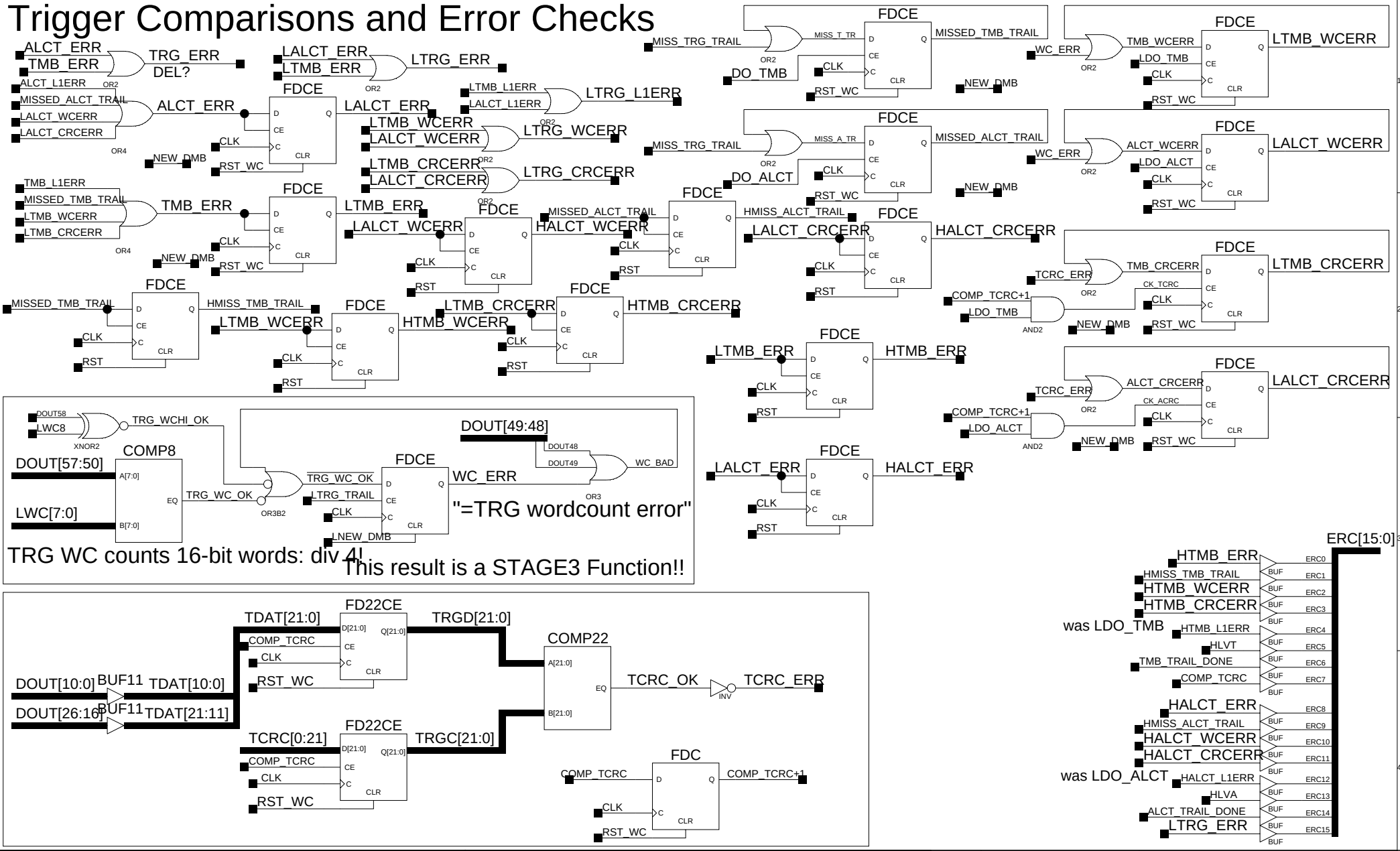
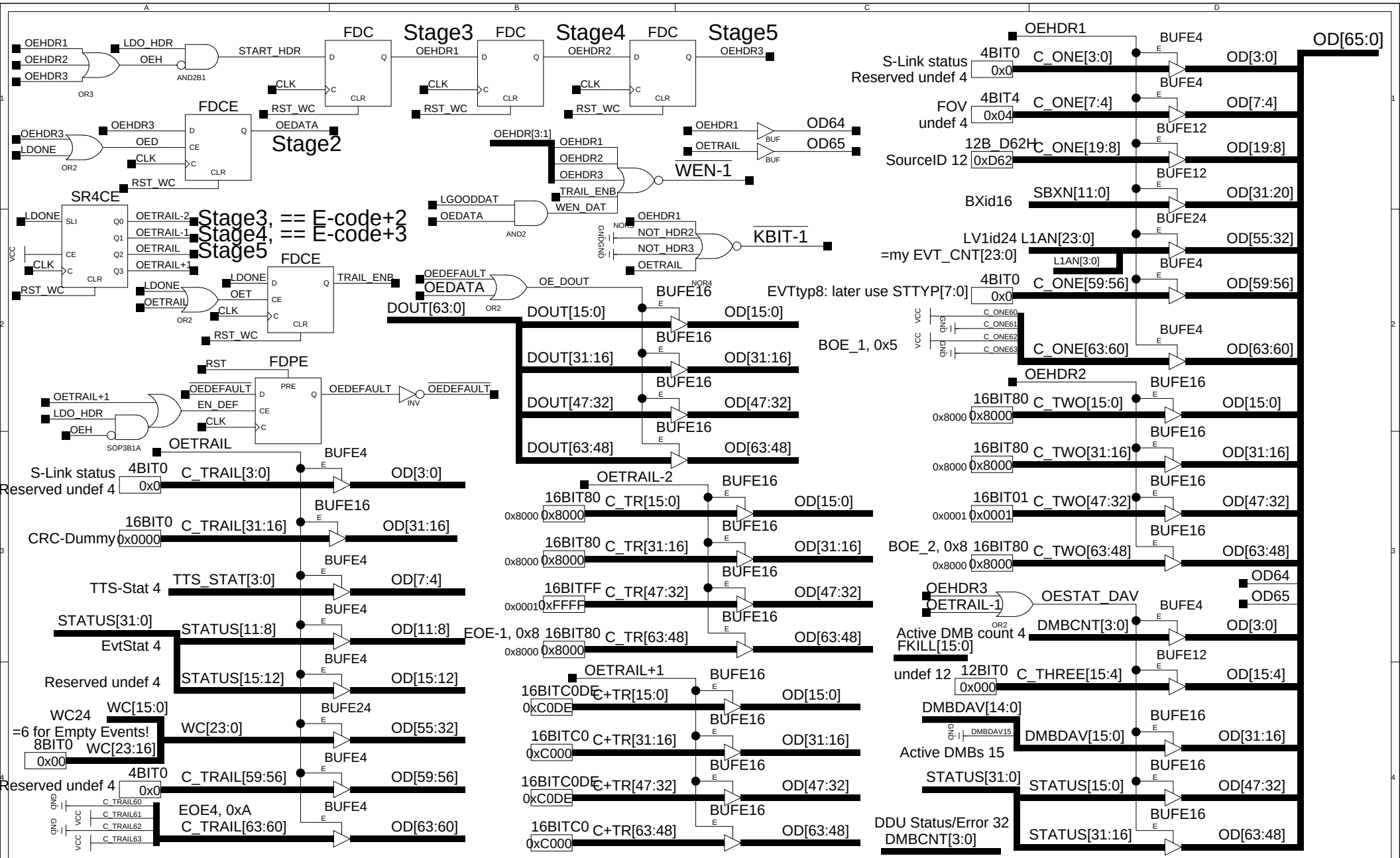
TITLE	Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2
		DATE 1-26-2005_12:28	PROJECT D785C
			FILE STAGE2 . 4
			PAGE 12C

Trigger Comparisons and Error Checks

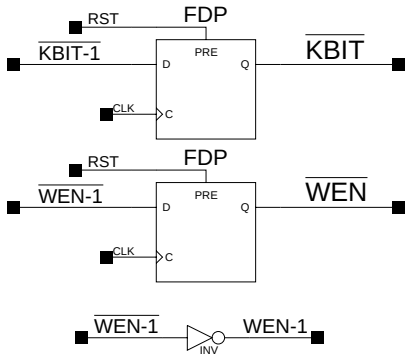


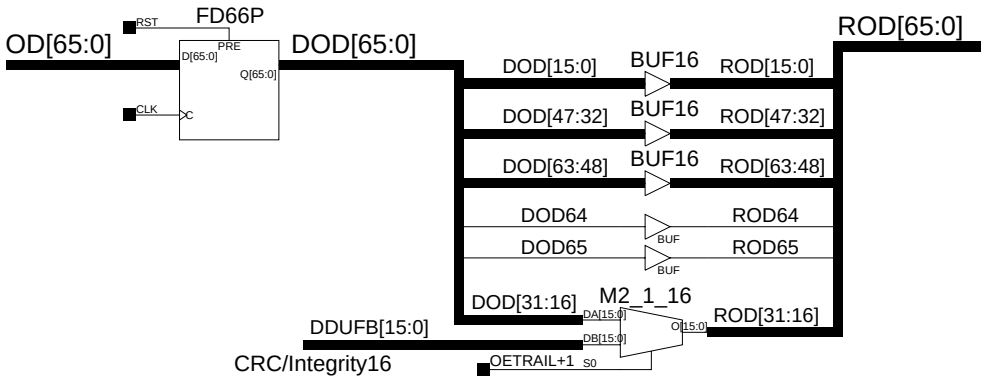
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C	
		DATE: 1-26-2005_11:30		FILE: STAGE2 . 5	PAGE: 12D

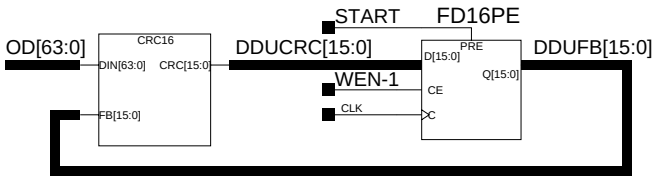


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 2-4-2005_13:38	FILE: STAGE2 . 6	PAGE: 12E

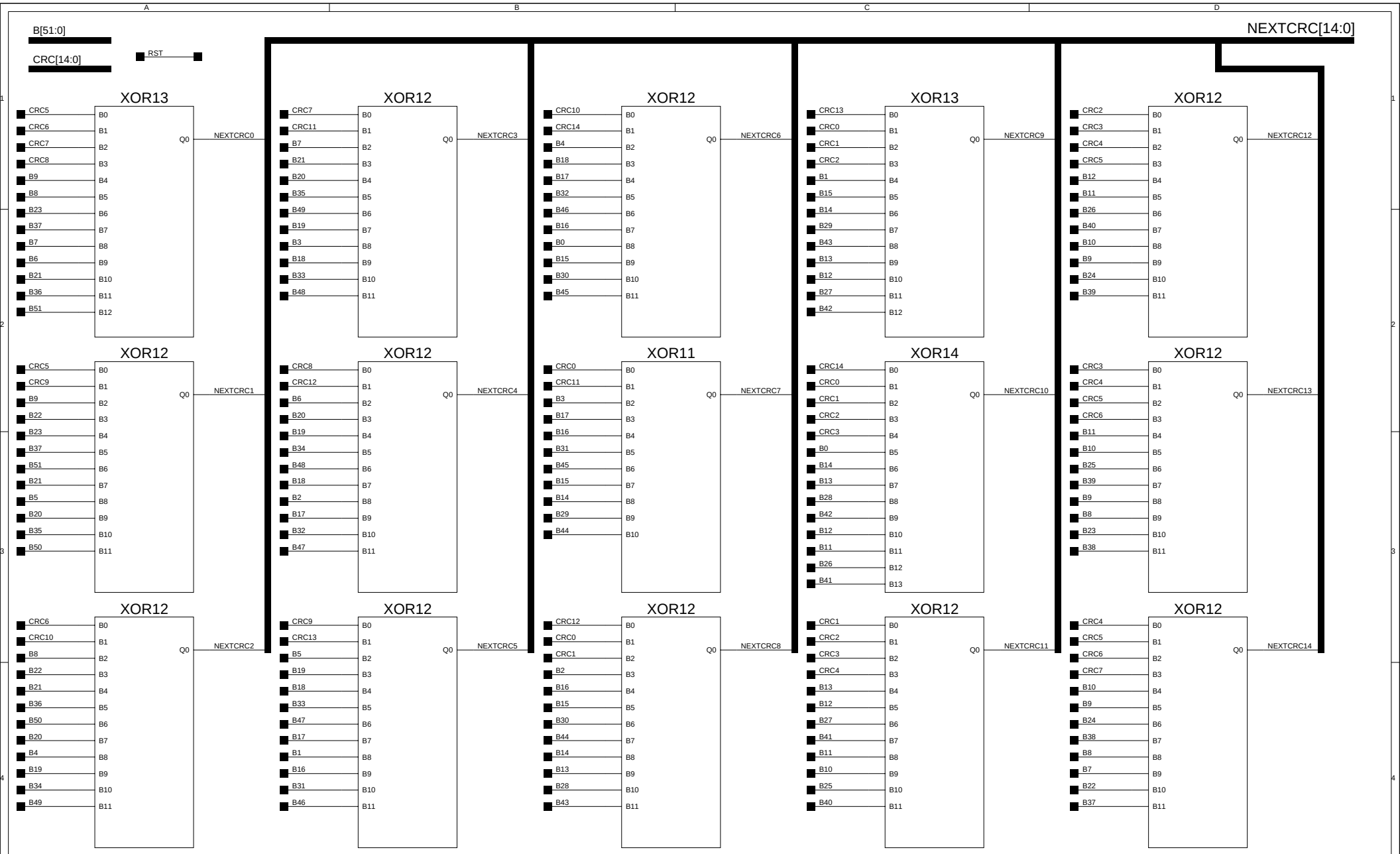
END







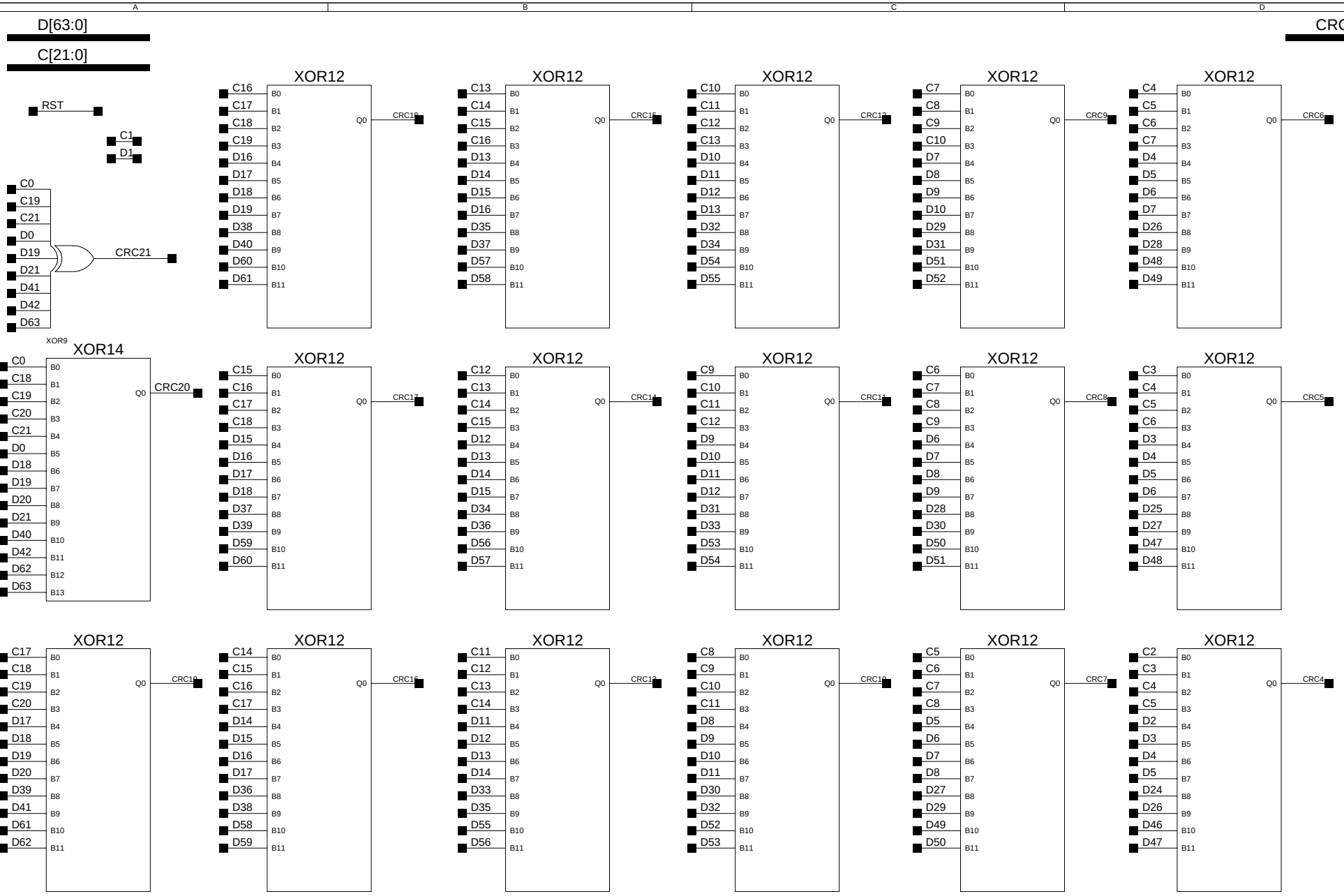
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU CRC Logic for SLINK/C.D.F. Compatibility DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 1-26-2005_11:38	FILE: STAGE2 . 7	PAGE: 12F



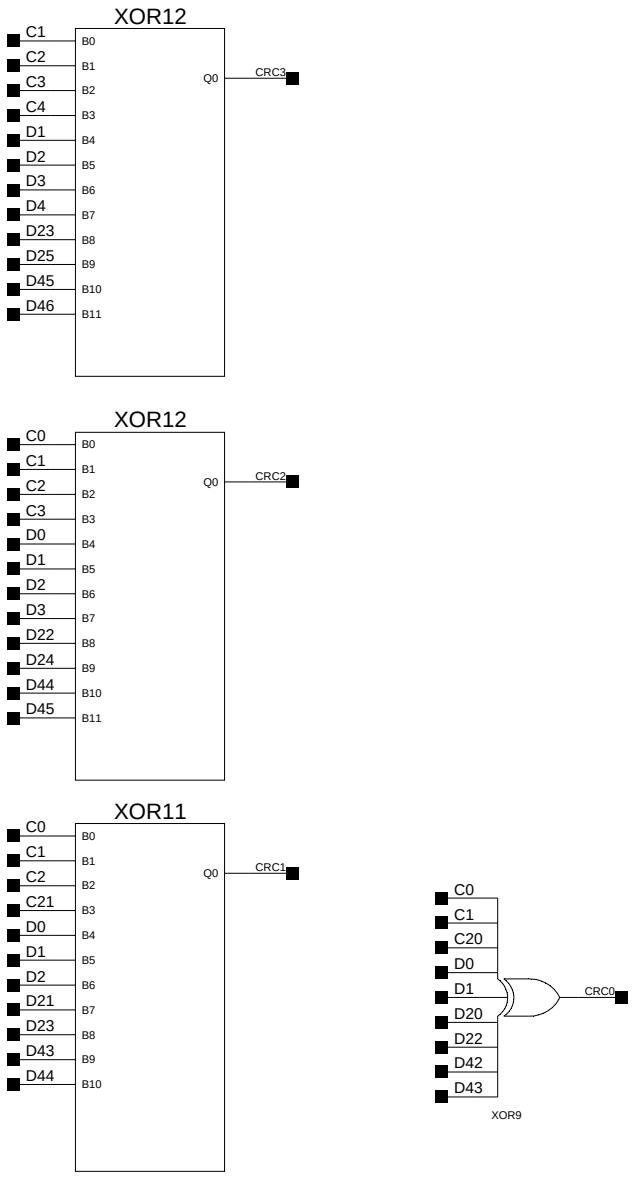
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: CRC15, 52-bit wide data equations
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	12B	D785C
DATE	FILE	PAGE
1-26-2005_11:33	CRC15_52 . 1	13

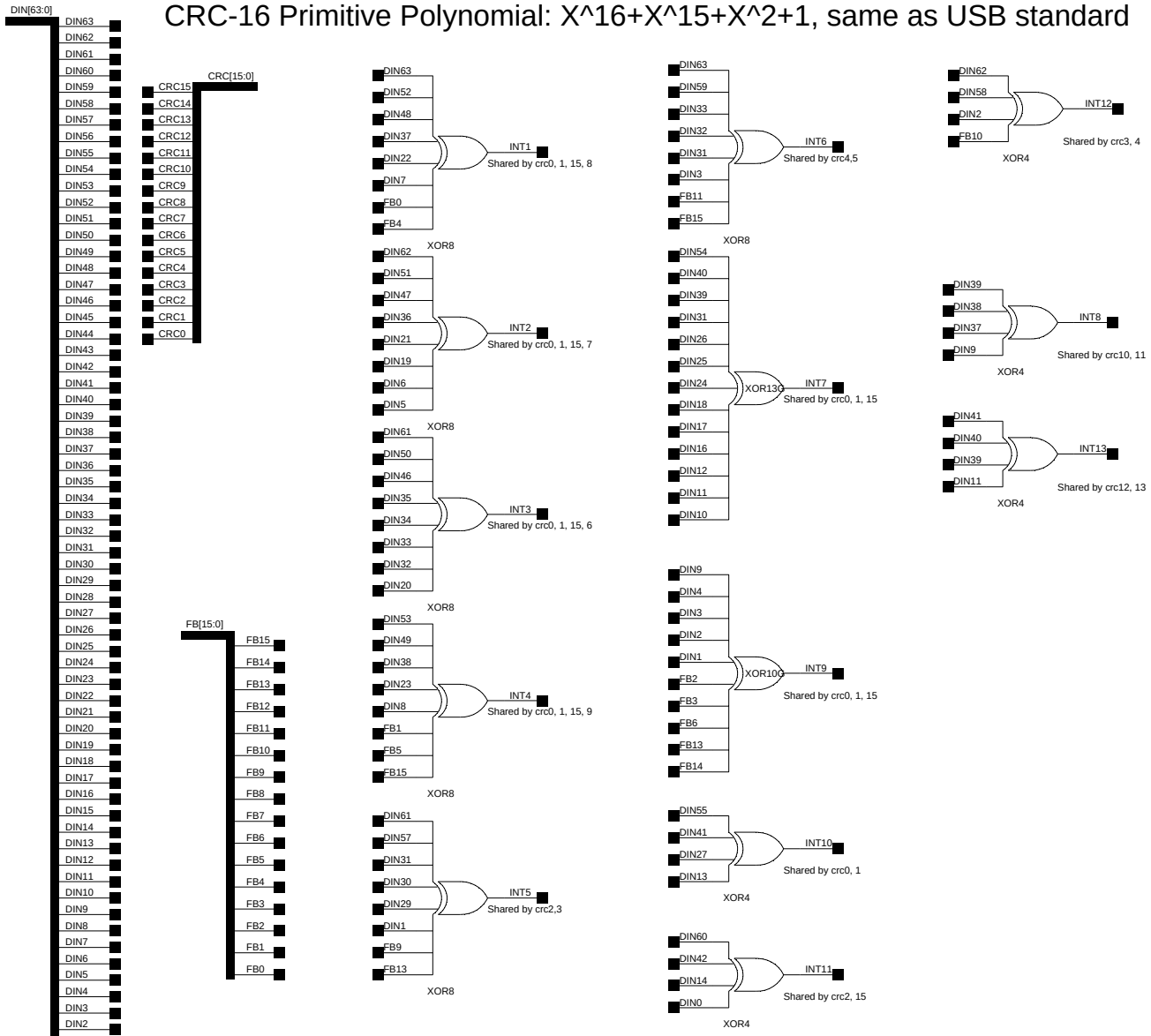


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:33	PARENT PAGE: 12C FILE: CRC22_64 . 1	PROJECT: D785C PAGE: 14

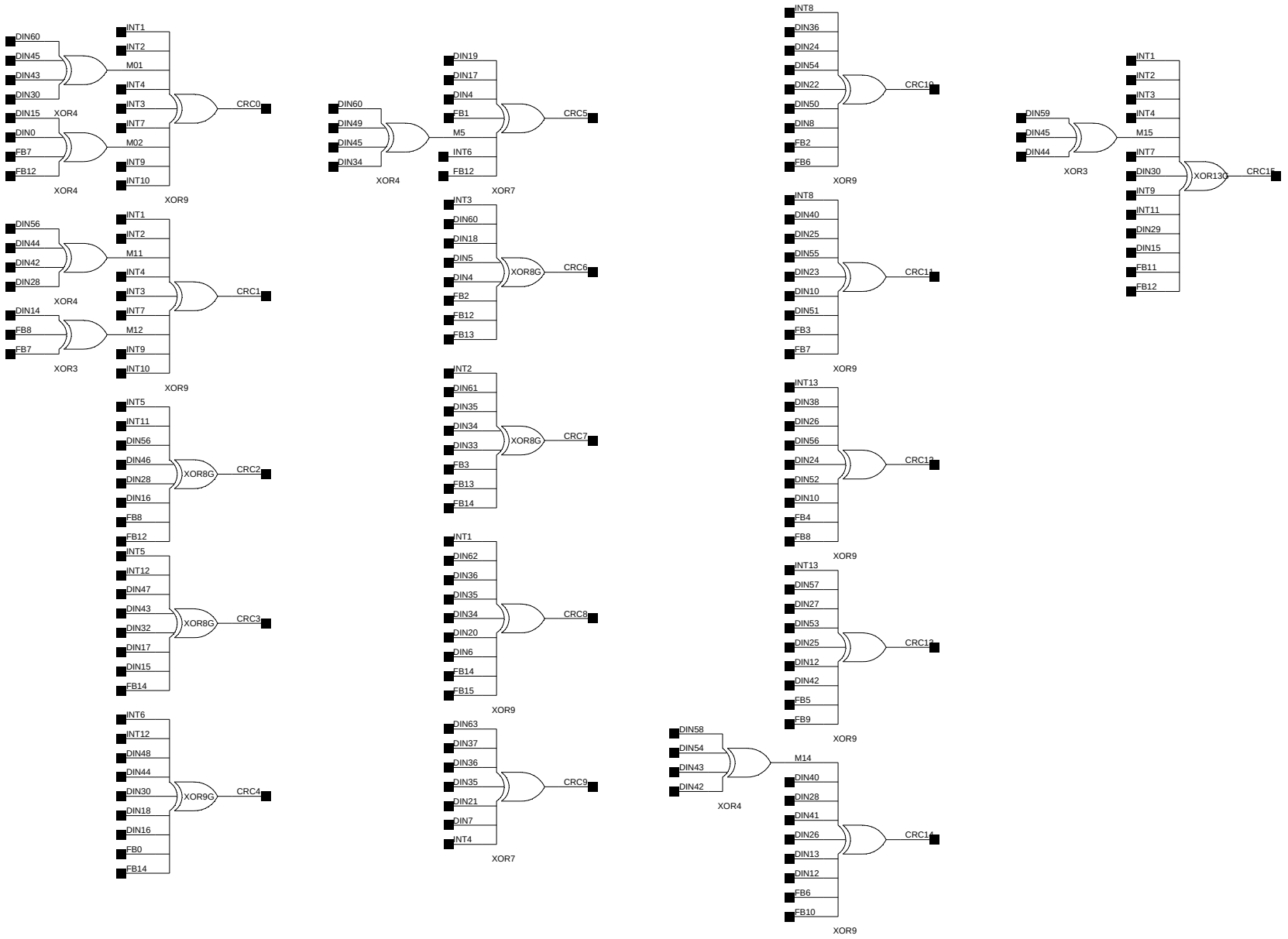


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:34	PARENT PAGE: 12C	PROJECT: D785C FILE: CRC22_64 . 2 PAGE: 14A

CRC-16 Primitive Polynomial: X^16+X^15+X^2+1, same as USB standard



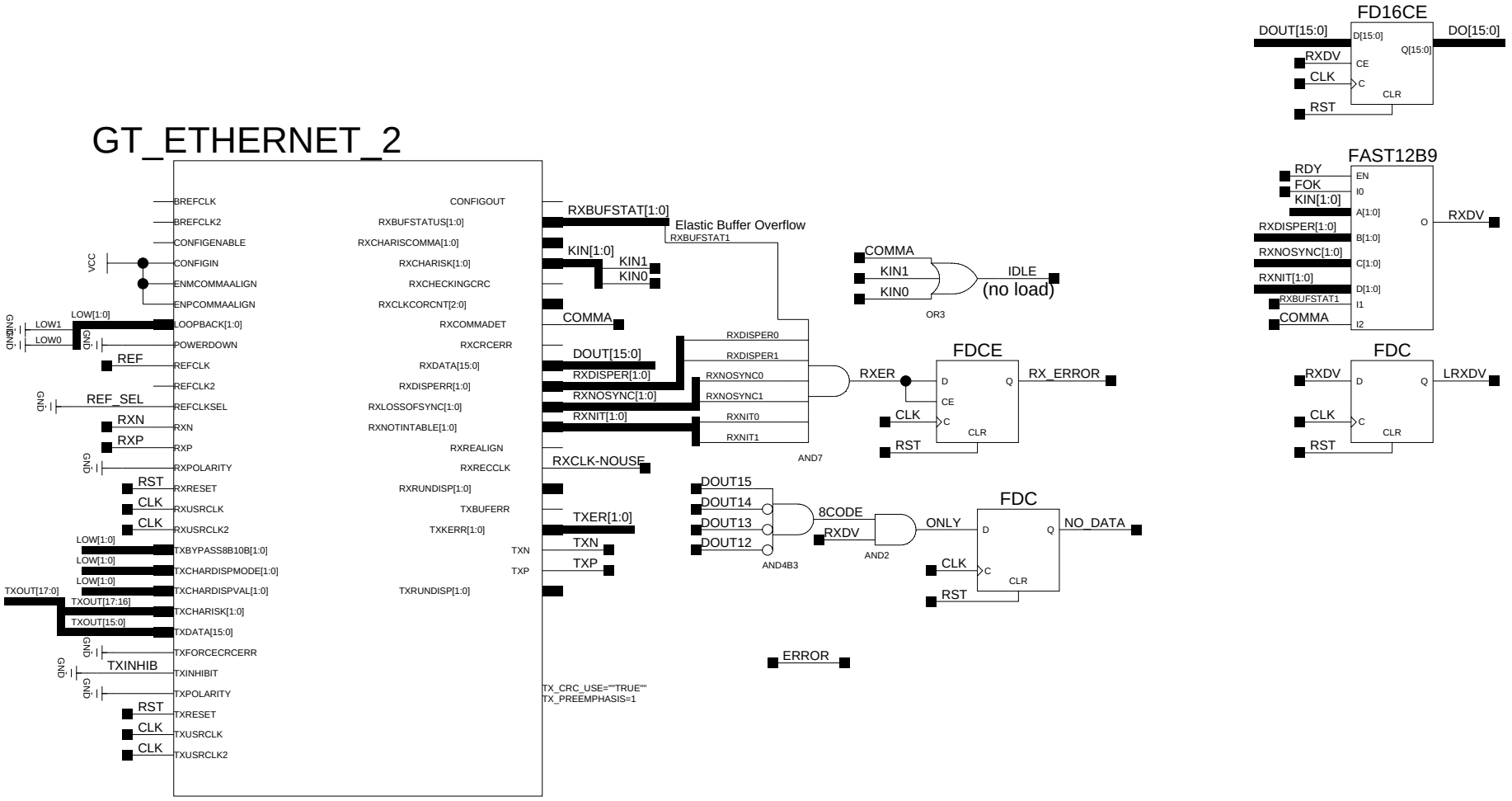
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	SLINK CRC16 Calculation, common components DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
			DATE 2-7-2005_17:29	FILE CRC16 . 1	PAGE 15A



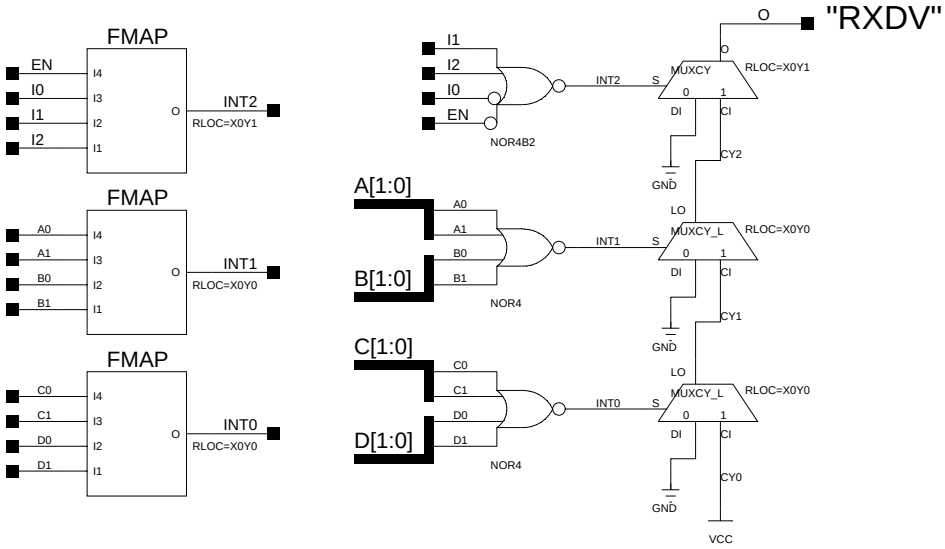
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: SLINK CRC16 Calculation DDU Slink Interface FPGA CMS CSC Electronics	BY: GU	PARENT PAGE: 12F	PROJECT: D785C
		DATE: 2-7-2005_17:29	FILE: CRC16 . 2	PAGE: 15B

Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.

---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.

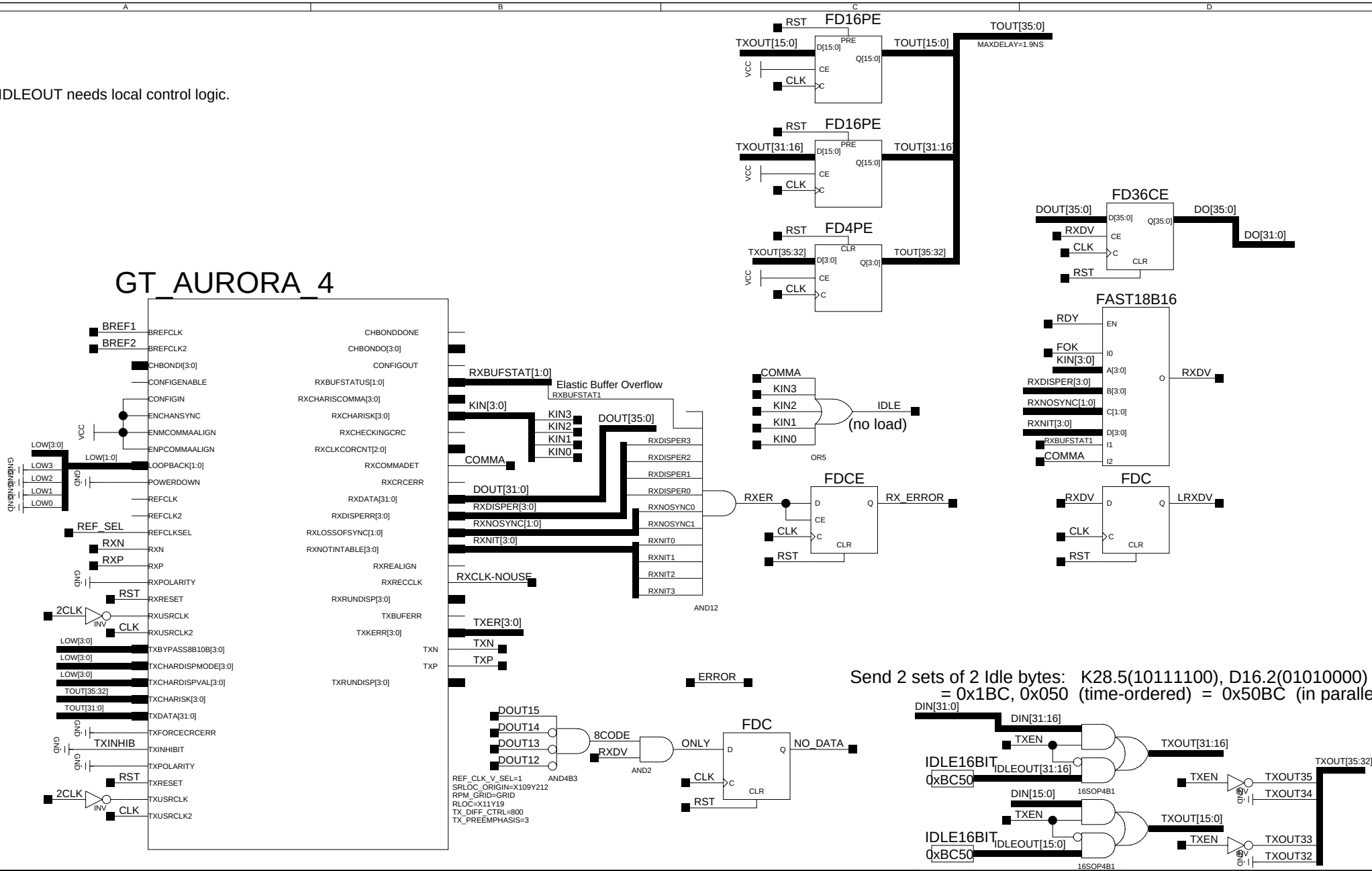


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Gigabit Ethernet Tranceiver DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:39	PARENT PAGE: 2E FILE: OUT_GBE . 1
		PROJECT: D785C	PAGE: 16

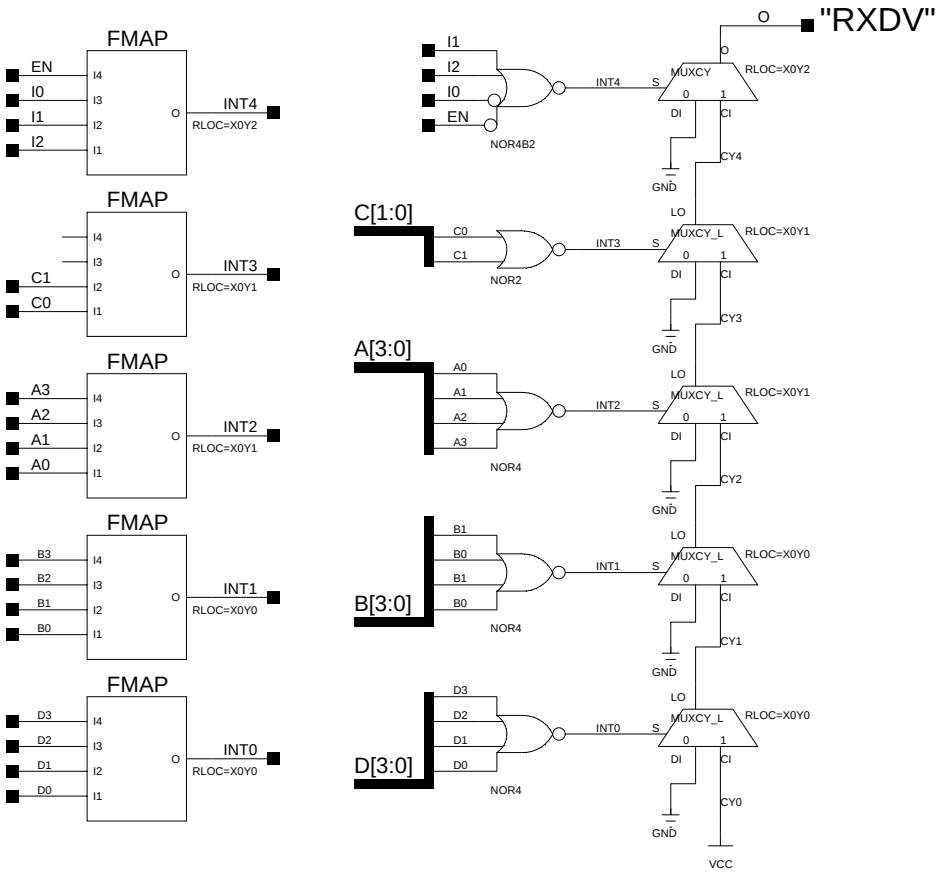


XILINX			JRG
Title:	FAST12B9		
Comments:	Custom Logic for DDU similar to: AND12B9		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

IDLEOUT needs local control logic.



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Multi Gigabit Tranceiver DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:44	PARENT PAGE: 2E FILE: OUT_UNIT . 1 PROJECT: D785C PAGE: 18



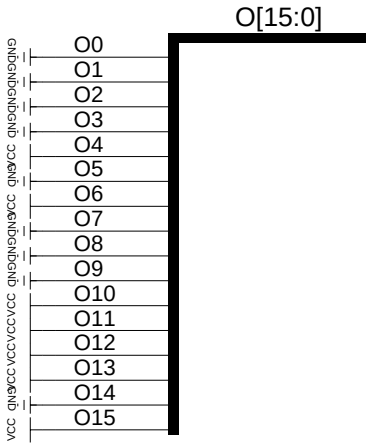
XILINX			JRG
Title:	FAST13B10		
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)

= 0x1BC + 0x050 (time-ordered)

= 0xBC50 (in parallel)

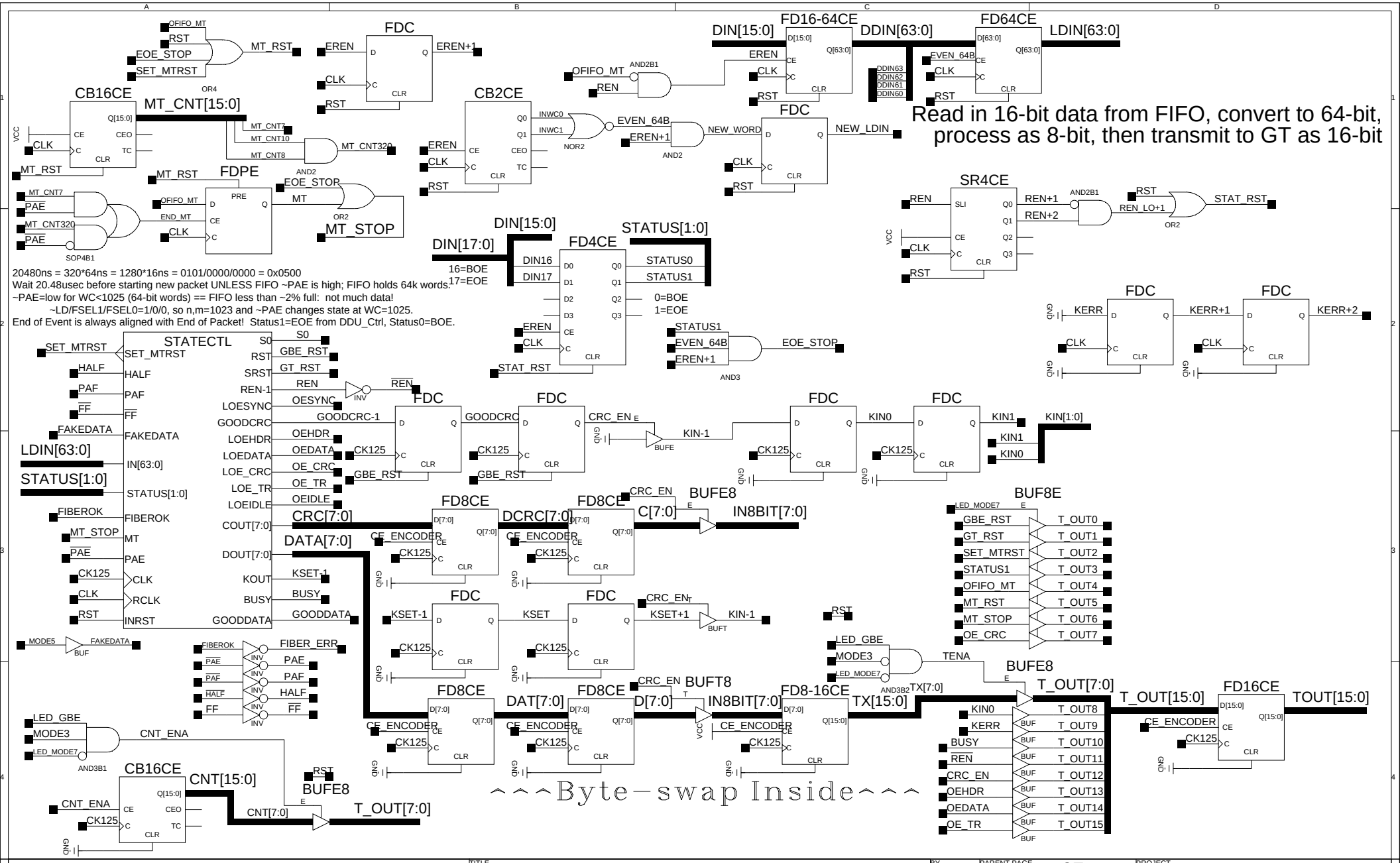


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

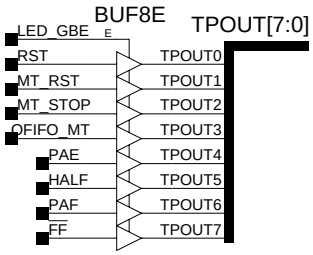
TITLE: Gigabit "Idle" Code
Constant Bus Settings
CMS CSC Electronics

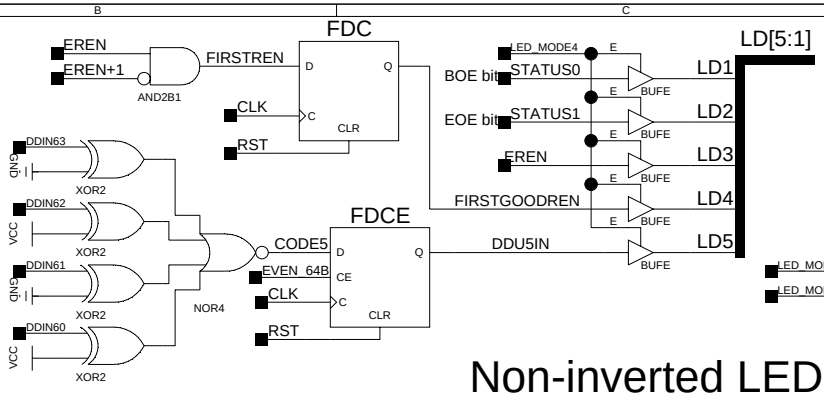
BY: JRG | PARENT PAGE: 18 | PROJECT: D785C

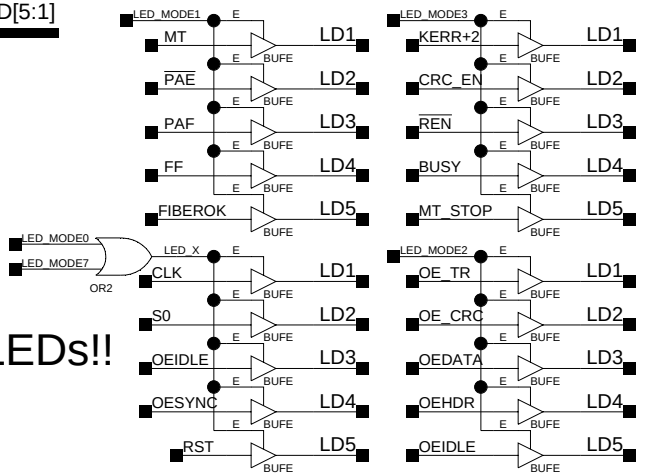
DATE: 1-26-2005_11:43 | FILE: IDLE16BIT . 1 | PAGE: 20



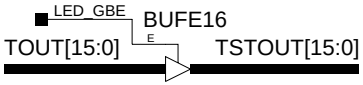
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:45	PARENT PAGE: 2F FILE: ETHCNTRL . 1
		PROJECT: D785C	PAGE: 21

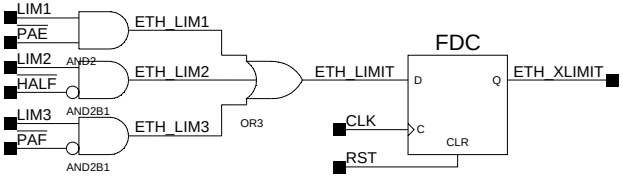


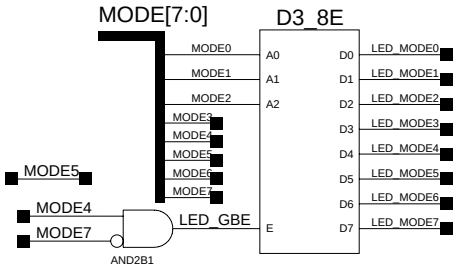




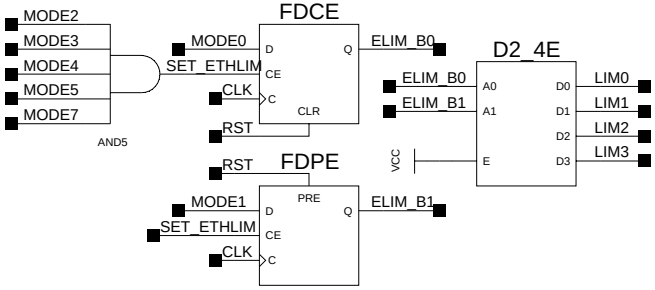
Non-inverted LEDs!!



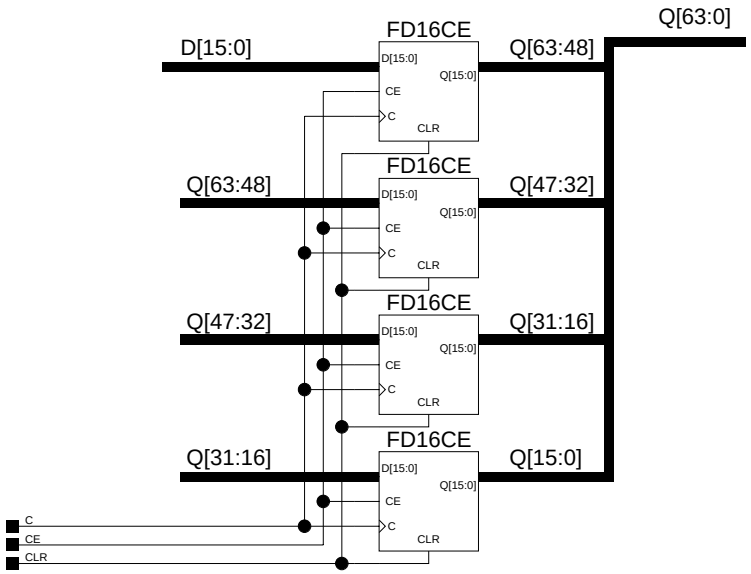




Find a better way to set ElimThresh bits!



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:45	PARENT PAGE: 2F FILE: ETHCNTRL . 2
		PROJECT: D785C	PAGE: 21A



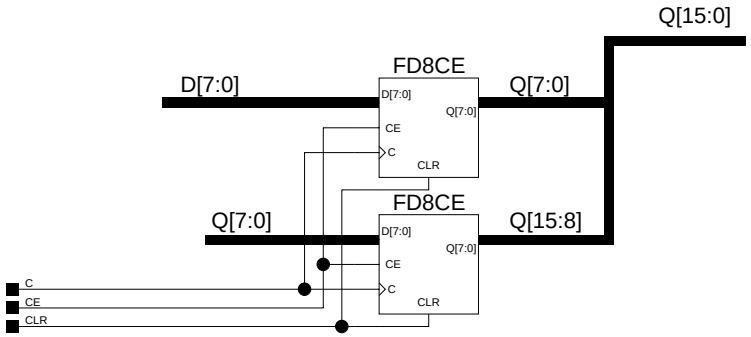
XILINX

JRG

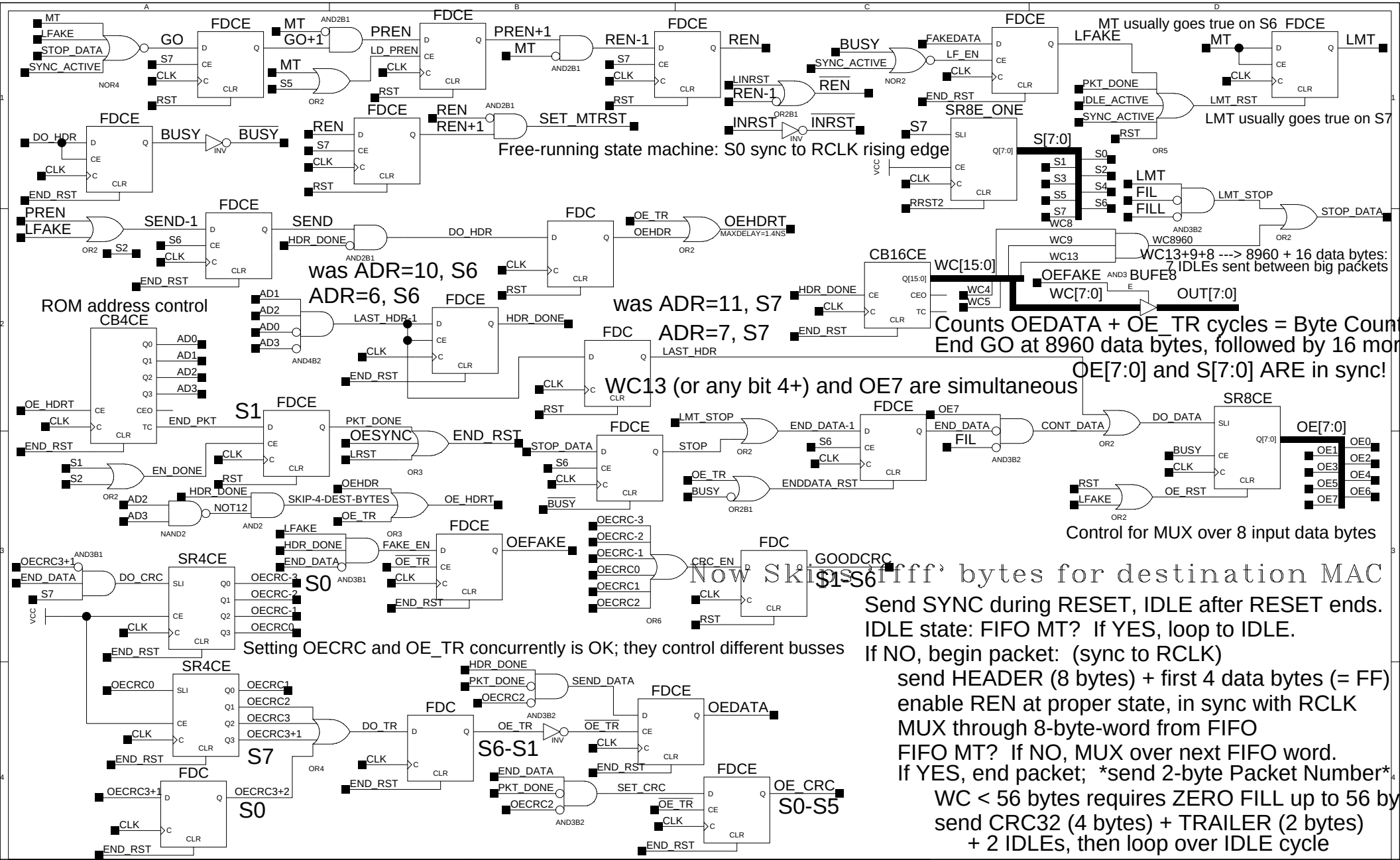
Title: VIRTEX Family FD16-64CE Macro

16-bit Bus Matching Register with Asynchronus Clear and Chip Enable

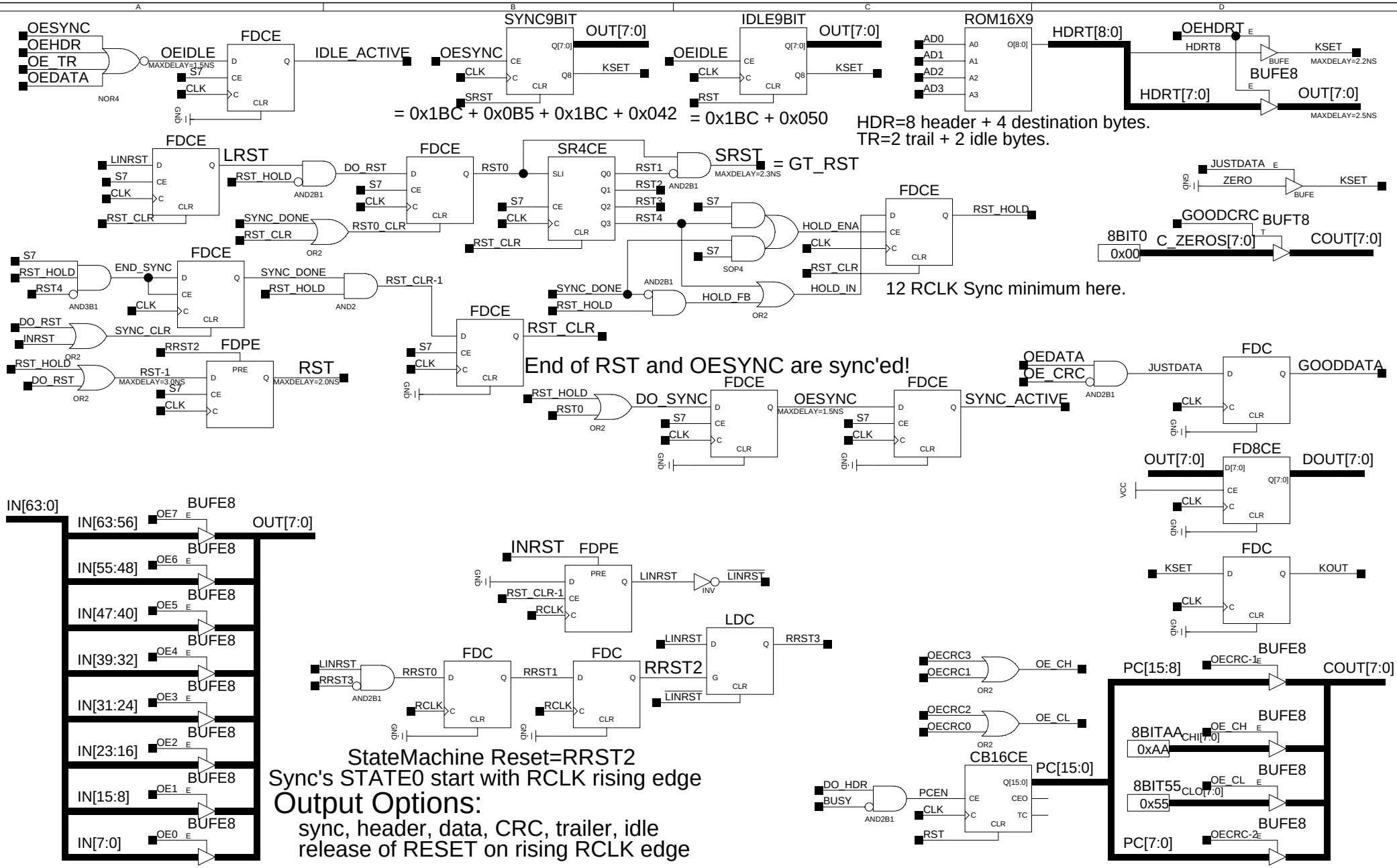
Date:	2nd February 2004	Ver:	1
Sheet Size: B		Rev:	A



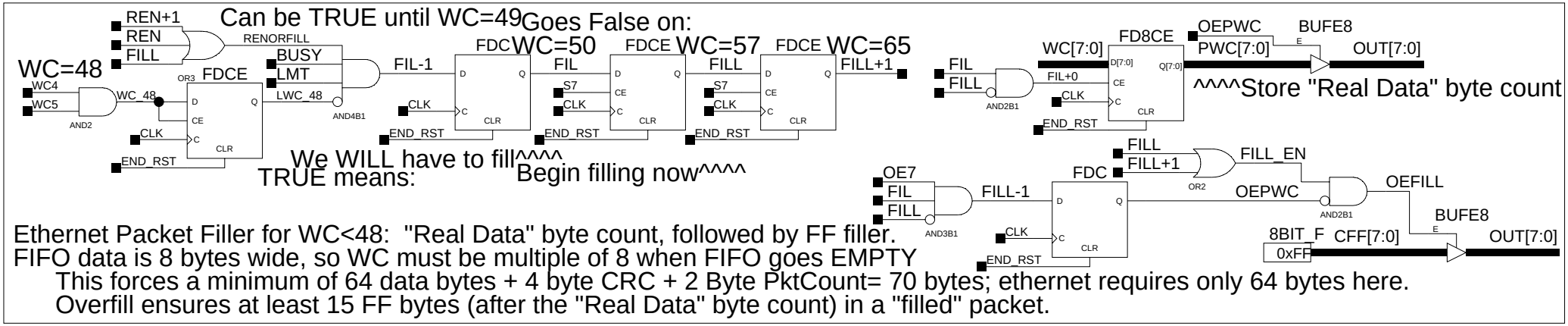
XILINX		JRG	
Title:	VIRTEX Family FD8-16CE Macro		
Comments:	8-16-Bit Bus Matching Register with Asynchronus Clear and Chip Enable		
Date:	4th February 2004	Ver:	1
Sheet Size: B		Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:50	PARENT PAGE: 21A FILE: STATECTL . 1
		PROJECT: D785C	PAGE: 24



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:50	PARENT PAGE: 21A FILE: STATECTL . 2
		PROJECT: D785C	PAGE: 24A



Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

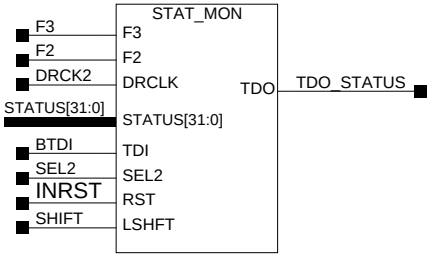
TITLE: State Machine Control
DDU Ethernet Logic
CMS CSC Electronics

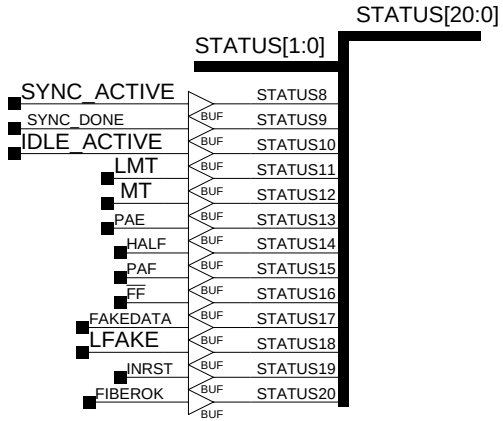
BY: JRG | PARENT PAGE: 21A | PROJECT: D785C
DATE: 1-26-2005_11:50 | FILE: STATECTL . 3 | PAGE: 24B

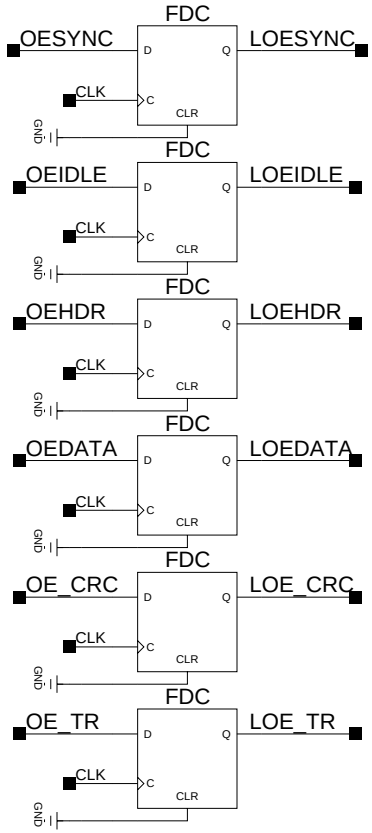
JTAG Instruction Decode

OpCode	Function [OpName]
0	No Operation [NOOP]
1	FPGA Reset
2	Check FPGA status, shift only [21 bits]
3	Check status with capture and shift test
4	
5	
6	
7	
8	
9	
10	
11	

Need JTAG Control (BTDI, SHIFT, SEL2, DRCK2 & F*) and TDO connections to B-Scan...

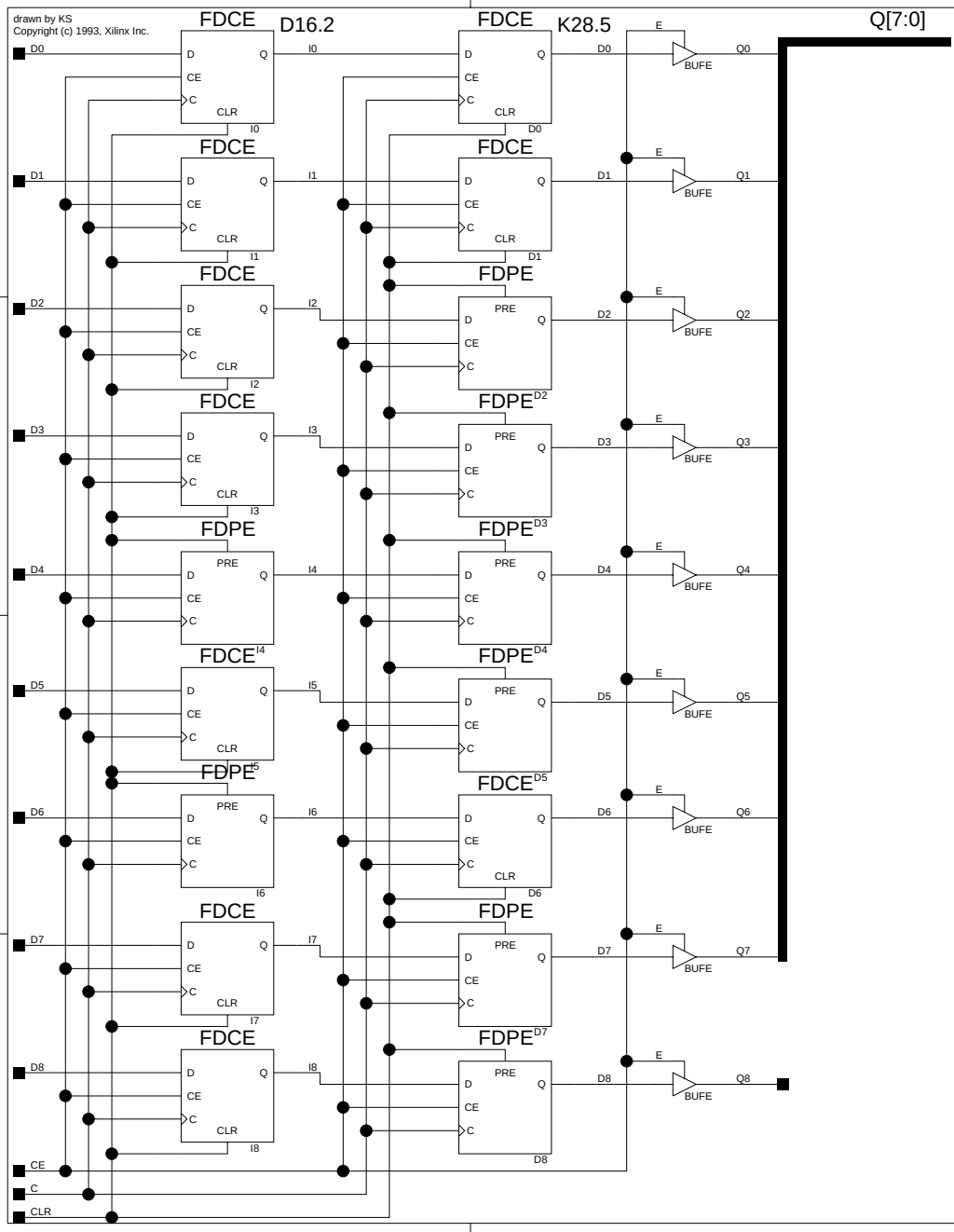






Debug Test Outputs

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Control Signals DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:50	PARENT PAGE: 21A FILE: STATECTL . 4
		PROJECT: D785C	PAGE: 24C

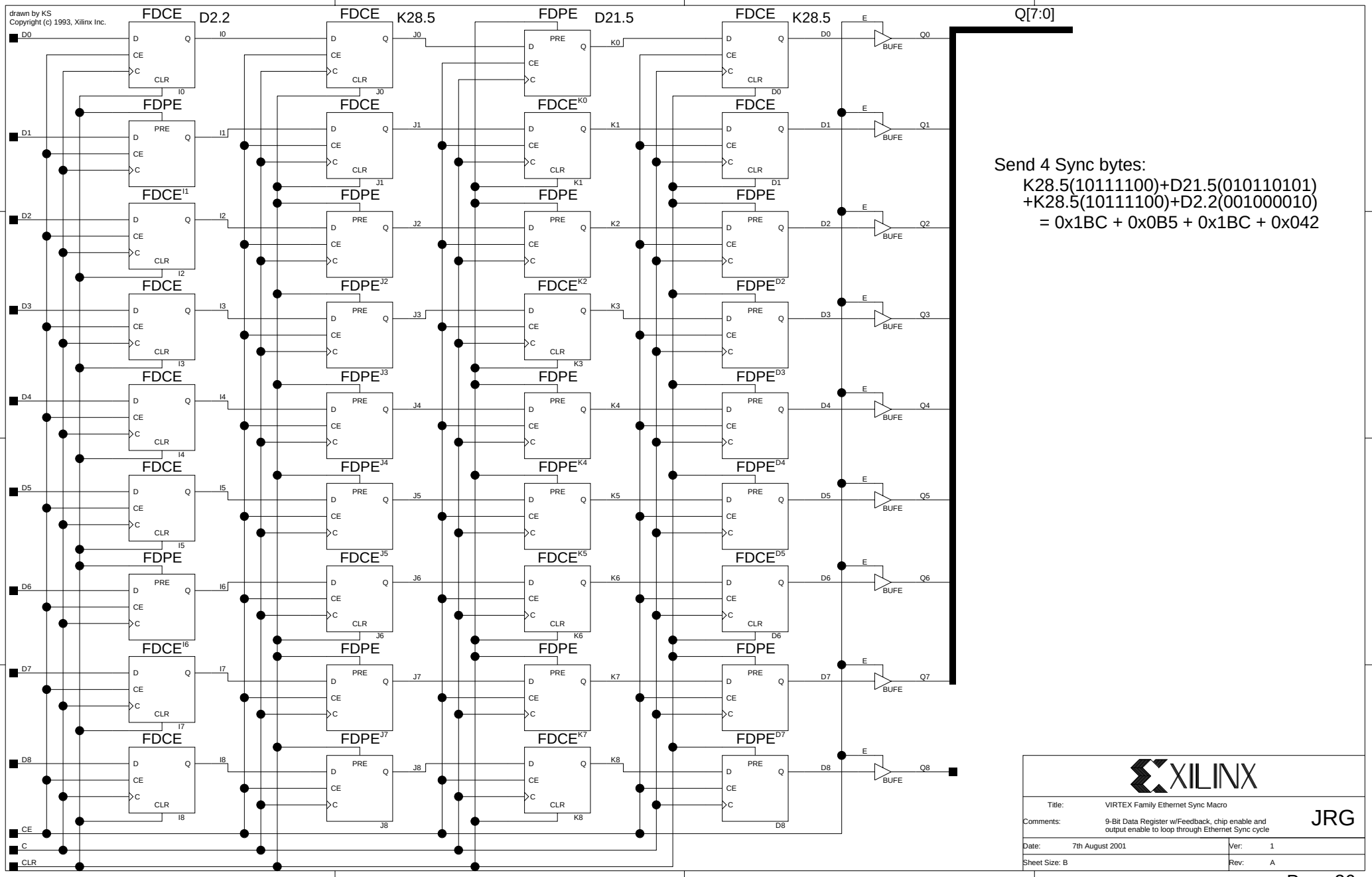


Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050

XILINX

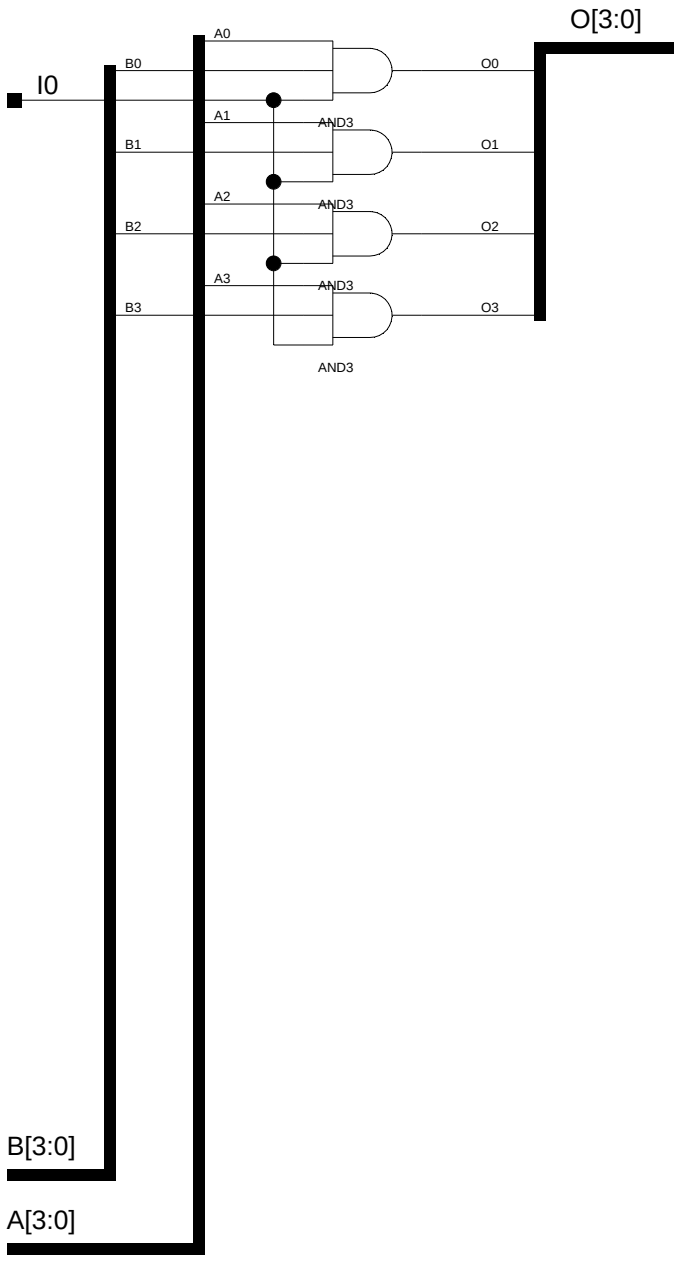
Title:	VIRTEX Family Ethernet Idle Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



Send 4 Sync bytes:

K28.5(10111100)+D21.5(010110101)
+K28.5(10111100)+D2.2(001000010)
= 0x1BC + 0x0B5 + 0x1BC + 0x042

Title:	VIRTEX Family Ethernet Sync Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Sync cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



XILINX

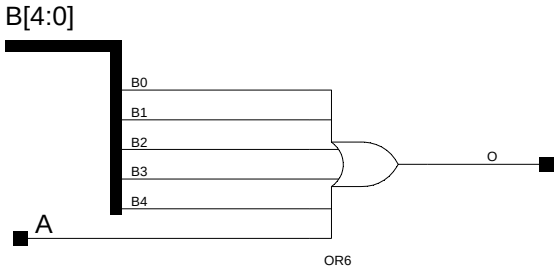
Title:VIRTEX Family 4-AND3COM1 Macro

Comments: 4-AND3 Bus Gate plus 1 common bit

JRG

Date:	1st October 2003	Ver:	1
Sheet Size: A		Rev:	A

drawn by KS



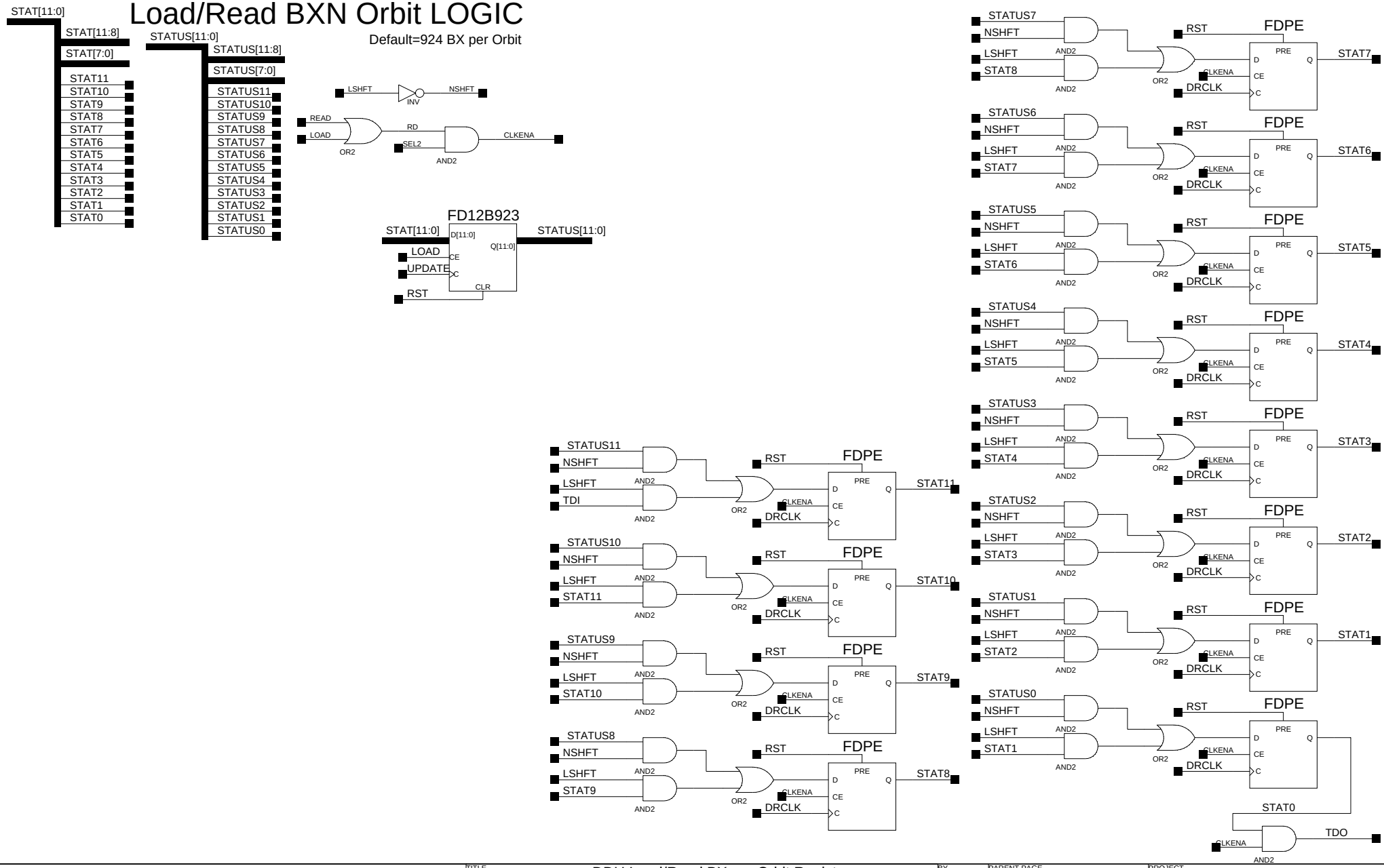
drawn by KS

XILINX

Title:	VIRTEX Family OR5+1 Macro		
Comments:	OR5 Bus Gate w/Common		JRG
Date:	27th December 2001	Ver:	1
Sheet Size: A		Rev:	A

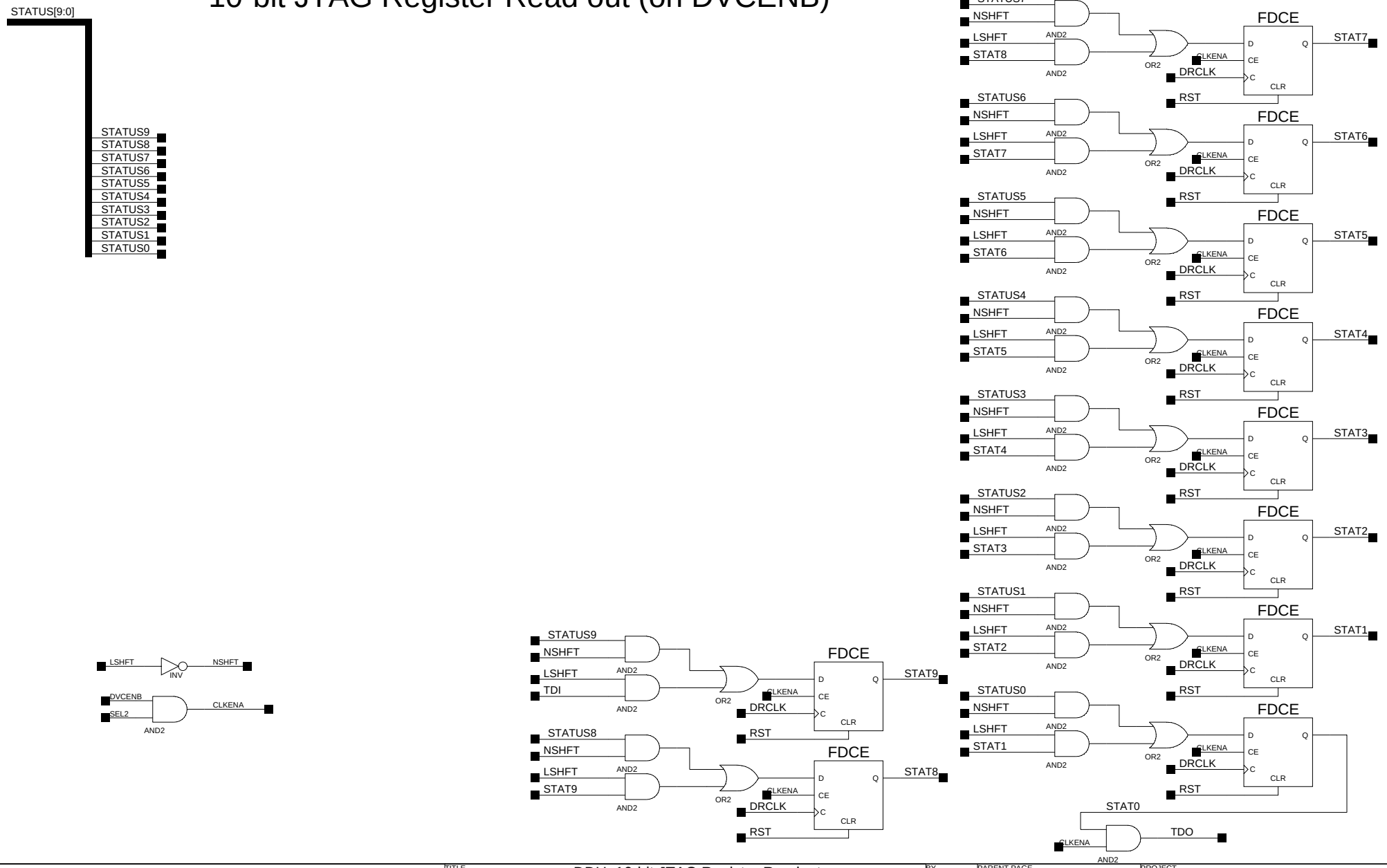
Load/Read BXN Orbit LOGIC

Default=924 BX per Orbit



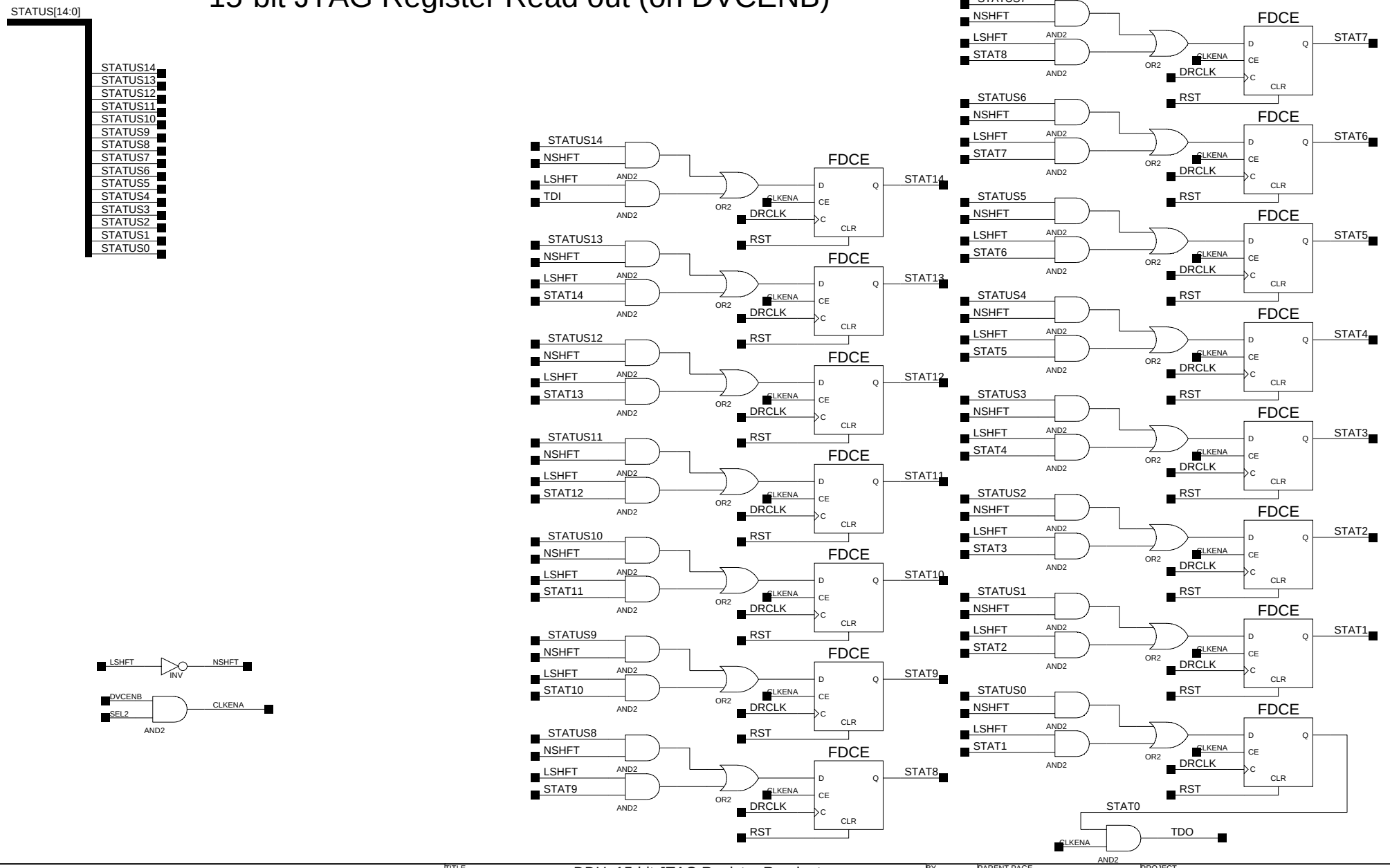
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Read BX per Orbit Register DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_12:11	PARENT PAGE: 3F FILE: BXN_REG . 1
		PROJECT: D785C	PAGE: 29

10-bit JTAG Register Read out (on DVCENB)



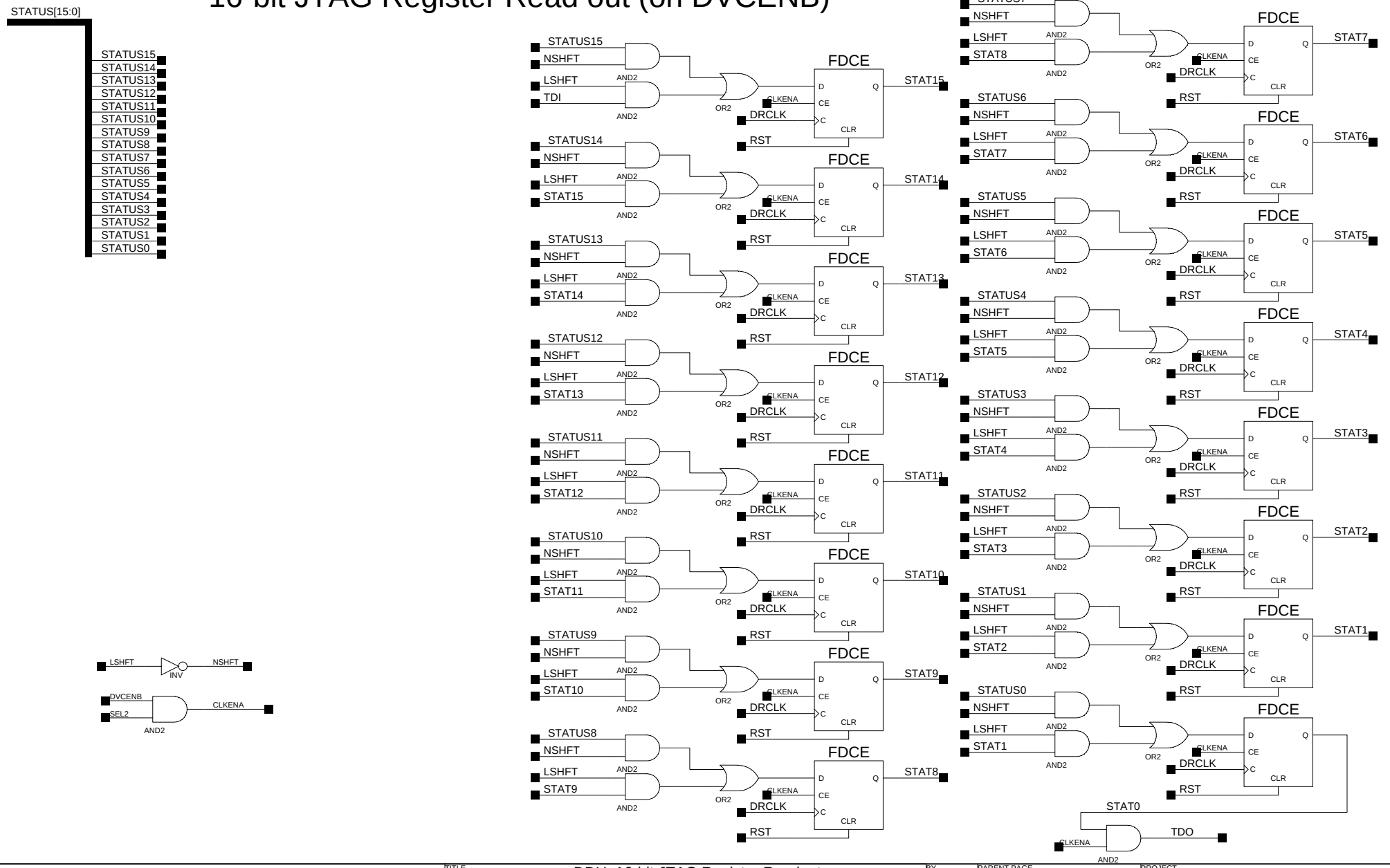
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 10-bit JTAG Register Readout DDU Input Control CMS CSC Electronics	BY: JRG	PARENT PAGE: 3F	PROJECT: D785
		DATE: 1-26-2005_12:16	FILE: CHECK_10 . 1	PAGE: 30

15-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 15-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_15 . 1	PAGE: 31

16-bit JTAG Register Read out (on DVCENB)

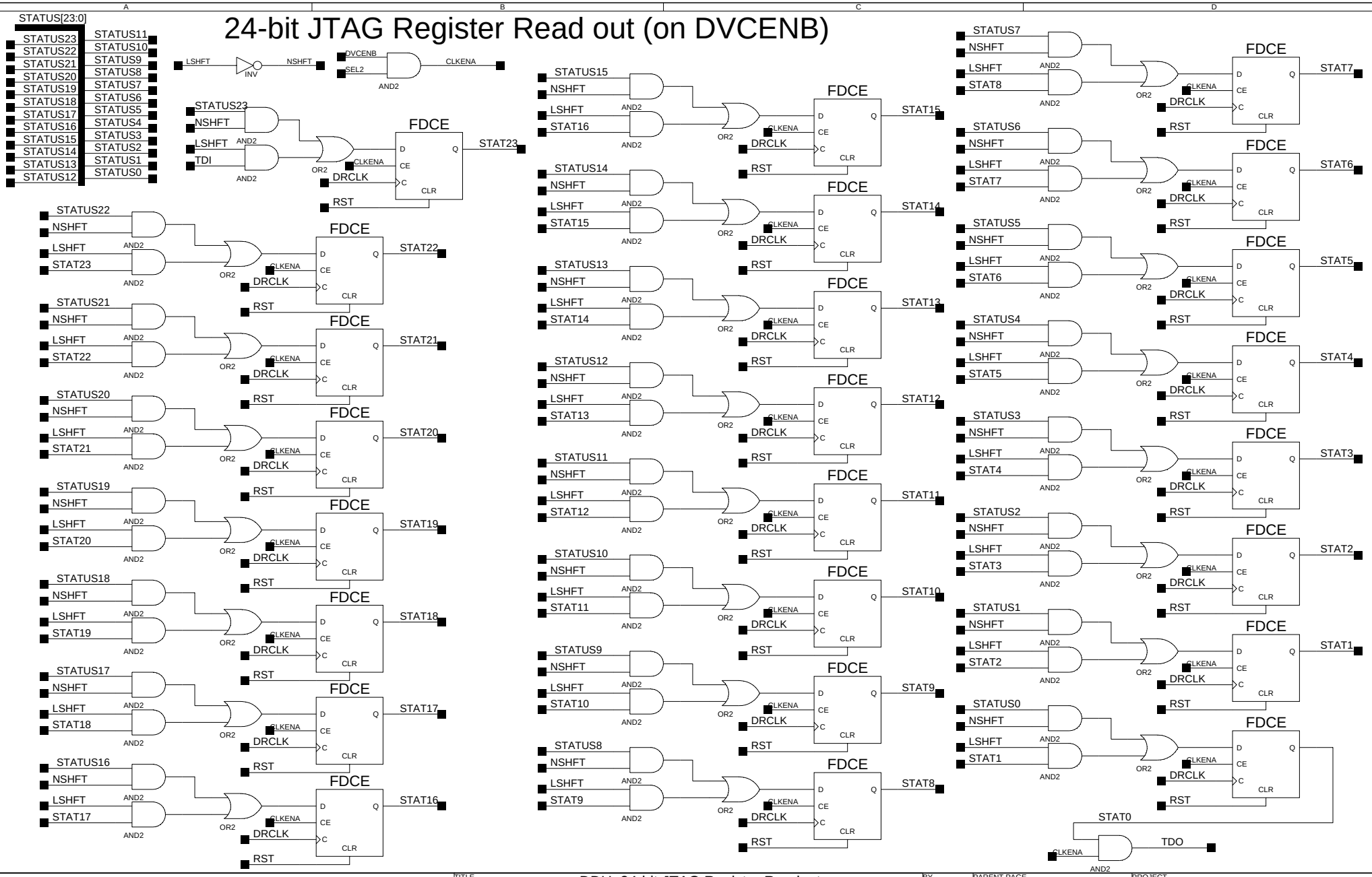


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU 16-bit JTAG Register Readout
DDU Controller
CMS CSC Electronics

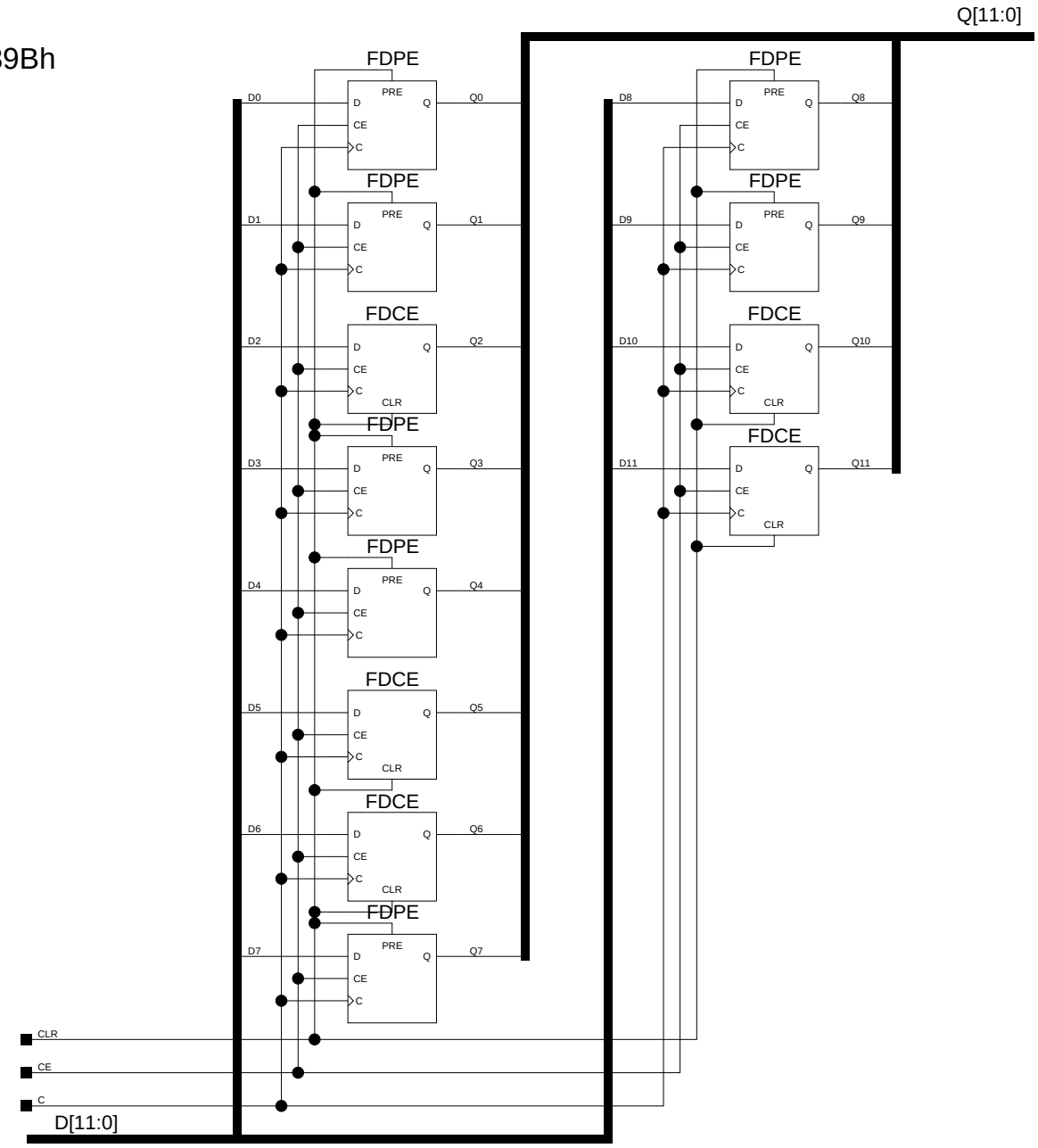
BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE	FILE	PAGE
1-26-2005_12:16	CHECK_16 . 1	32

24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:17	FILE: CHECK_24 . 1	PAGE: 33

def=923=39Bh



XILINX

Title: VIRTEX Family F12b923 Macro

Comments: 12-Bit D Flip-Flop with Preset to 923d and Enable

JRG

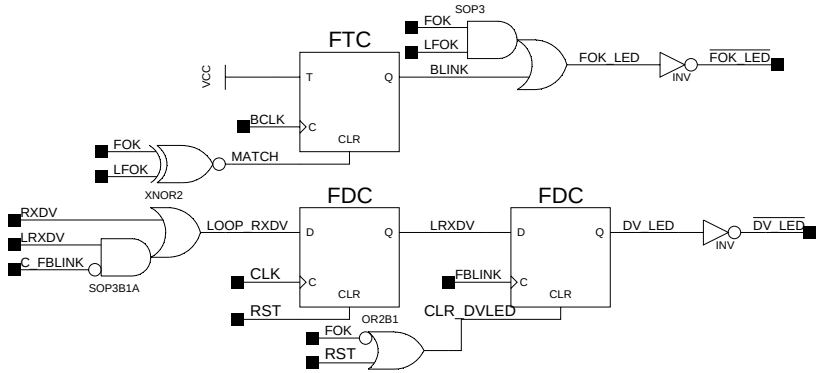
Date:	8th May 2003	Ver:	1
Sheet Size: B		Rev:	A

FOK LED

--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

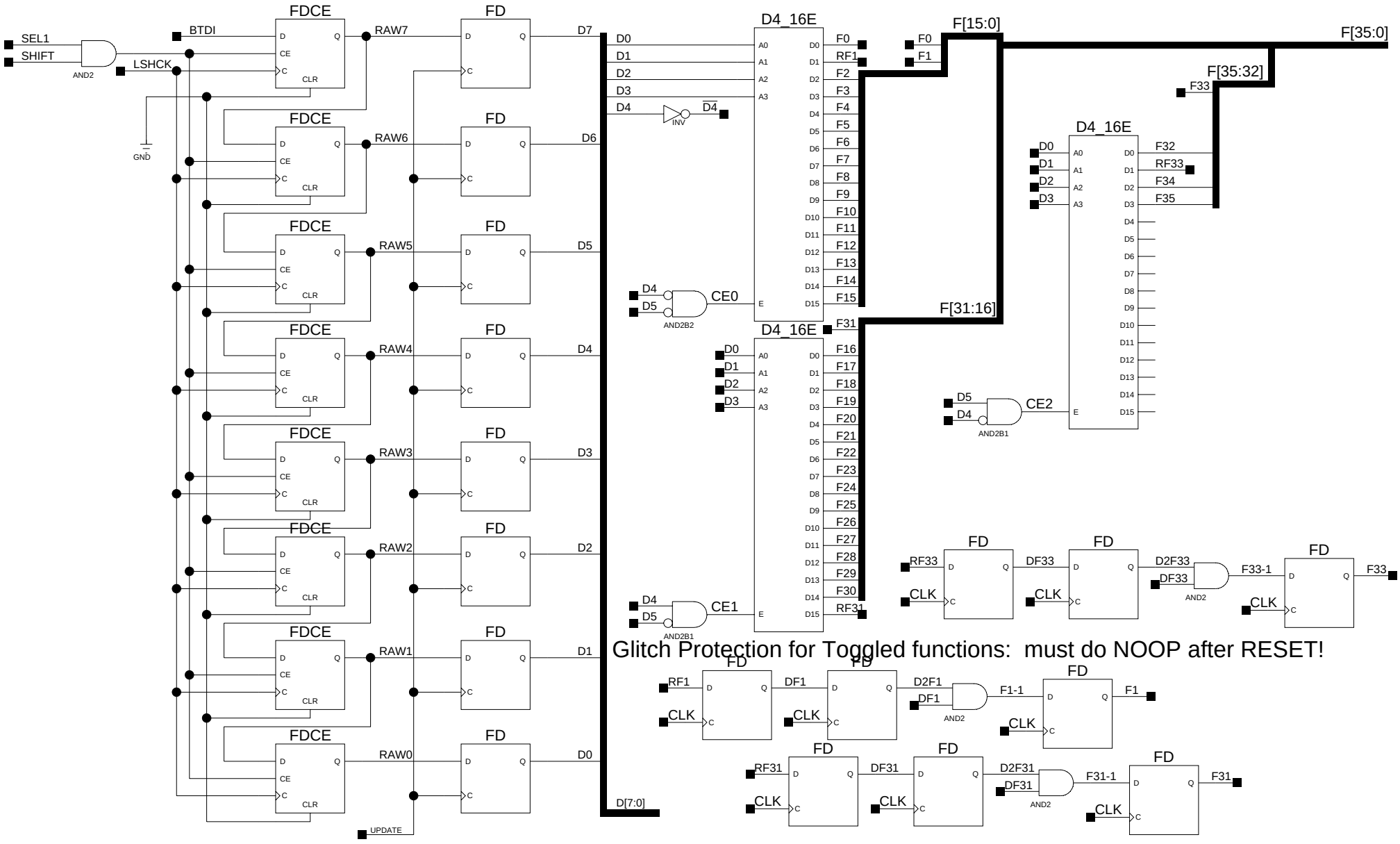
DAV LED

--LIT == Active Data Xmit
--OFF == No data to Xmit



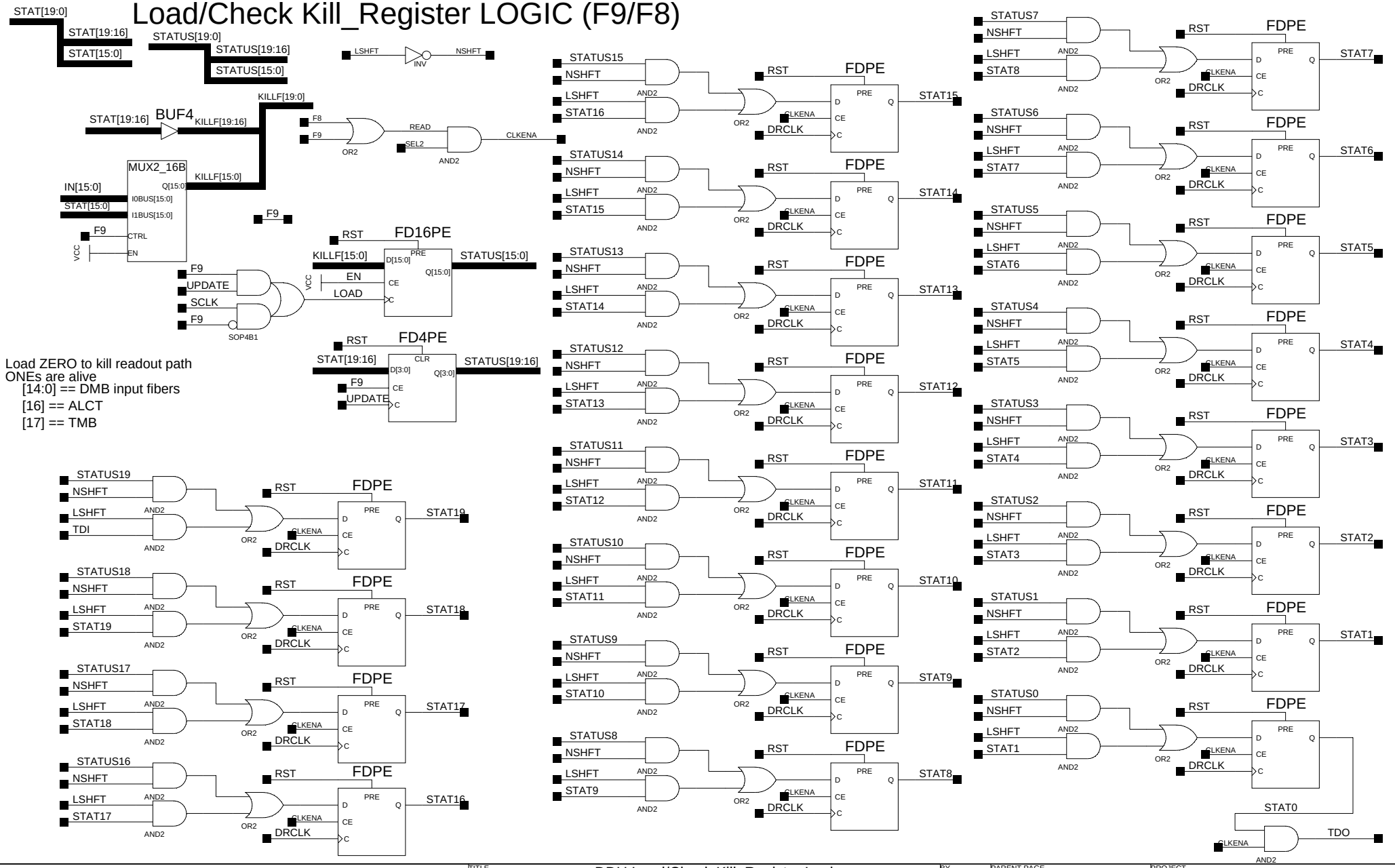
XILINX JRG

Title:	FIBERLED
Comments:	Custom LED Slow-Blink Control for Fiber Inputs
Date: 27th January 2004	Ver: 1
Sheet Size: B	Rev: A

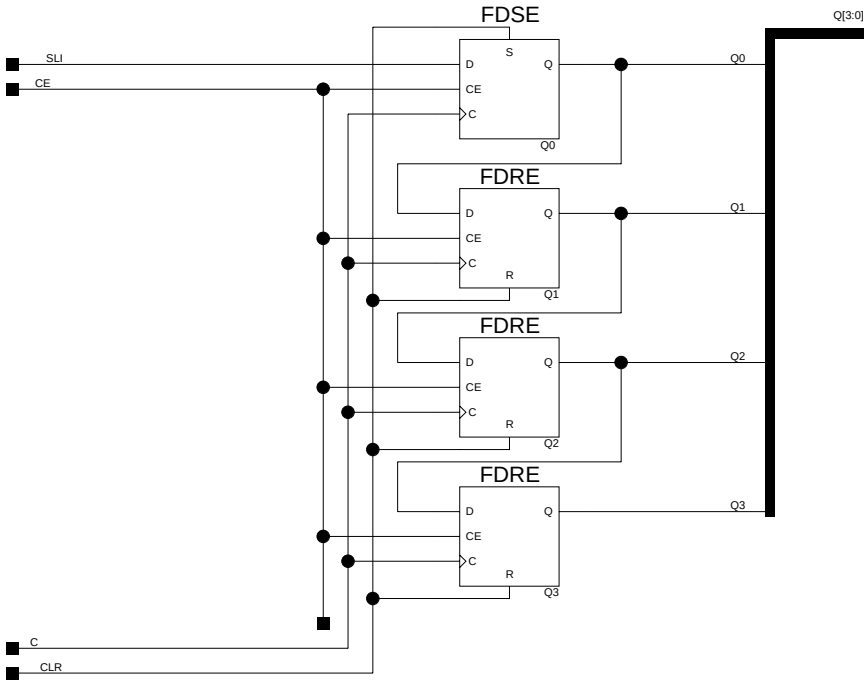


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Instruction Decode DDU Controller CMS CSC ELECTRONICS	BY: JRG PARENT PAGE: 3D DATE: 1-26-2005_12:19	PROJECT: D785C FILE: INSTRGDC . 1 PAGE: 36

Load/Check Kill_Register LOGIC (F9/F8)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Check Kill_Register Logic DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:20	FILE: KILL_REG . 1	PAGE: 37



drawn by KS

XILINX

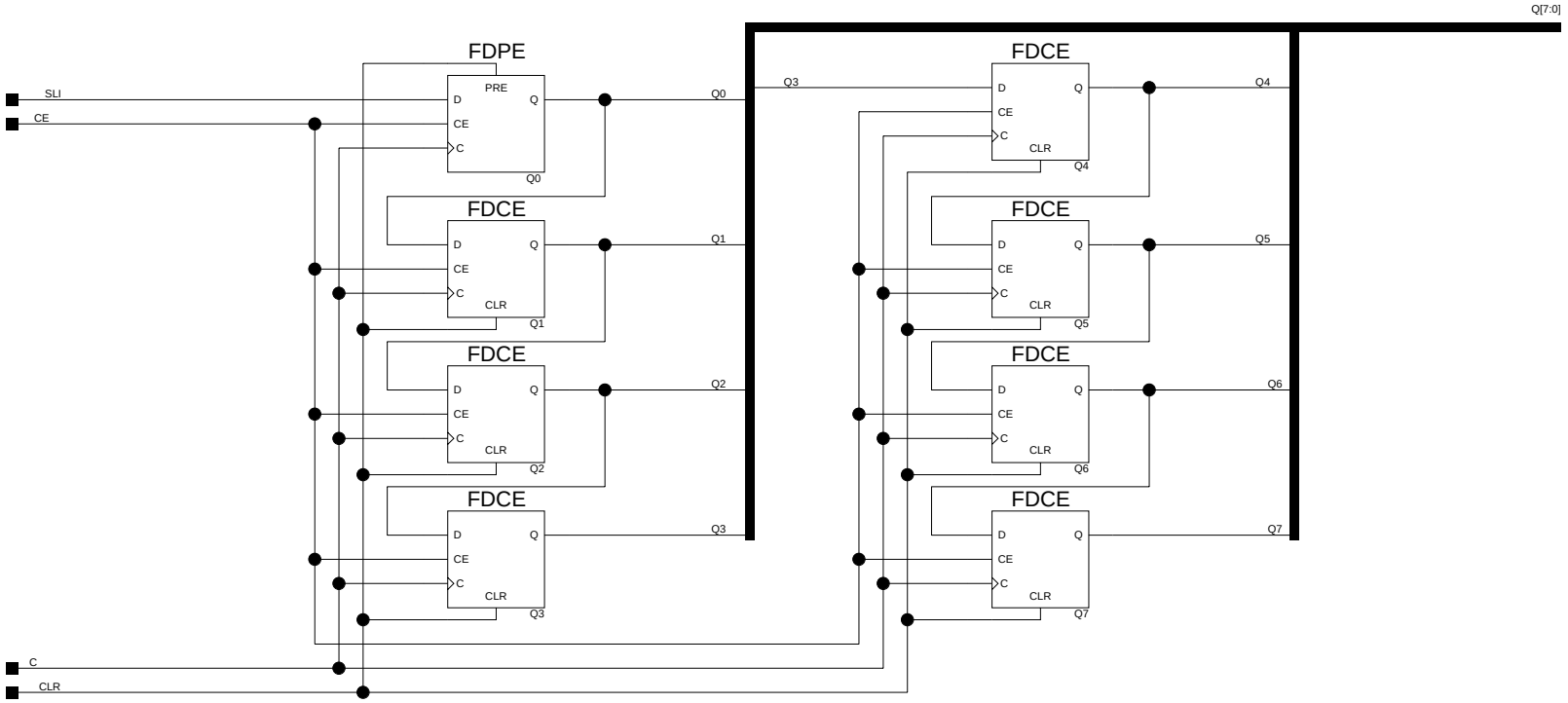
Title: VIRTEX Family SR4CE Macro

Comments: 4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset

JRG

Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A



drawn by KS

XILINX

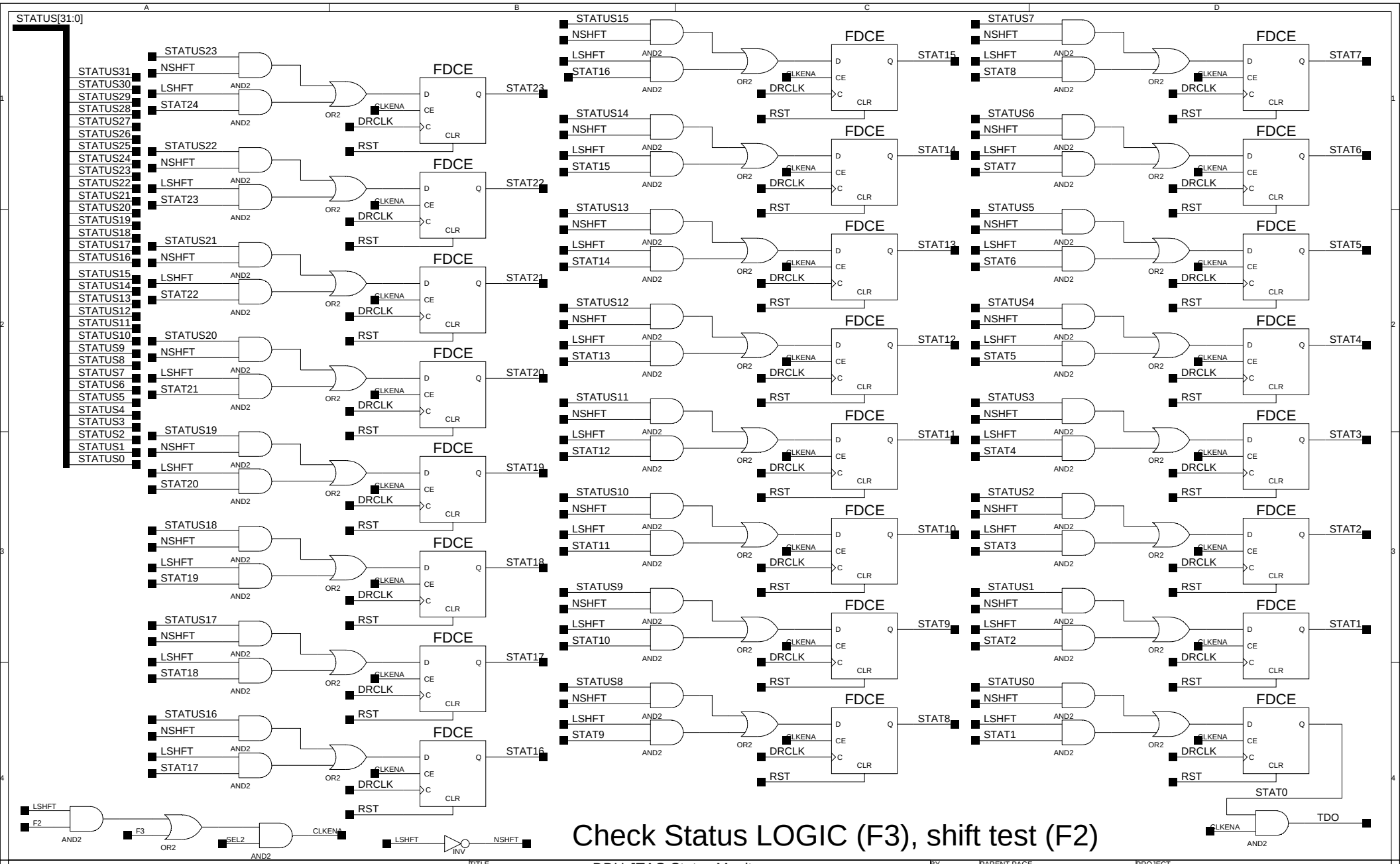
Title: VIRTEX Family SR8CE Macro

Comments: 8-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single one on Async Clr

JRG

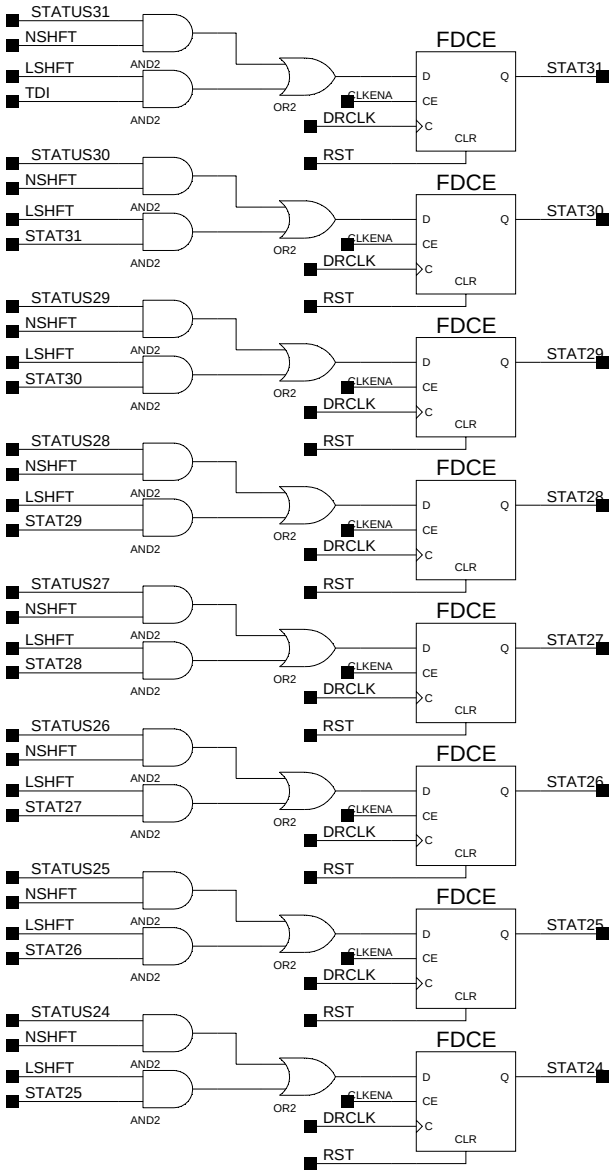
Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A



Check Status LOGIC (F3), shift test (F2)

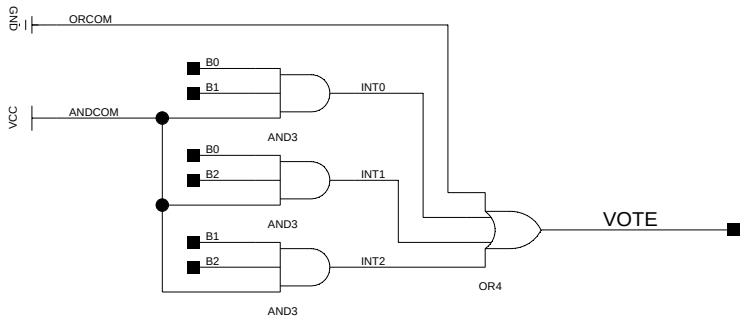
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D
		DATE: 1-26-2005_12:27	PROJECT: D785C
		FILE: STAT_MON . 1	PAGE: 40



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 3D | PROJECT: D785C
DATE: 1-26-2005_12:27 | FILE: STAT_MON . 2 | PAGE: 40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Vote 2 out of 3 DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 12C	PROJECT D785C
		DATE 1-26-2005_12:28	FILE VOTE3 . 1	PAGE 41