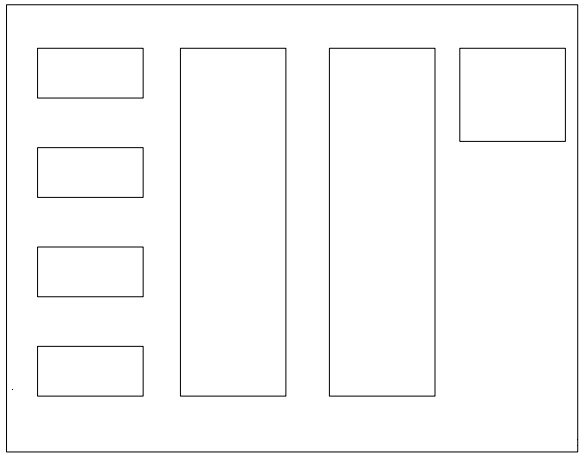
Project Directory: M:\WV\D785\D785N
Pads Directory: M:\WV\D785\D785N\PADS\B785N\
Pads Library: M:\WV\D785\D785N\PADS\B785N\B785N.PT4

D785N

CMS CSC DDU VERSION 4

BLOCK



ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

JTAG0 (Emergency VME) ---> CPLD (driven by cable or FPGA1)
JTAG1 (DDU Control) ---> EPROM1 ---> FPGA1 (driven by cable, CPLD or FPGA1): for now TDO1 goes only to cable, but future version should feed TDO1 back into FPGA1
JTAG2 (GBE Control) ---> EPROM2 (driven by cable or FPGA1)
JTAG3 (GBE Control) ---> FPGA2 (driven by FPGA1)

mojo

MODIFICATIONS TO D785A PCB

1. PULLUP'S ADDED TO SELECT JTAG TDO PINS. THE FPGA TDO PINS ARE OPEN DRAIN OUTPUTS. (330Z to 2.5V)
   TDO2
   TDO3
   TDO6
2. THE ORIGINAL SERIES JTAG PATH OF THE CONTROLLER PROM1>PROM2>FPGA WAS SPLIT INTO TWO PATHS
   U21 PIN #31 PROM TDO PIN WAS LIFTED FROM PAD.
   U21 PIN #31 PIN GOES TO VME FPGA PIN #AA15 (PROM TDO PIN)
   U21 PIN #31 PAD GOES TO VME FPGA PIN #AB15 (FPGA TDI PIN)
3. RESISTOR DIVIDER ON JTAG HEADER. TO PROTECT 2.5V TOLERANT I/O FROM THE 5V MOJBLASTER.
   R125, R126, R128 CHANGED TO 100Z
   R122, R127, R129 CHANGED TO 330Z
   REMOVE R16 (PULLDOWN ON TCK1). THIS WAS REDUNANT WITH THE RESISTOR DIVIDER.
4. R/C filter added to the DS1033z for hardrst.
   (after programming, the current would increase causing the voltage level to fall

   this drop in voltage would cause the reset debouncer to retrigger.
   The power pin was lifted and a 220Z and 47uF capactor were installed to minimize the voltage drop effect.

5. The SD pin from input optical transceiver is a 3.3V signal feeding to 2.5V I/O banks.
   Causes current surges

   330Z pulldowns were used to help draw some of the current and
   also keep the FOK signal from floating with no fiber unit installed

6. Switch the 2.5V regulator to a TI unit due to large dropout and maximum current to be exceeded.
   this drop in voltage would cause the reset debouncer to retrigger.
   The power pin was lifted and a 220Z and 47uF capactor were installed to minimize the voltage drop effect.

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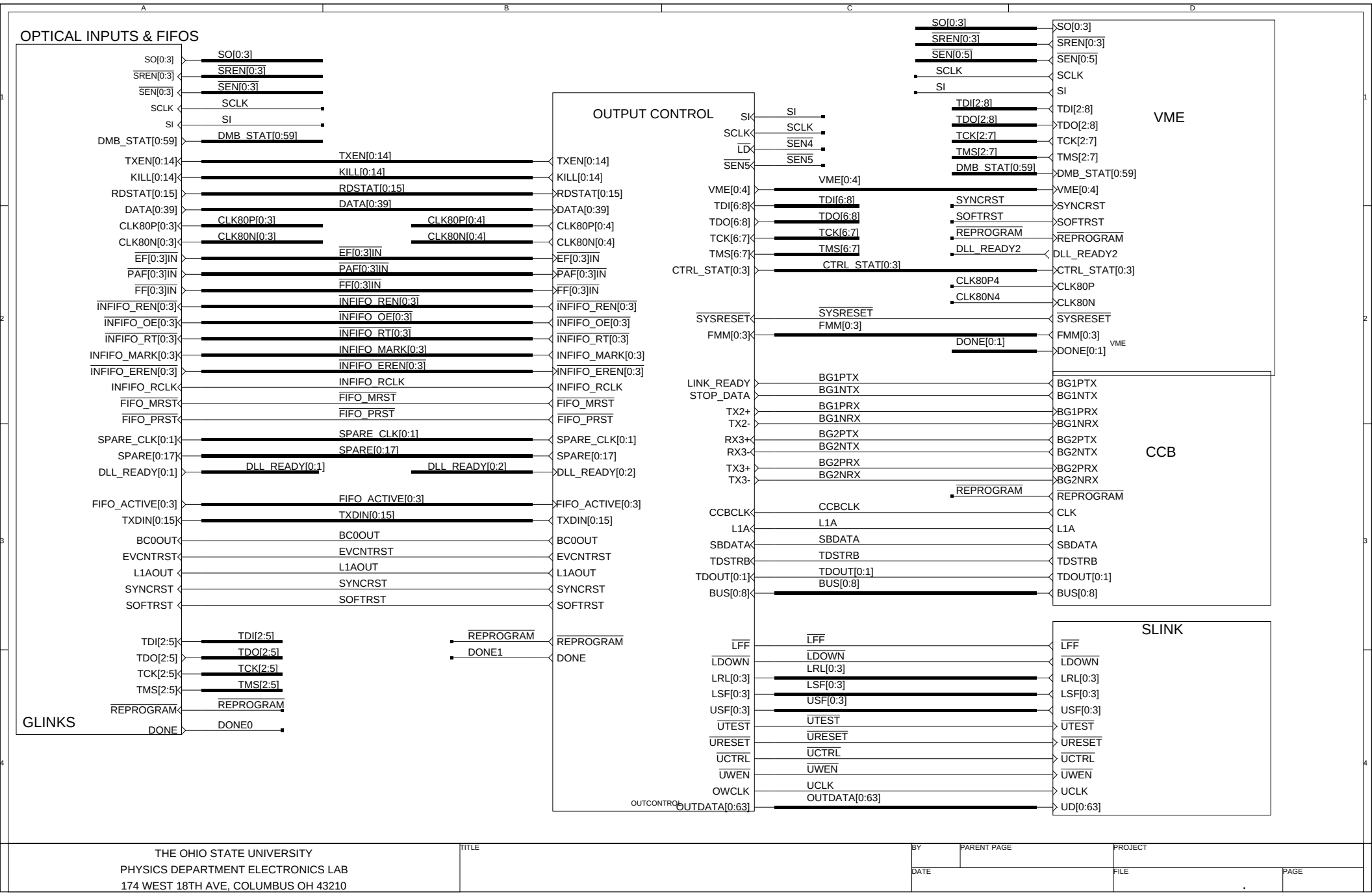

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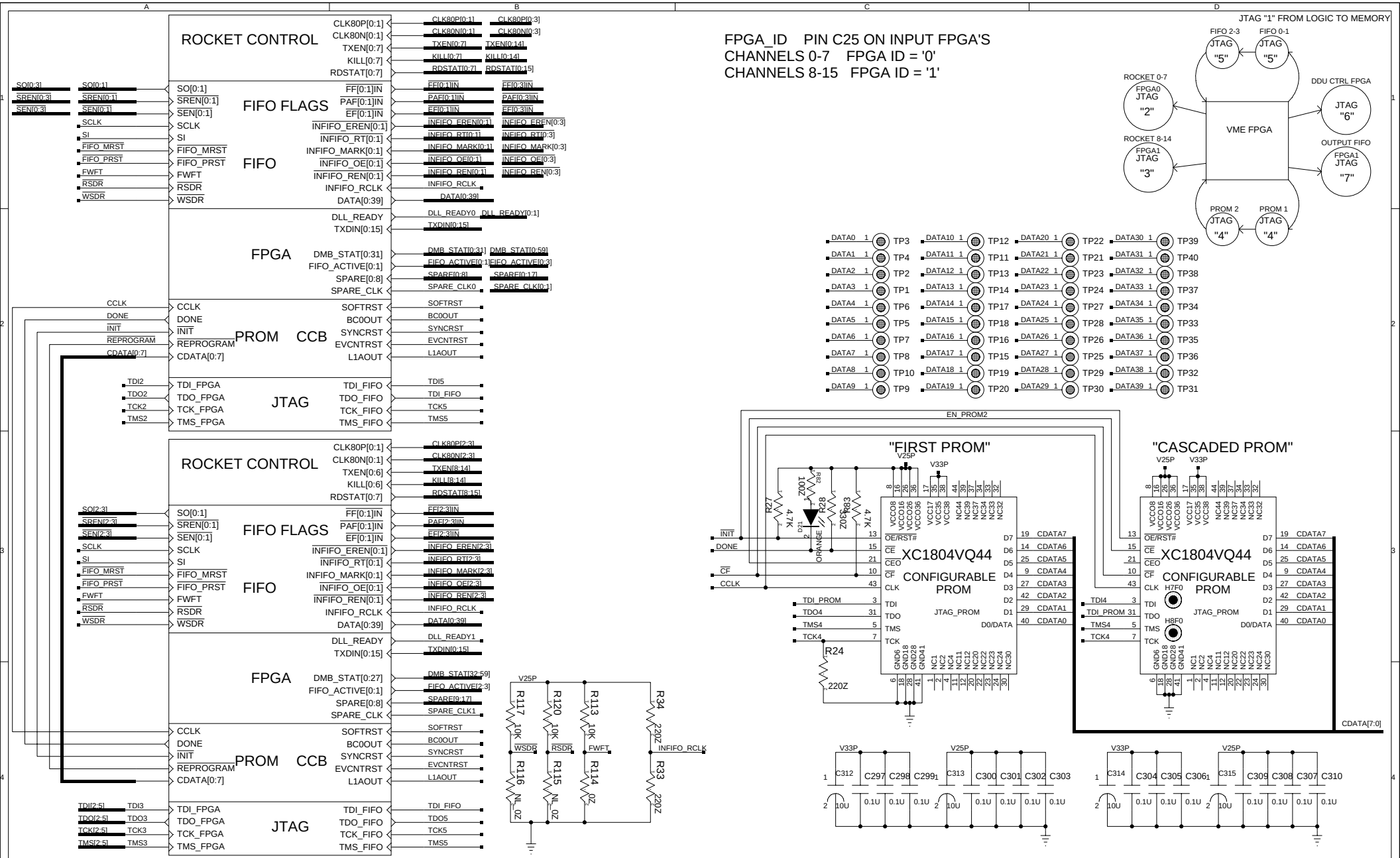
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE

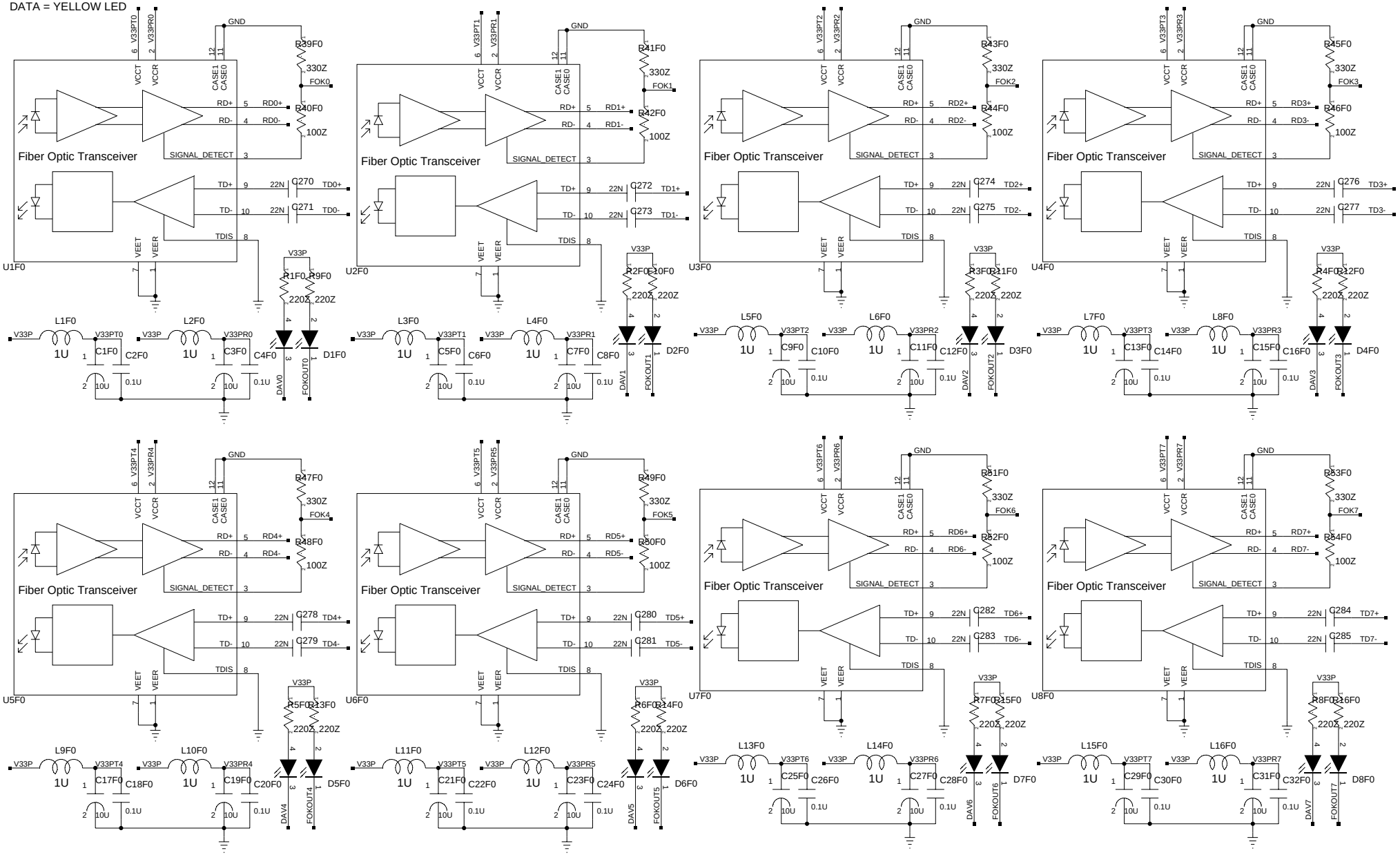
BY | PARENT PAGE | PROJECT

DATE | FILE | PAGE

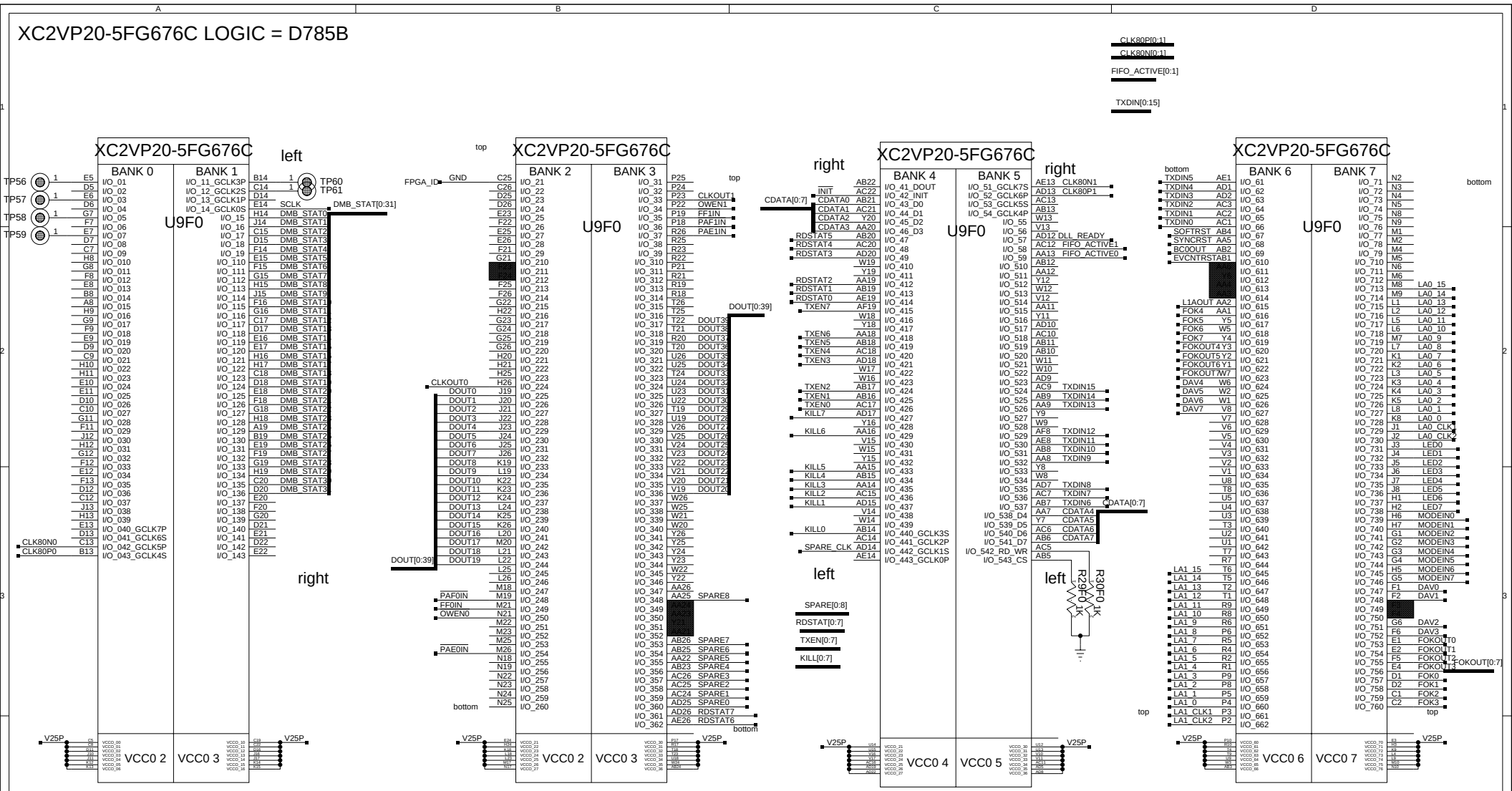


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: INPUT BLOCK FULL DDU CMS CSC ELECTRONICS	BY: dch DATE: 4-13-2004_16:06	PARENT PAGE PROJECT: D785A FILE: GLINKS . 1 PAGE: 2

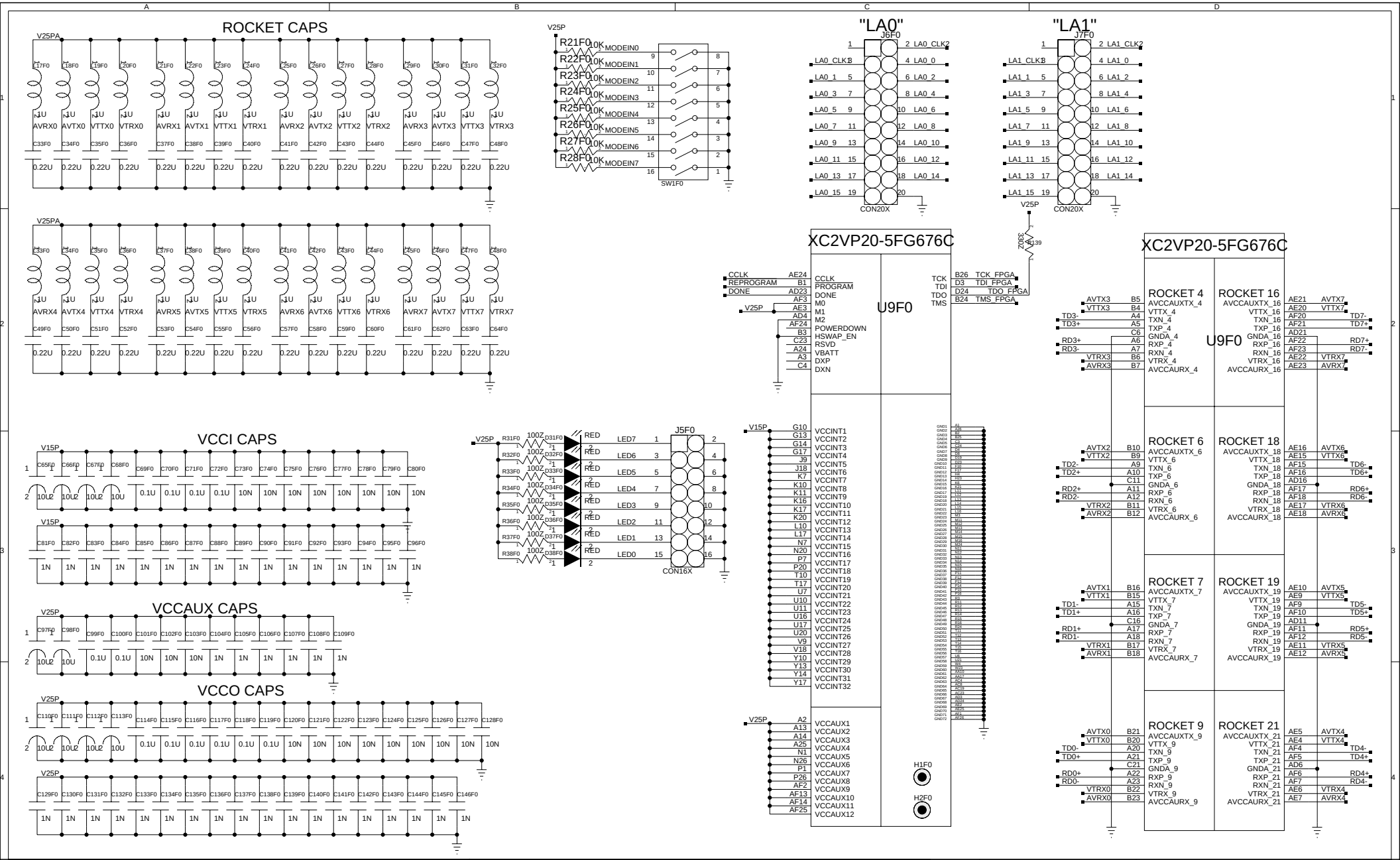
FOK = GREEN LED
DATA = YELLOW LED



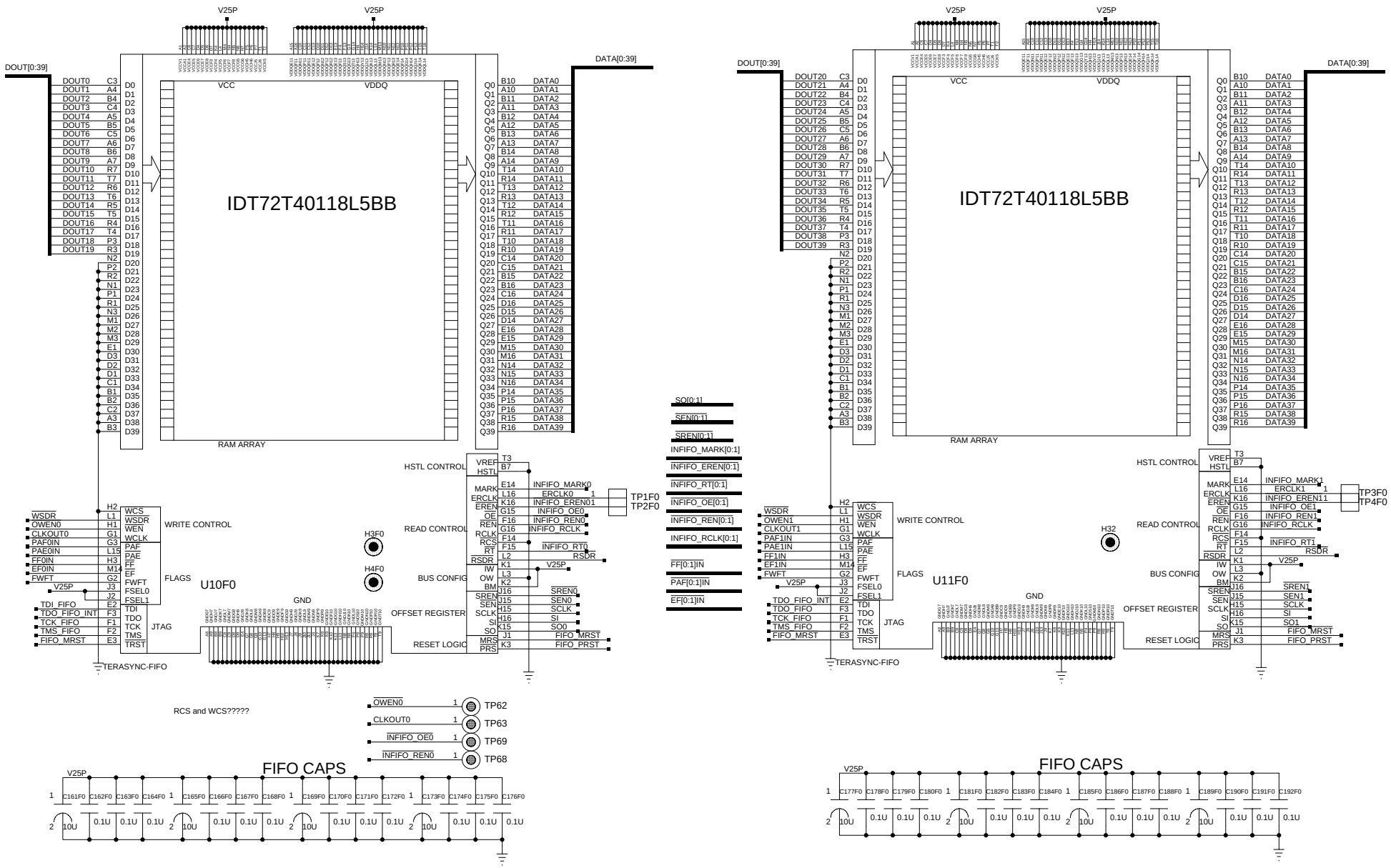
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH	PARENT PAGE:	PROJECT: D785A
		DATE: 11-15-2004_10:52	FILE: INPUTF0 . 1	PAGE: 2A



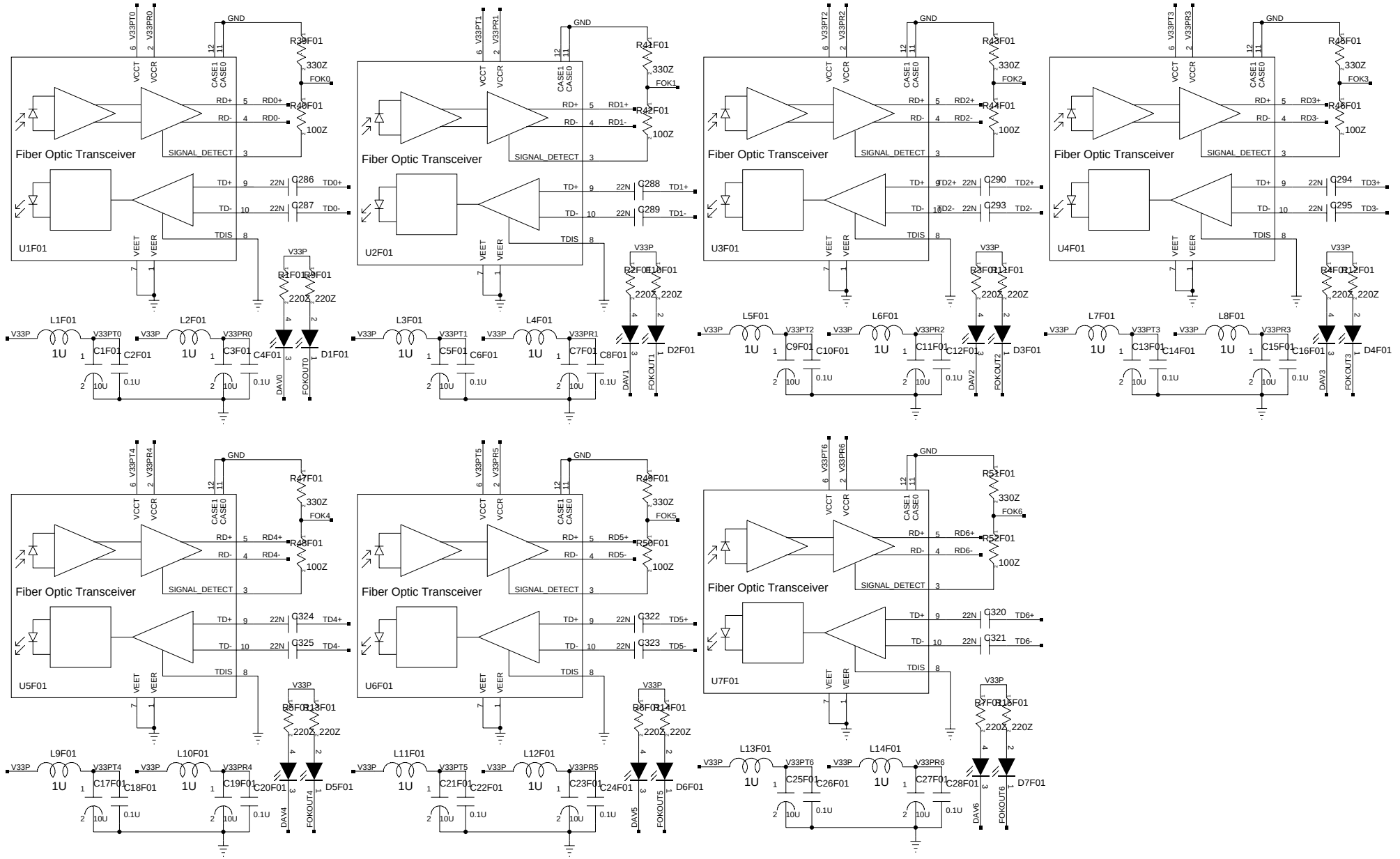
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_11:05	PARENT PAGE PROJECT: D785A FILE: INPUTF0 . 2 PAGE: 2A



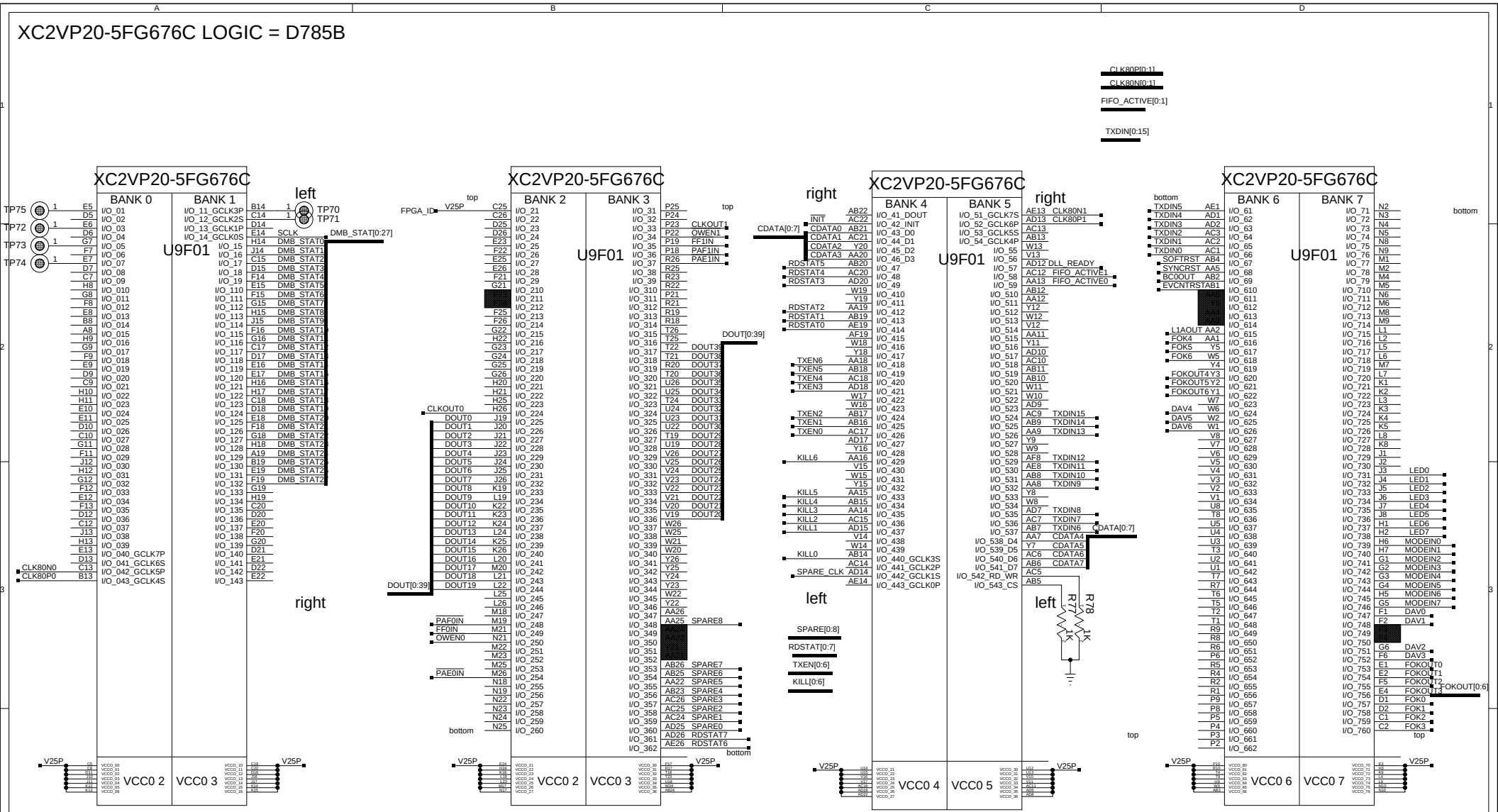
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_10:33	PARENT PAGE FILE: INPUTF0 . 3
		PROJECT: D785A	PAGE: 2A



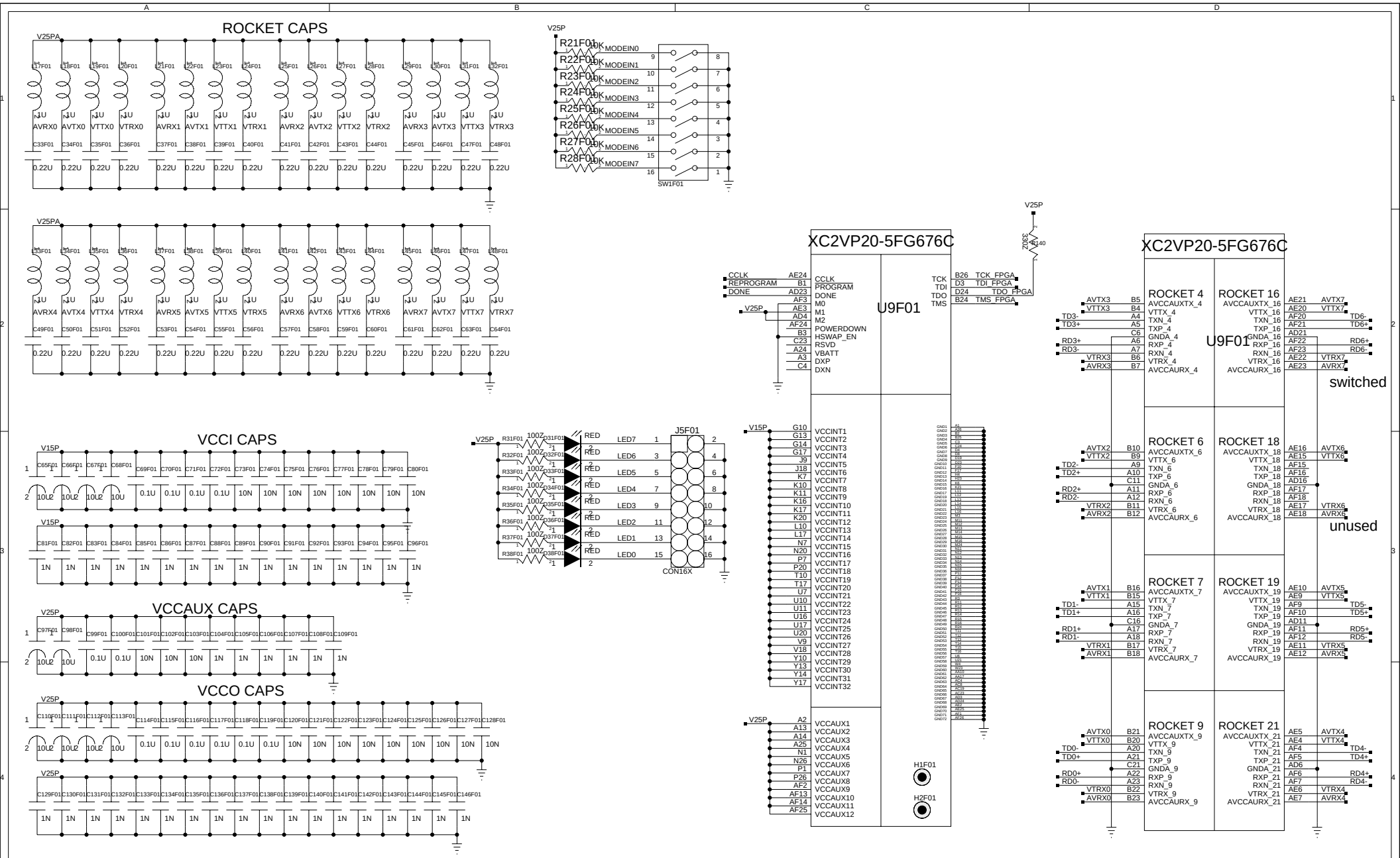
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_10:59	PARENT PAGE PROJECT: D785A FILE: INPUTF0 . 4 PAGE: 2A



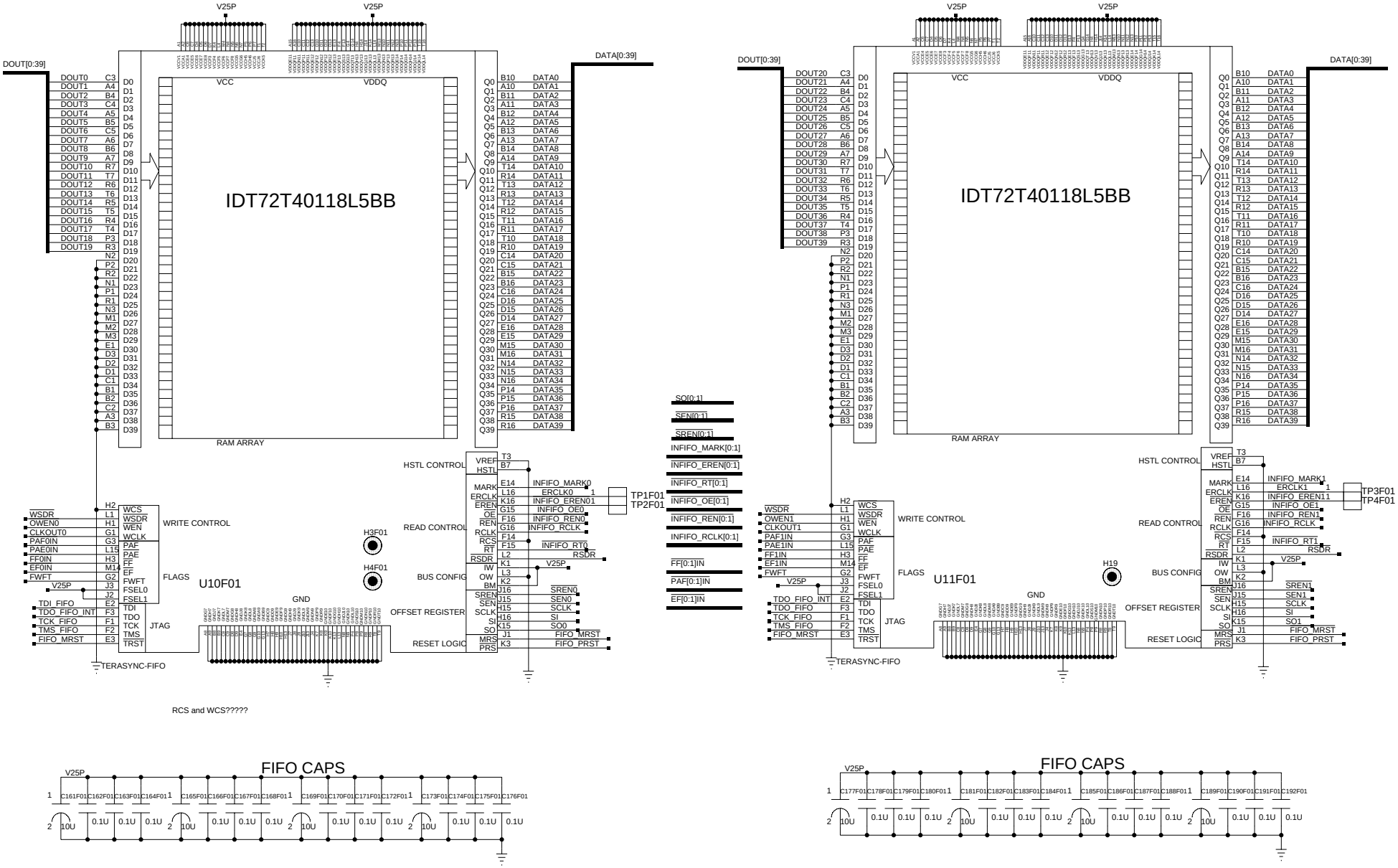
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH PARENT PAGE: DATE: 11-15-2004_10:53	PROJECT: D785A FILE: INPUTF01 . 1 PAGE: 2A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_11:05	PARENT PAGE PROJECT: D785A FILE: INPUTF01 . 2 PAGE: 2A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_10:33	PARENT PAGE FILE: INPUTF01 . 3
		PROJECT: D785A	PAGE: 2A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: OPTICAL TRANSCEIVERS AND ROCKET I/O FULL DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-15-2004_11:00	PARENT PAGE FILE: INPUTF01 . 4
		PROJECT: D785A	PAGE: 2A

For now TDO1 goes only to cable, but future version should feed TDO1 back into FPGA1

Test input BNCs are not needed in next version; use those 4 I/O (TBX0, TBXRST, TL1ACC, TL1ARST) for test points instead.

Add "DDU Control" box

RDSTAT[0:15]
TXDIN[0:15]
DLL_READY[0:2]
CTRL_STAT[0:3]
FIFO_ACTIVE[0:3]
SPARE[0:17]
SPARE_CLK[0:1]
VME[0:4]

TDI[6:8]
TMS[6:7]
TDO[6:8]
TCK[6:7]
FMM[0:3]
TXEN[0:14]
KILL[0:14]
BUS[0:8]
TDOUT[0:1]

PAF[0:3]IN
EF[0:3]IN
FF[0:3]IN
INFIFO_EREN[0:3]
INFIFO_REN[0:3]
INFIFO_OE[0:3]
INFIFO_MARK[0:3]
INFIFO_RT[0:3]

DATA[0:39]
OUTDATA[0:63]
BUS[0:9]
TDOUT[0:1]
USF[0:3]
LSF[0:3]
LRL[0:3]

XC2VP7-6FF672C
BANK 0 BANK 1
bottom
U35
top

XC2VP7-6FF672C
BANK 2 BANK 3
right
U35
left

XC2VP7-6FF672C
BANK 4 BANK 5
top
U35
bottom

XC2VP7-6FF672C
BANK 6 BANK 7
left
U35
right

VCC0 0 VCC0 1 VCC0 2 VCC0 3 VCC0 4 VCC0 5 VCC0 6 VCC0 7

DESKEW AFTER PROGRAMMING AND RESET?

pulldown's on jtag?

XC2VP7-6FF676C LOGIC = D785C

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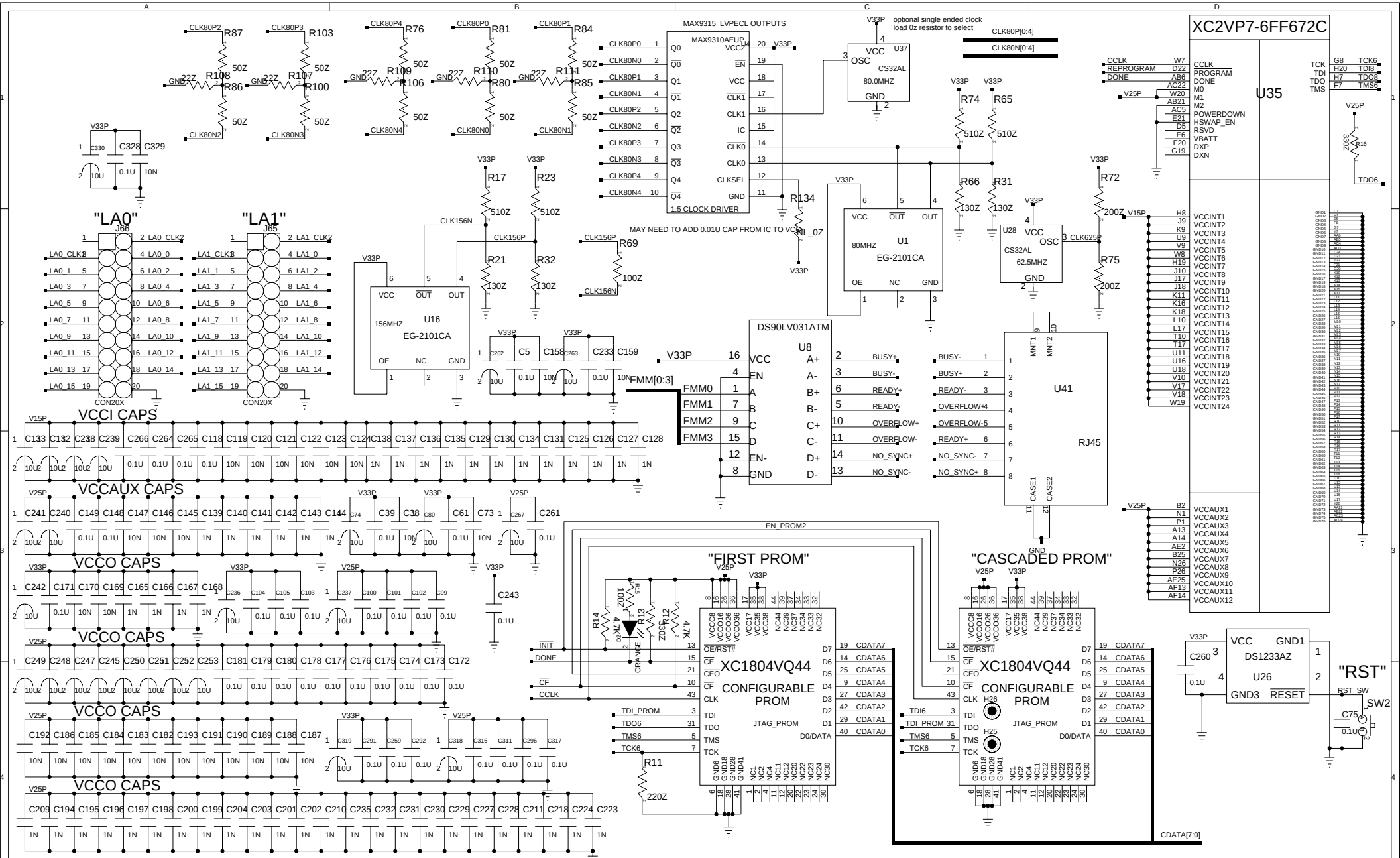
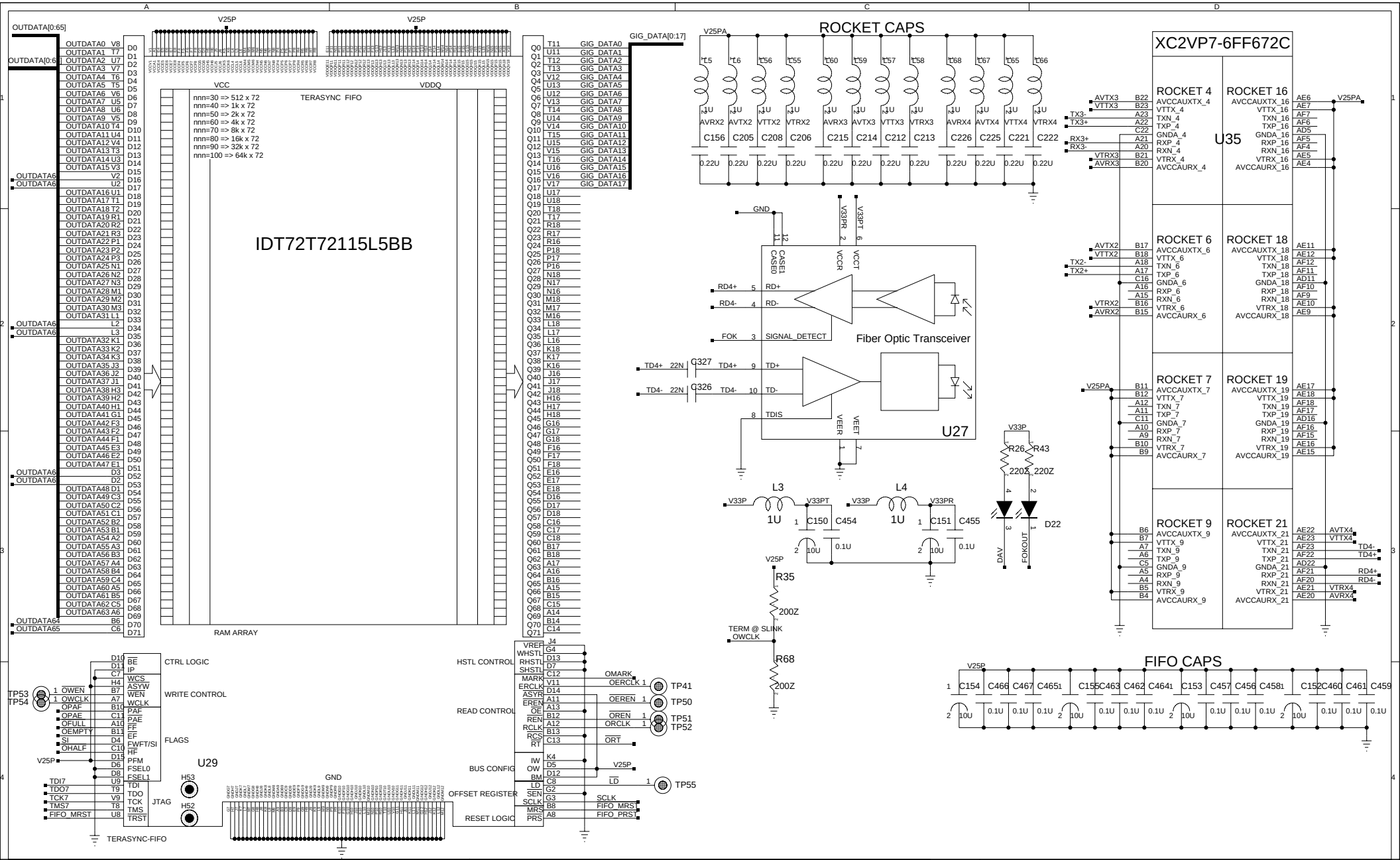
TITLE: OUTPUT CONTROL
Practice Full DDU
CMS CSC ELECTRONICS

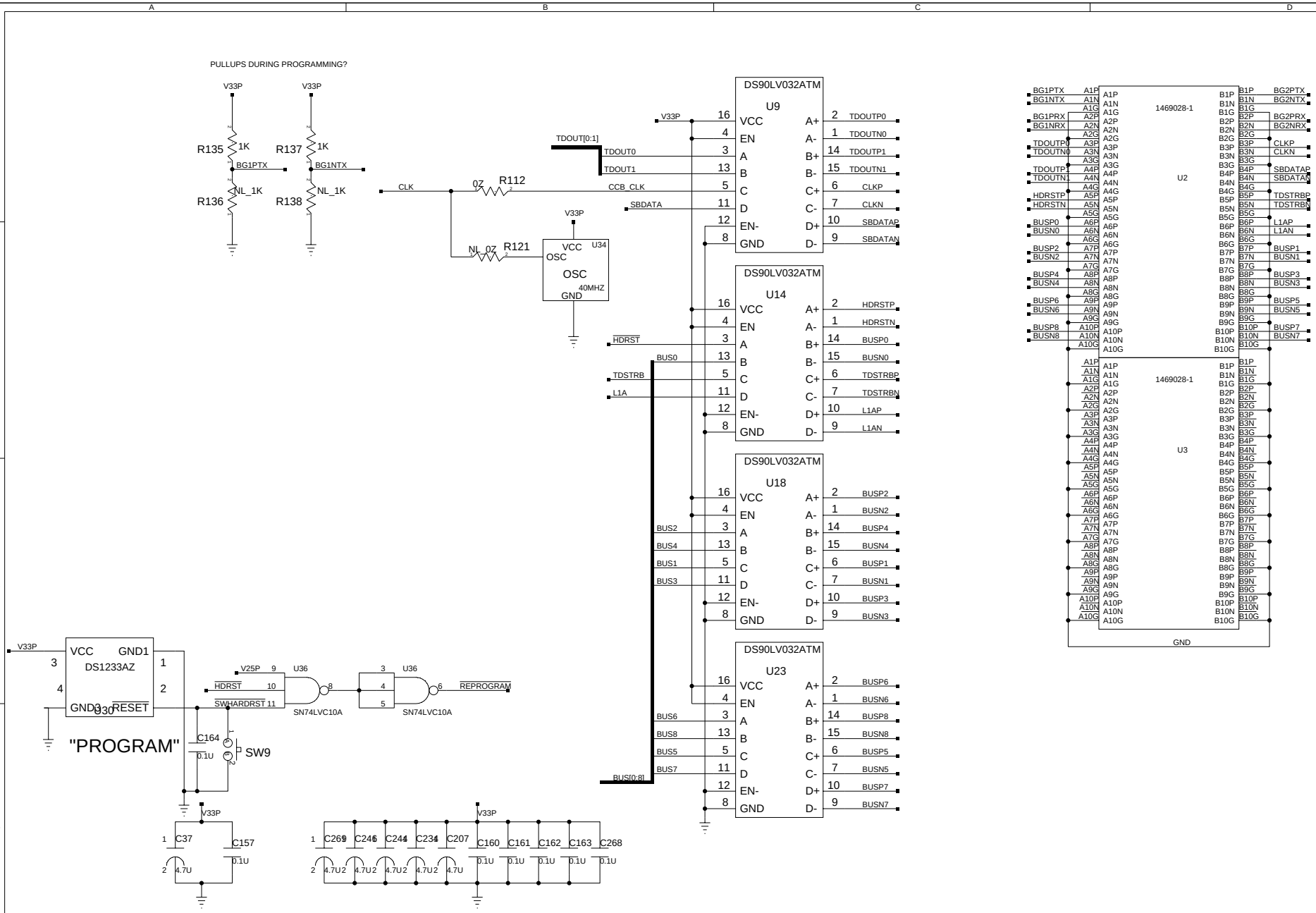
BY: moj
PARENT PAGE:
PROJECT: D752J
DATE: 11-19-2004_9:19
FILE: OUTCONTROL . 1
PAGE: 4A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE OUTPUT CONTROL Practice Full DDU CMS CSC ELECTRONICS	BY moj DATE 11-19-2004_9:19	PARENT PAGE PROJECT D752J FILE OUTCONTROL_2 PAGE 4B

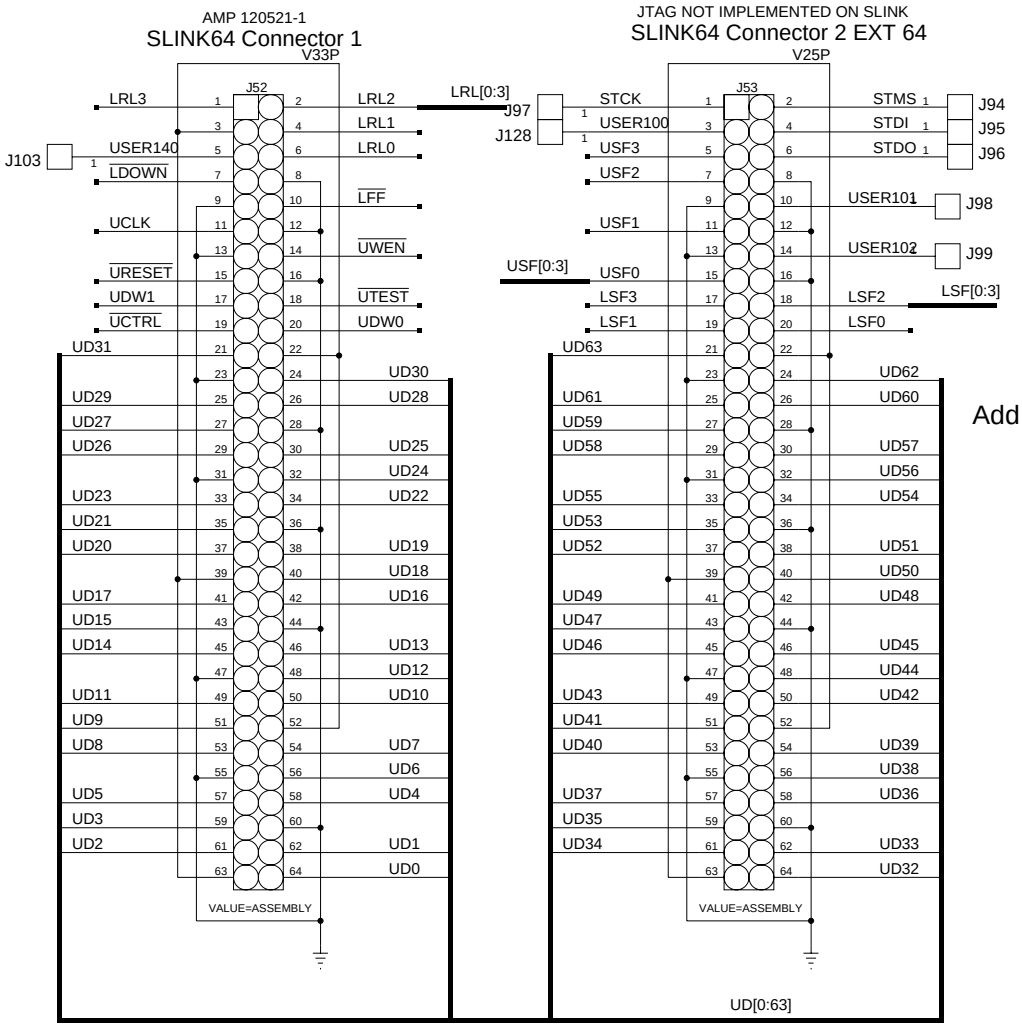


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE OUTPUT CONTROL Practice Full DDU CMS CSC ELECTRONICS	BY moj DATE 3-23-2004_9:32	PARENT PAGE PROJECT D752J FILE OUTCONTROL_3 PAGE 4B



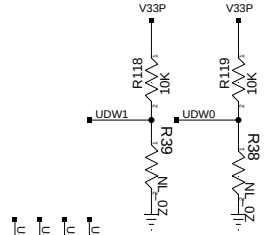
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CCB and External Test Connectors Practice Full DDU CMS CSC ELECTRONICS	BY: DCH	PARENT PAGE: 1	PROJECT: D752J
		DATE: 4-13-2004_16:14	FILE: CCB . 1	PAGE: 6

Implement basic S-LINK architechture on DDU board?



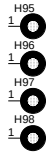
Not Used on Current LSC

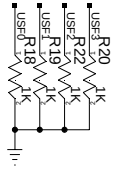
UDW[0:1] = 11 FOR 64 BIT TRANSFERS



SLINK64/LSC Standoff Holes

Isolated per SLINK Spec pg. 43/62





Voltage Keying Hole

USER140, USER101, USER102 NOT USED

USER100 IS FOR DESKEW OPTION, NEED TO DRIVE

Add accessible testpoints for UCLK, UWEN, UCTRL very near S-LINK port

fix 3.3v 2.5v on slink

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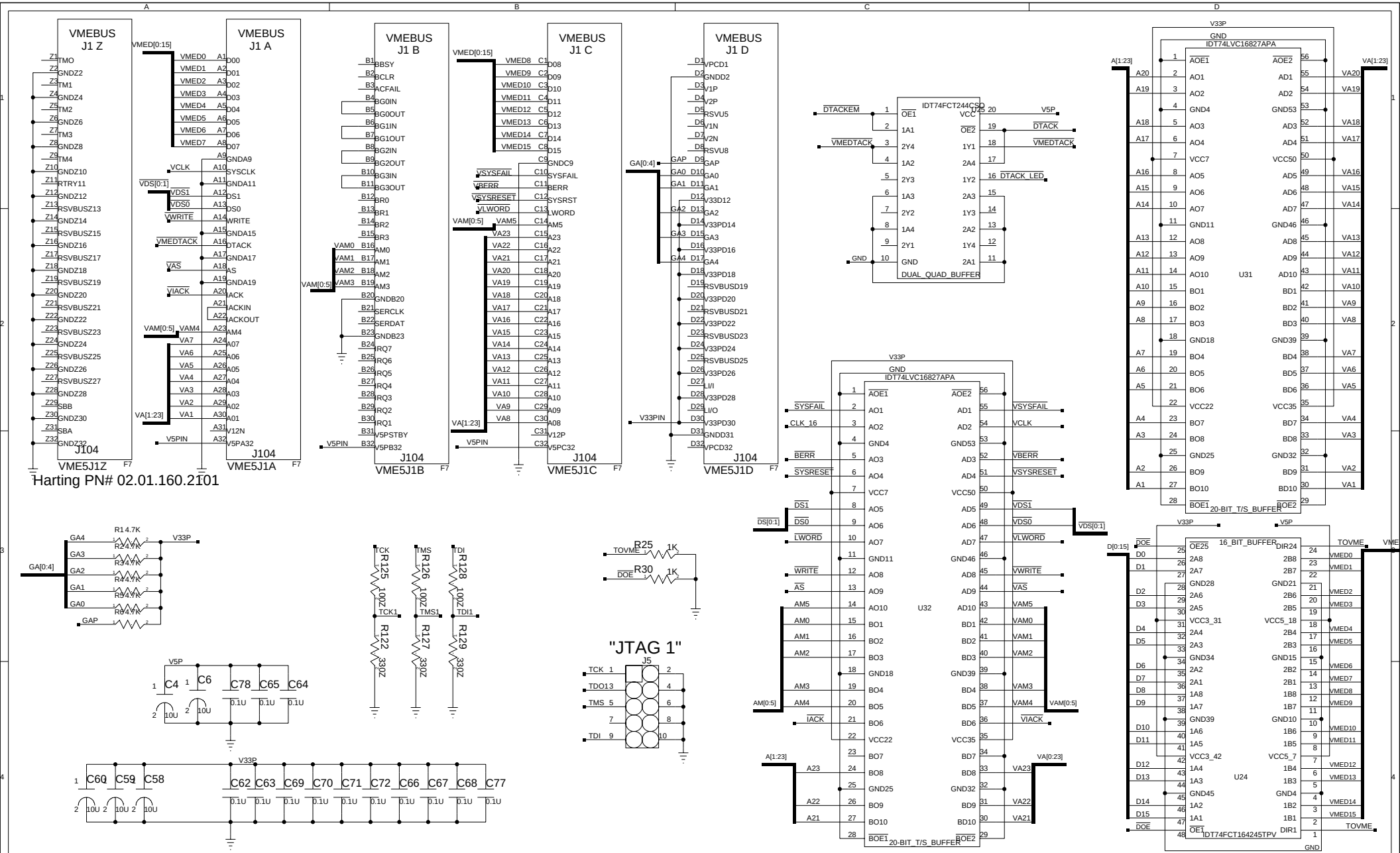
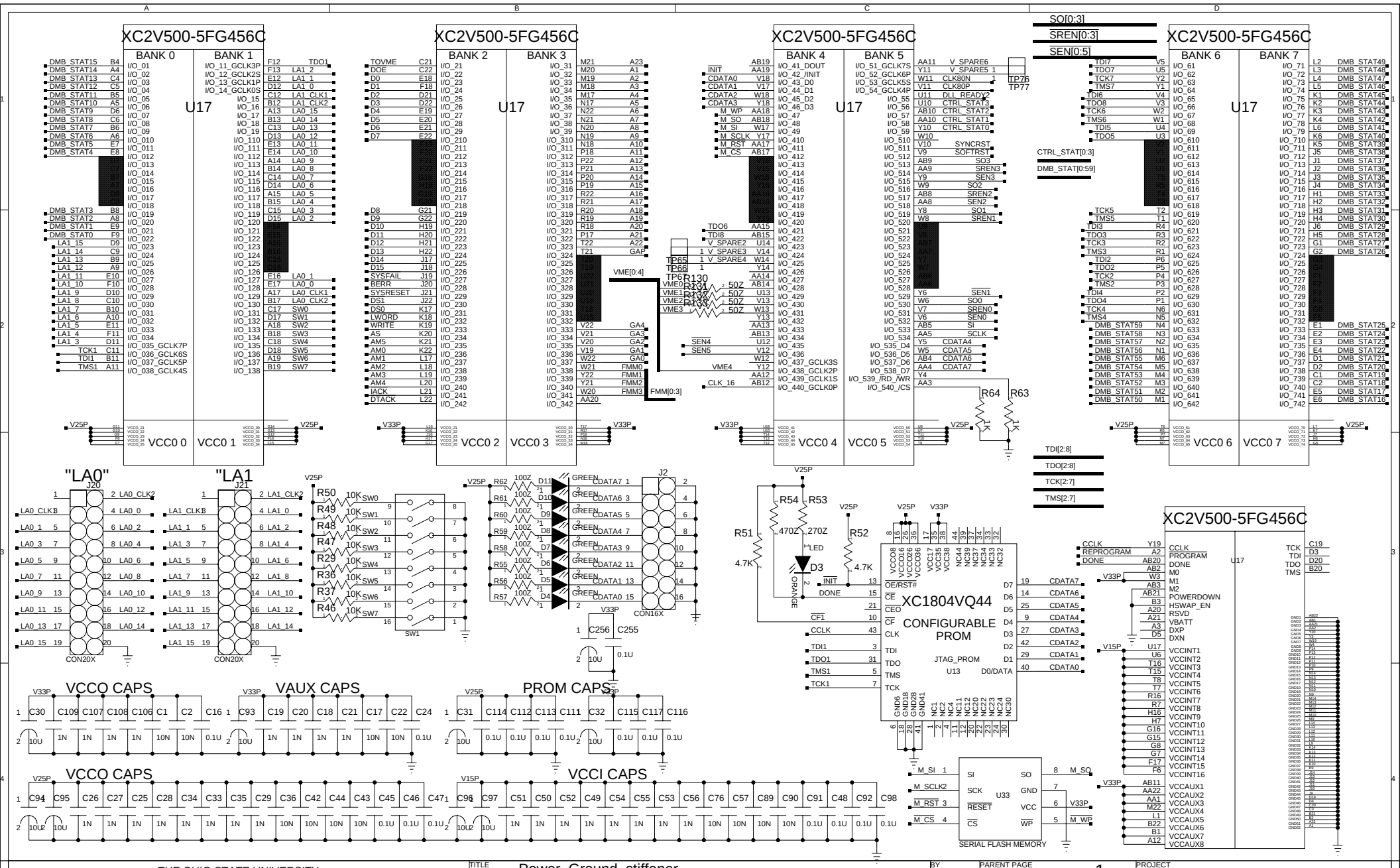
TITLE	SLINK INTERFACE Practice Full DDU CMS CSC Electronics		
BY dch	PARENT PAGE	PROJECT	D752J
DATE	1-13-2004_17:20	FILE	SLINK . 1
		PAGE	7

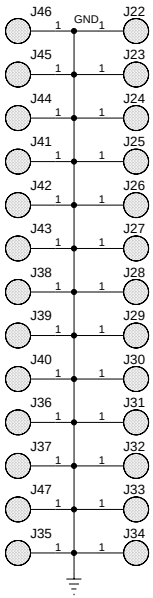

VMEBUS J1 Z
VMEBUS J1 A
VMEBUS J1 B
VMEBUS J1 C
VMEBUS J1 D
J104
VME5J1Z
VME5J1A
VME5J1B
VME5J1C
VME5J1D
Harting PN# 02.01.160.2101
IDT74FCT244CSO
DUAL_QUAD_BUFFER
IDT74LVC16827APA
20-BIT_T/S_BUFFER
IDT74FCT164245TPV
16_BIT_BUFFER
"JTAG 1"
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
VMEbus P1, transceivers & Power Supply
Practice Full DDU
CMS CSC Electronics
DCH/GU
11-15-2004_10:16
D752J
VME . 1
5A

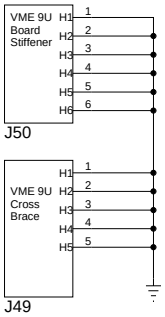
XC2V500-5FG6456C LOGIC = D785D



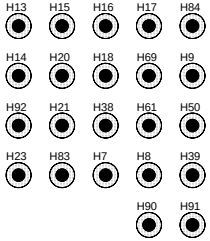
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Power, Ground, stiffener Practice Full DDU CMS CSC ELECTRONICS	BY: DCH DATE: 11-19-2004_10:07	PARENT PAGE: 1 FILE: VME. 2	PROJECT: D752J PAGE: 5B

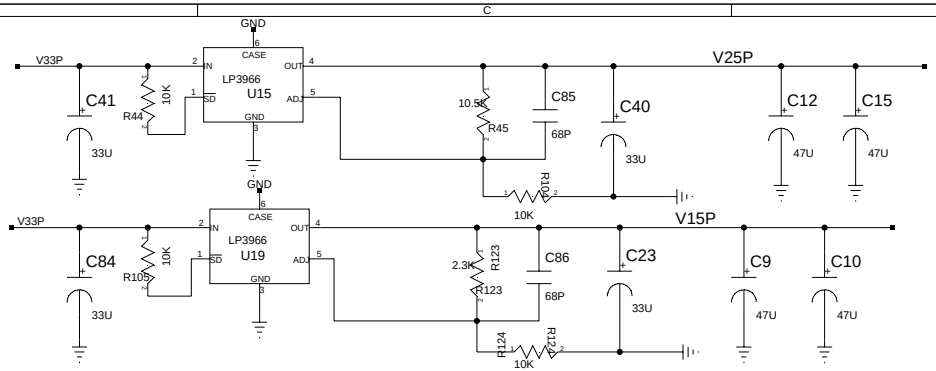
GROUND POINTS BOARD STIFFENER



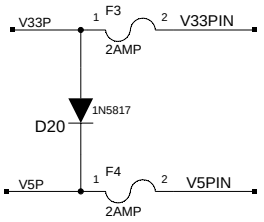


PART FIDUCIALS

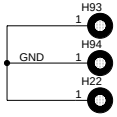




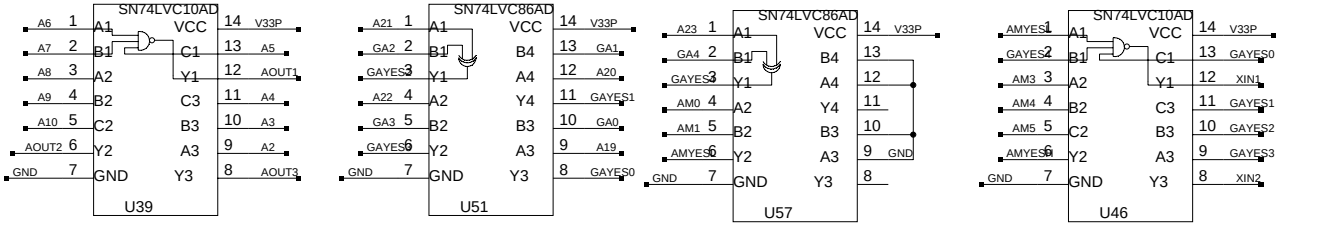
INPUT POWER

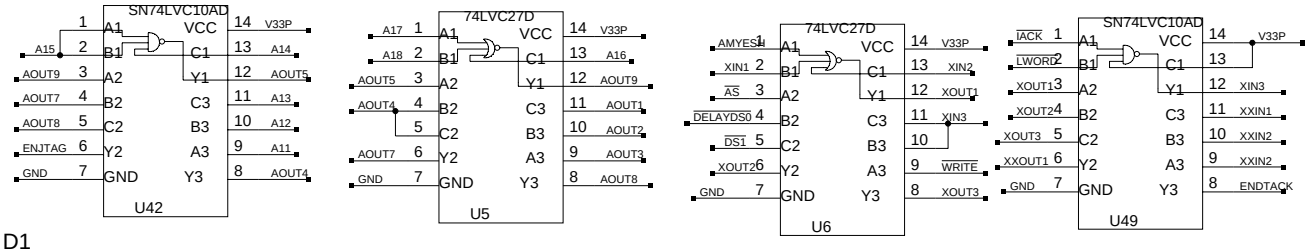


FRONT PANEL MOUNTS

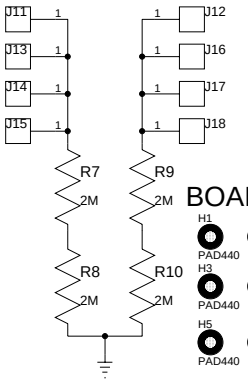


Discrete logic to load the VPROM in emergency

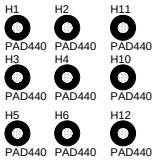




DISCHARGE UNIT



BOARD STANDOFFS



D1