this DDU:
add _BX Offset_ to Flash SRAM

VME5CTRL (file 0ddu_vme5) BF014A04 Version 14

10-5-2005_15:29

CMS CSC DDU5, VME FPGA

v1: Begin vme5ctrl from vme4ctrl v5, new DDU5 pinout
v3-8: All PROM JTAG lines now have 3-state drivers, fixed UCF FMM pins
v9-10: Add VME Serial ADC control (Device 8...13 in r2), debug on LEDmode14; tune DLLs
v11-13: Modify FMM LEDs, add 3 IRQ pins, add VME Registers for GbE/SLINK_WAIT, Fake_L1A_Enable & DDU production testing
v14: Add Restore-Idle after SoftReset, add Busy/Warn history on VMEparDev6/5, tune RealFMM logic
v14r2-4: Tune Busy/Warn history

Set all Banks to 3.3V I/O

Indep Clocks: clk80, sclk
Dependent Clocks: ck40=clk

VMECNTRL

PART=XC2V500-5-FG456
PROM=XC18V04-VQ44 (PARALLEL)

ddu5_vme\VME5Ctrl\vme5ctrl

PromID: 05036093h

Mode 1 Switch Block, reversed labels on board
1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4 } 00 for Standard Debug, 01 for VME-Serial
6: Mode Bit 5 } 10 for Flash RAM, 11 for VME-Parallel
7: Disable Auto Serial Load
8: Set all LA bits HIGH, ~FPGA version on LEDs
RST_1=Soft_Reset for FPGAs and ALL FIFOs

VME Broadcast Addresses:
24=OSU-TCB "Test Control Board"
25=DMB
26=TMB
27=Both DMB and TMB
28=DDU
29=DCC

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Replace EmptyIN/FIFO_EMPTY PUs?

To Do:
- Test VME_IRQ pin functions
- Check GbE-thresh Autoload
- Put GbE Prescale into Flash RAM
- Connect and drive FMM signals
  ---> Set correct default state on board!
- No logic for VMECLK, VMEA1...OK.

DDU Format Since DDUctrl v15:

BOE1 type L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK

49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH

LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

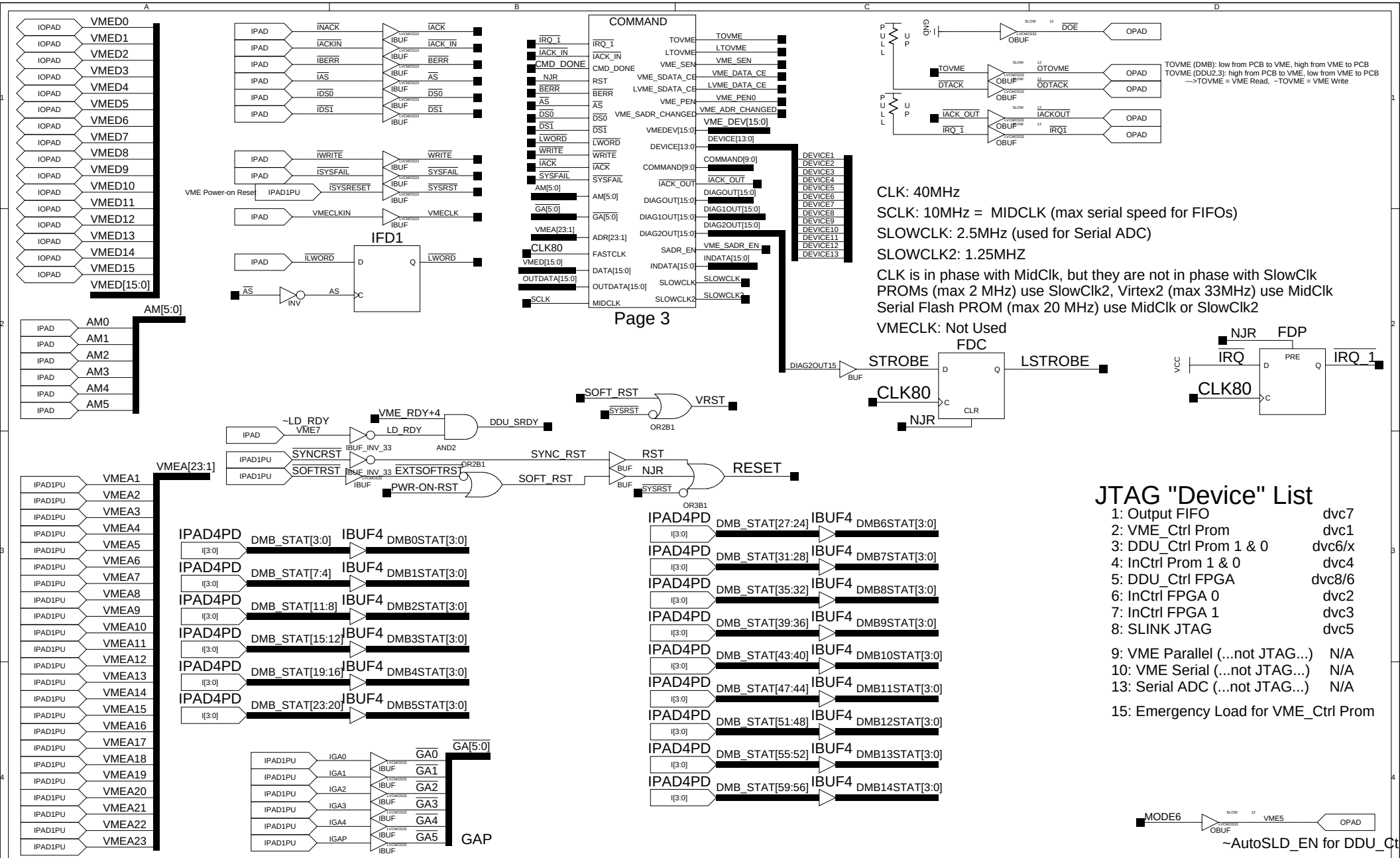
64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000

DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP

EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0x19A = 410 dec.
DDU WC, 1 DMB with 2 CFEB: 0x32A = 810 dec.
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 0x32E = 814 dec.
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 0x64E = 1614 dec.
DDU_WordCount = (6 + 25*Nts*nCFEB + 3*nDMB) <= 30050 (ignoring Trigger boards)
Ethernet_ByteCount = 8*DDU_WordCount 16 TS assumed

mojo



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TITLE: VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	1	D785
DATE	FILE	PAGE
10-5-2005_15:27	VMECNTRL . 1	2A

DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK

The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz

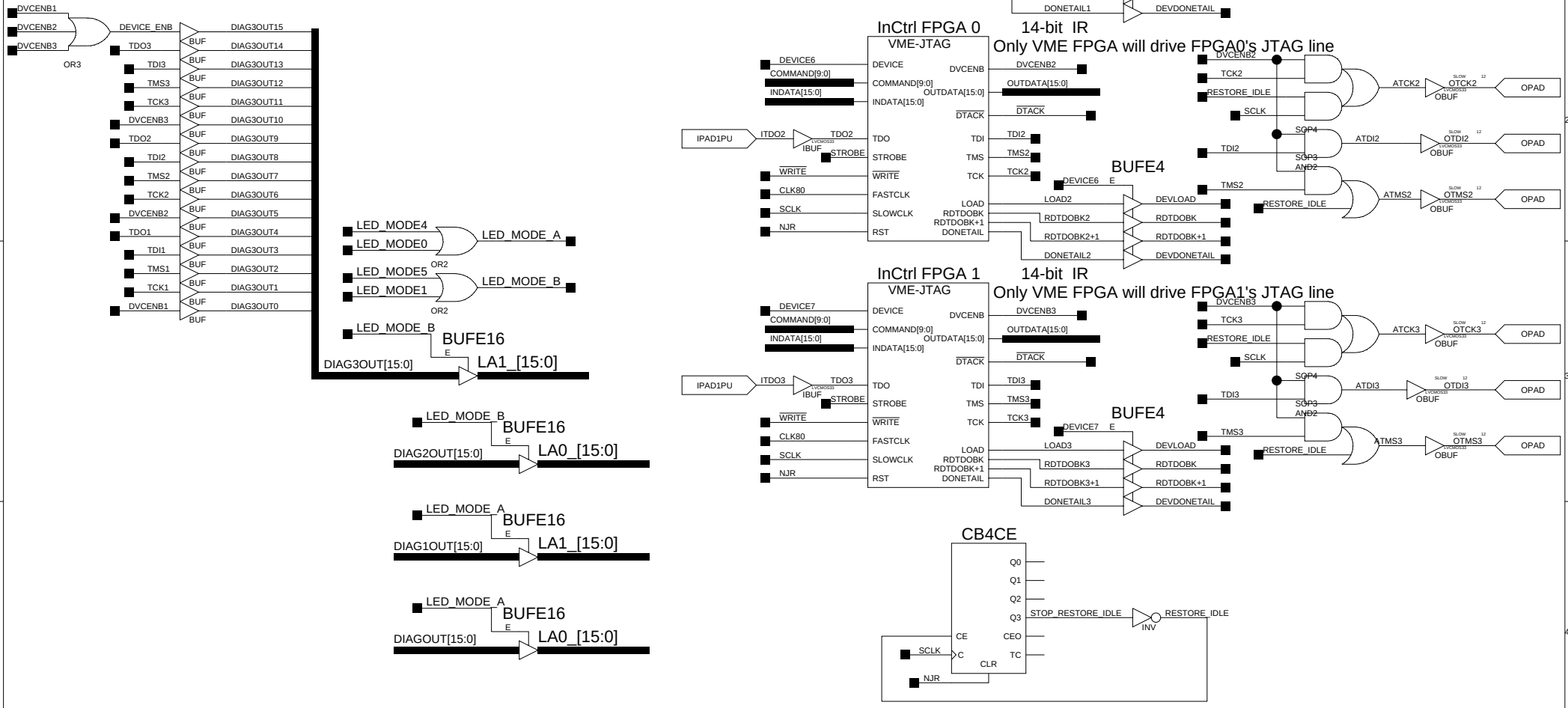
The ISP does not work at 2.5MHz or faster

Free LED_Modes

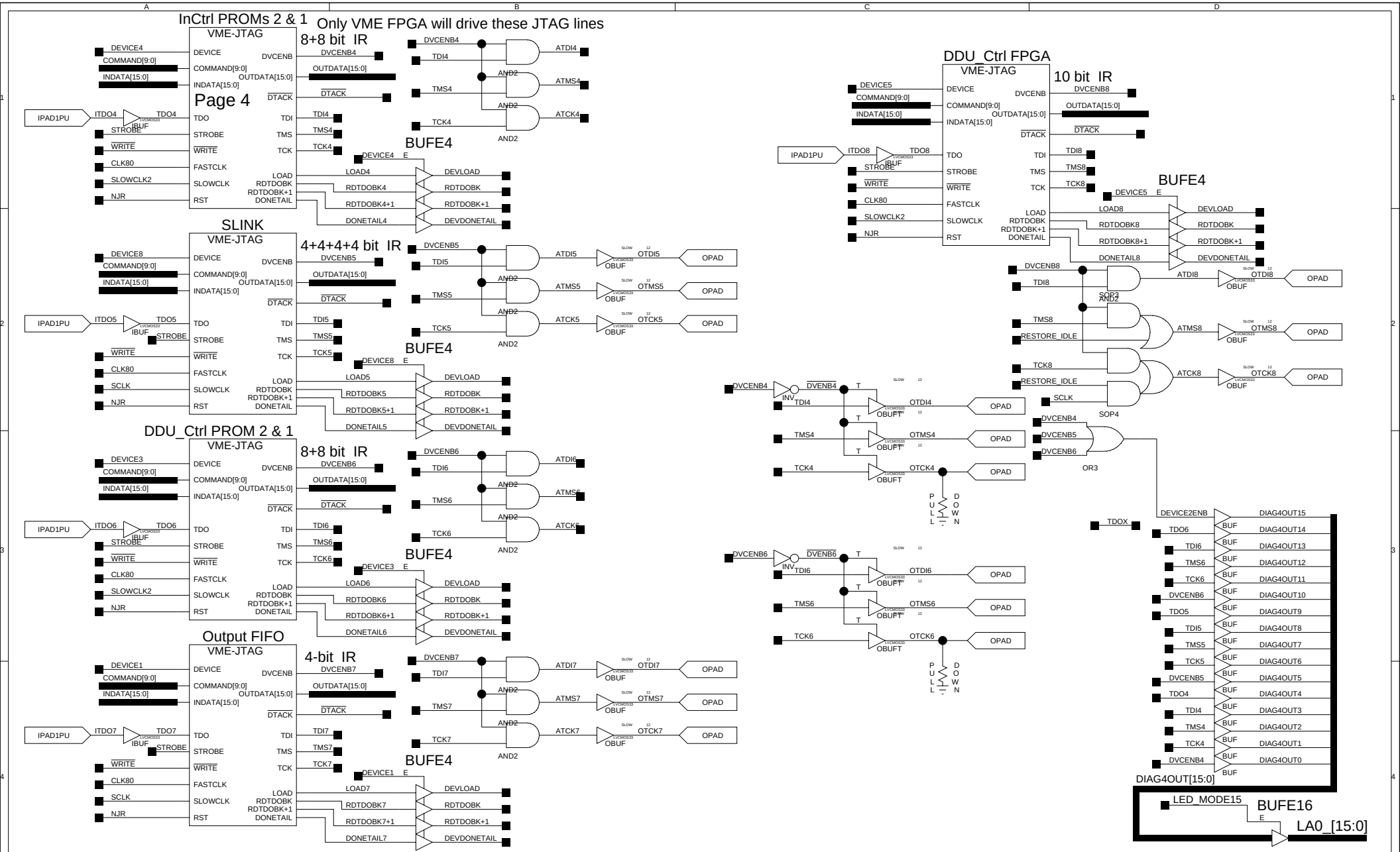
LA free: 12,13

LEDs Free: 12,13

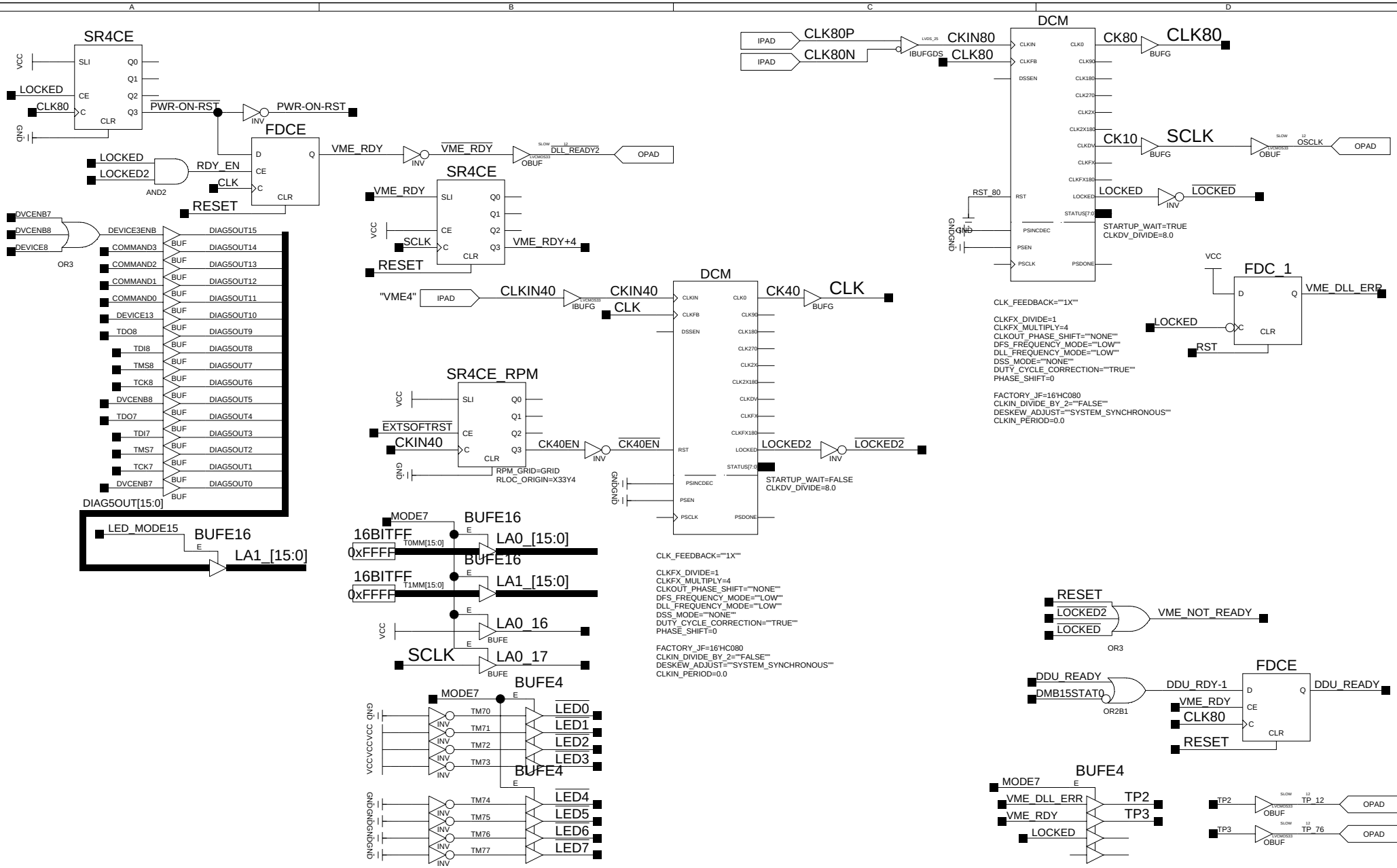
TP 2-4 Used: 0,1



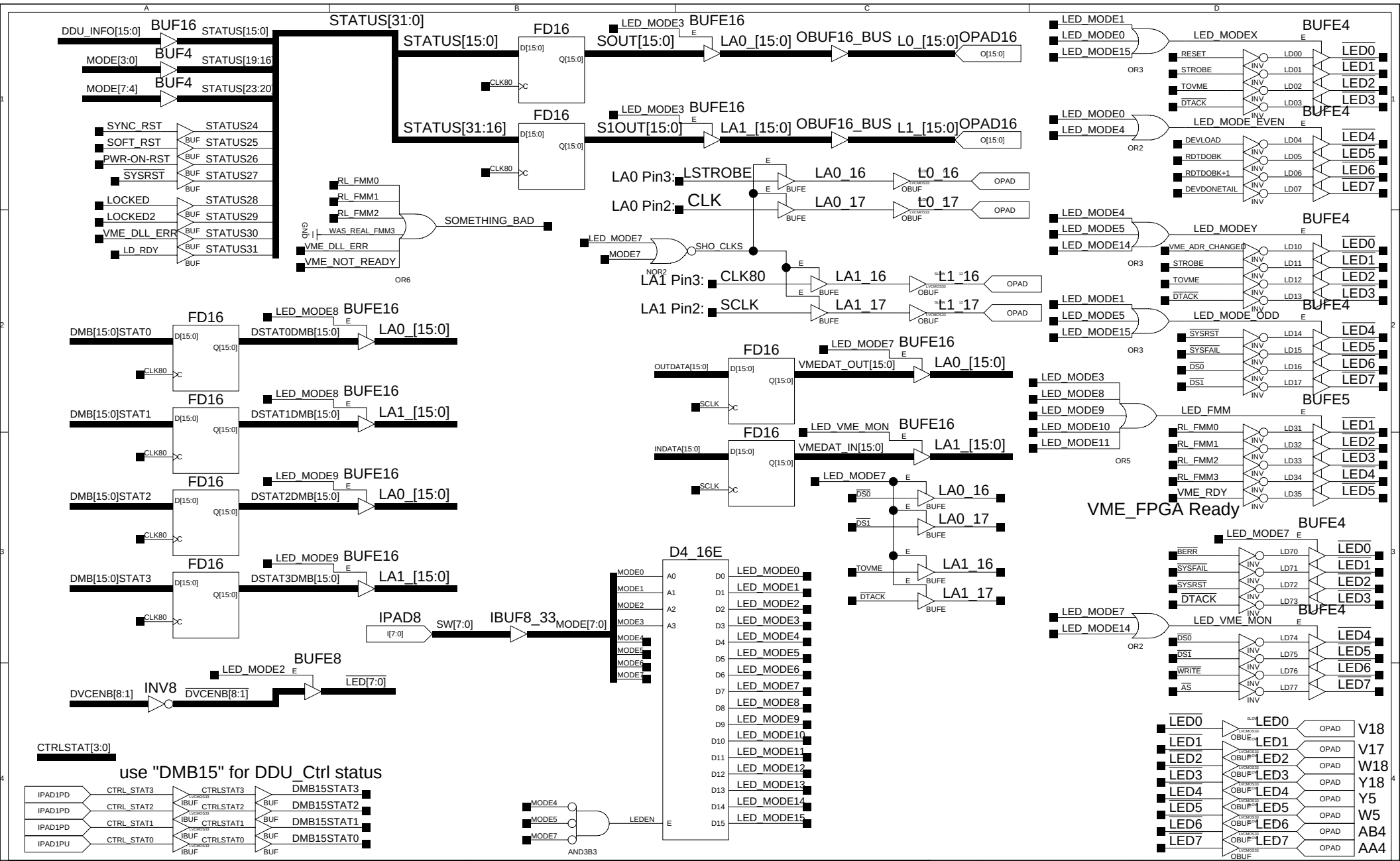
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 1	PROJECT D785
			DATE 9-1-2005_11:25	FILE VMECNTRL . 2	PAGE 2B



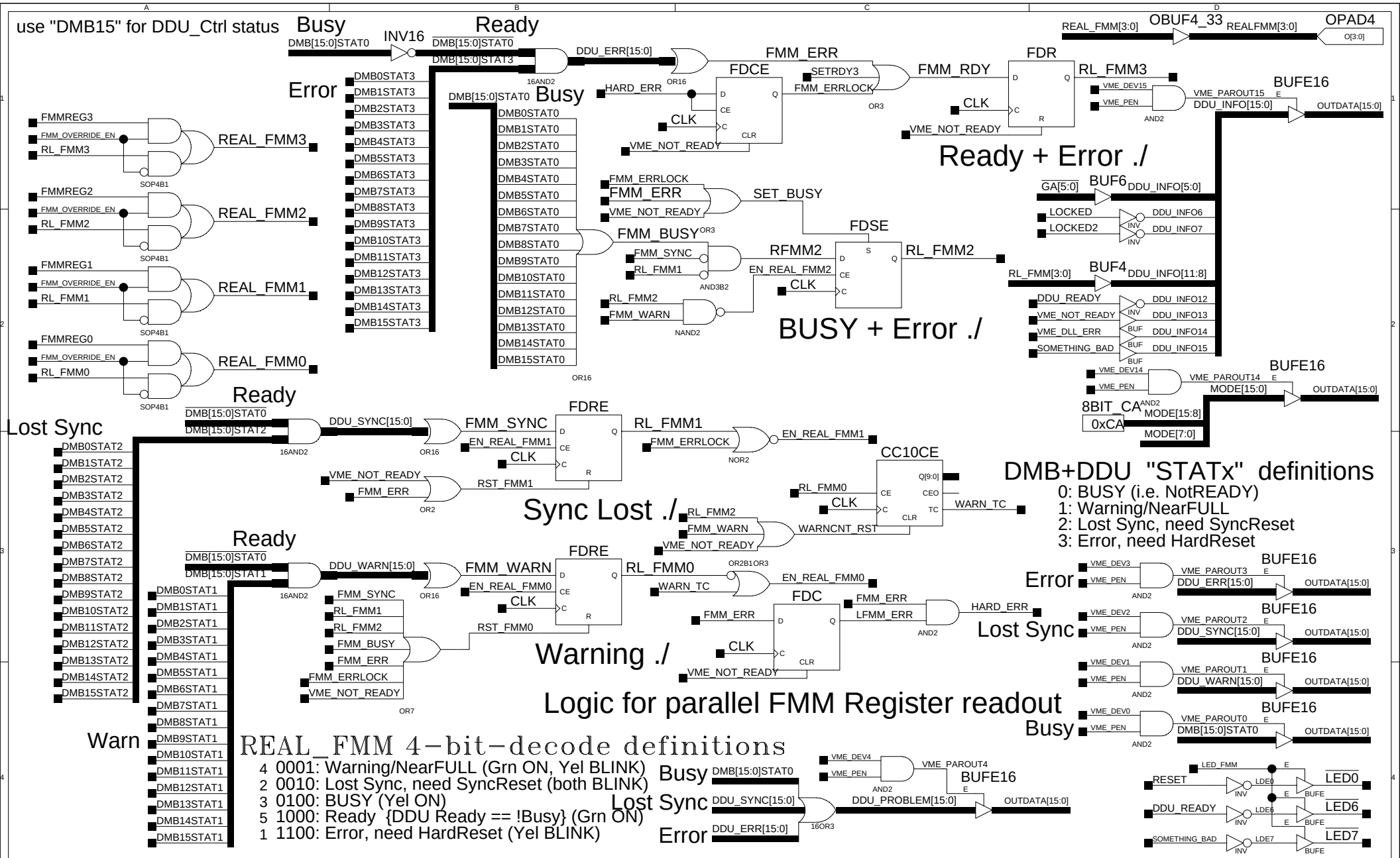
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-1-2005_11:28	PARENT PAGE: 1 FILE: VMECNTRL . 3
		PROJECT: D785	PAGE: 2C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-2-2005_14:15	PARENT PAGE: 1 FILE: VMECNTRL . 4
		PROJECT: D785	PAGE: 2D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-2-2005_14:15	PARENT PAGE: 1 PROJECT: D785 FILE: VMECNTRL . 5 PAGE: 2E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785
		DATE: 10-5-2005_15:26	FILE: VMECNTRL . 6	PAGE: 2F

Serial Device List (12 device functions, SEN = Serial Load)

0x 00: Read InFIFO 0
01: Read InFIFO 1
02: Read InFIFO 2
03: Read InFIFO 3
04: R/W Flash SRAM

Non-VME!! Auto Load Only

0x 08: W Load DDR InFIFO 0
09: W Load DDR InFIFO 1
0A: W Load DDR InFIFO 2
0B: W Load DDR InFIFO 3

VME_SDEV>=8 or ==4 are Writeable; others are Read Only.

0C: W Load GBE Output FIFO (SEN=LD, set HI during MRST) --test?
0D: W Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.) --test?
0E: W Load DDU_Ctrl FPGA (Board ID) --test?
0F: W Load all 4 DDR InFIFOs

9 VME Reads, 4 VME Writes, 7 Auto commands

Flash <--> Serial
Auto Load After MRST

VME <--> Serial-Rd Only, No Flash SRAM (dev,FMpage=VMEcmd)

vmedev 00 --ToVME=1
01 --ToVME=1
02 --ToVME=1
03 --ToVME=1

SLDcmd 02: (all 4 in parallel) 08,04 09,04 0A,04 0B,04 DDR

SLDcmd 03: 0C,05 GbE

SLDcmd 00: 0D,01 (on DDU_Ctrl request) Kill-Ch

SLDcmd 01: 0E,07 (after 0D,01) Board-ID

VME <--> Flash SRAM, No Serial Dev

vmedev04/cmd 00 --ToVME=1
09 --ToVME=0
0C --ToVME=0
0D --ToVME=0
0F --ToVME=0

Flash Memory Access (9 VME-Serial commands on Dev4)

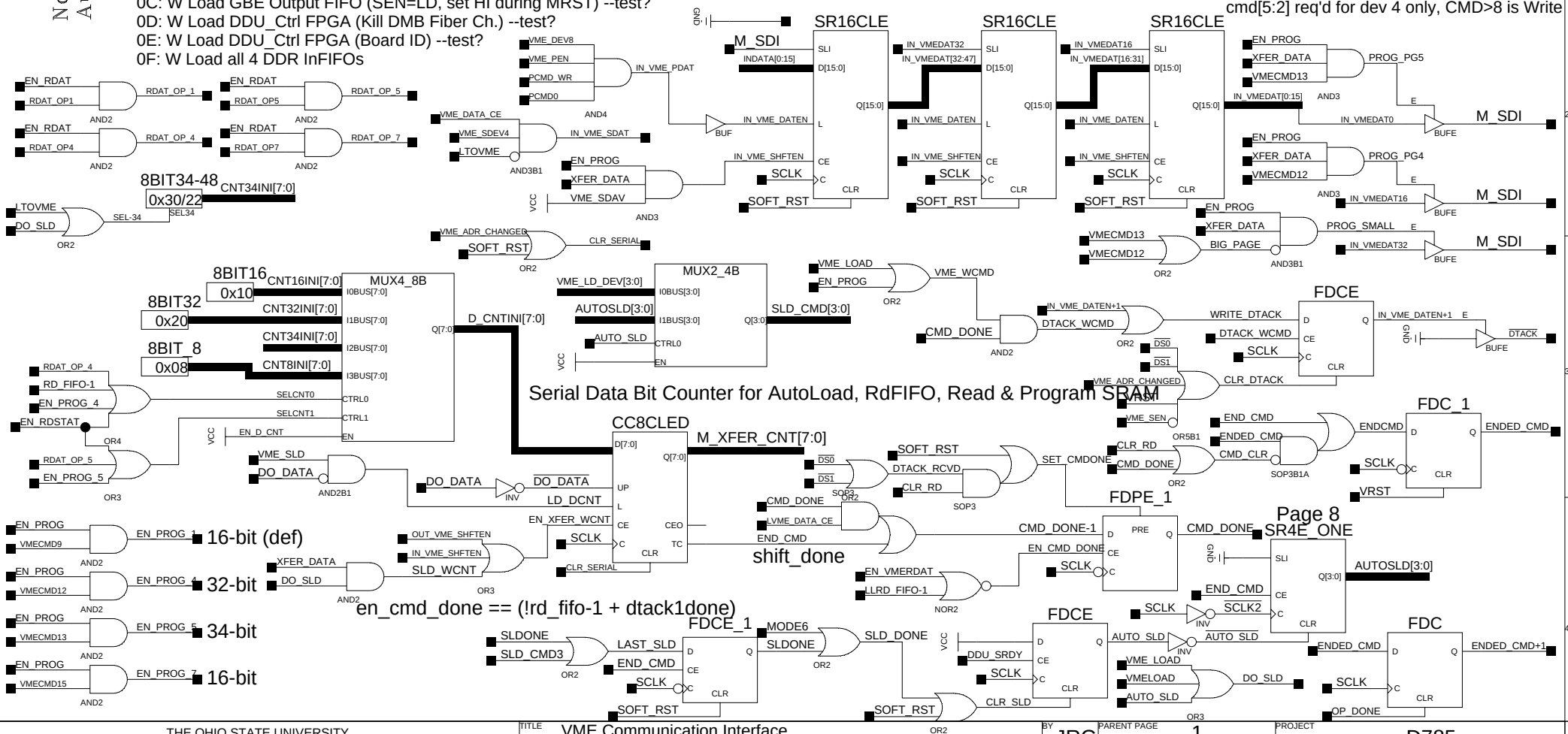
CMD<9 is Read Only. CMD>=9 is Write Only.

0x 00: Read Status Register
01: Read page 1 (Kill Ch.) to DDU_Ctrl
04: Read page 4 (DDR offsets) to In DDR FIFO
05: Read page 5 (GBE offsets) to GBE Out FIFO
07: Read page 7 (Board ID) to DDU_Ctrl

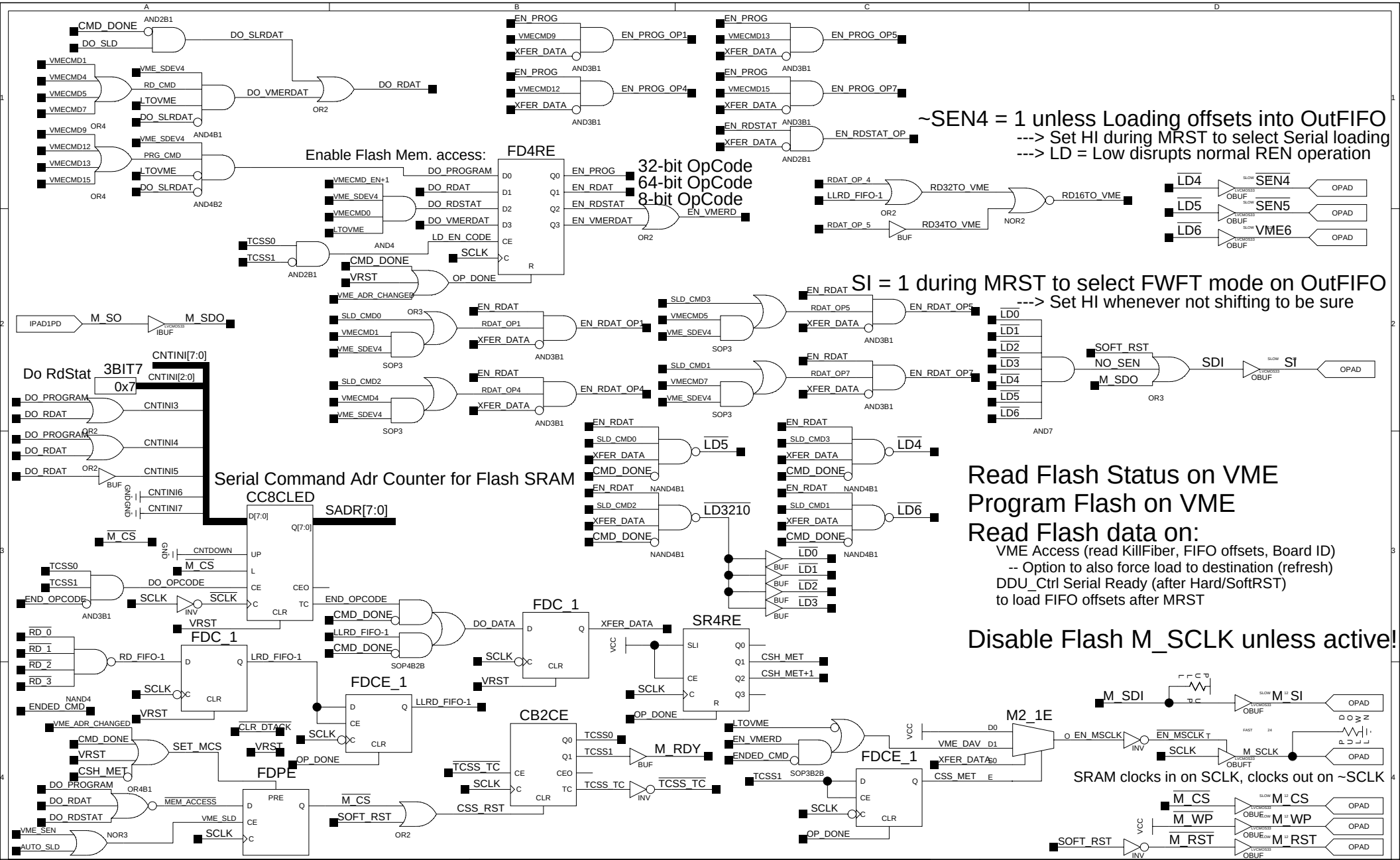
0x 09: W Program page 1 (Kill Ch.) [16 bit data]
0C: W Program page 4 (DDR offsets) [32 bit data]
0D: W Program page 5 (GBE offsets) [34 bit data]
0F: W Program page 7 (Board ID) [16 bit data]

Serial VME_ADR: slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]

cmd[5:2] req'd for dev 4 only, CMD>8 is Write

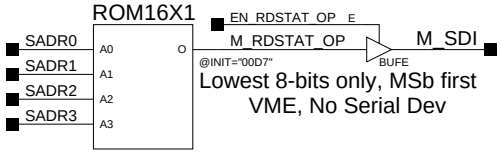


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_17:22	PARENT PAGE: 1 FILE: VMECNTRL . 7	PROJECT: D785 PAGE: 2G

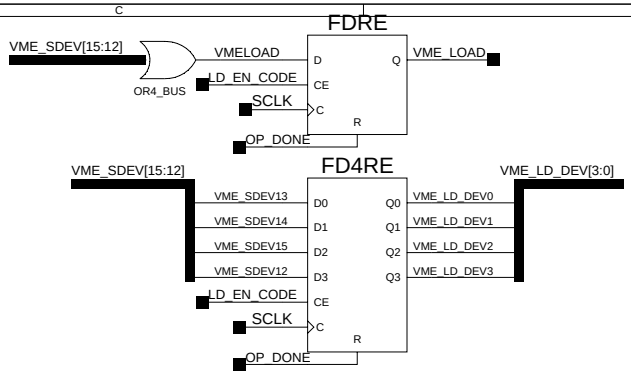


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 6-29-2005_16:47	PARENT PAGE: 1 FILE: VMECNTRL . 8
		PROJECT: D785 PAGE: 2H	

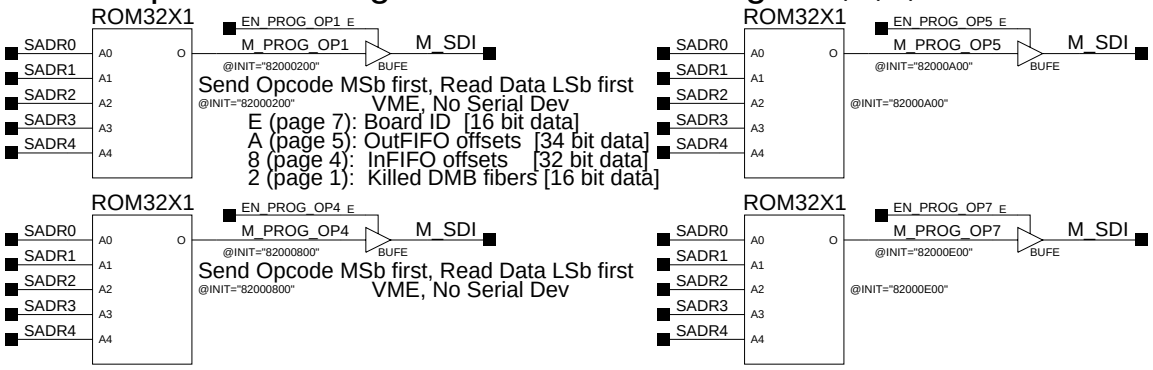
8-bit Opcode: Read Flash SRAM Status



Lowest 8-bits only, MSb first
VME, No Serial Dev

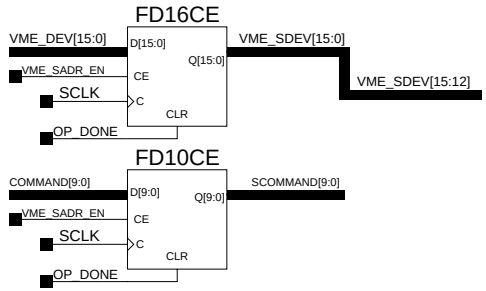


32-bit Opcodes: Program Flash SRAM Pages 1,4,5,7

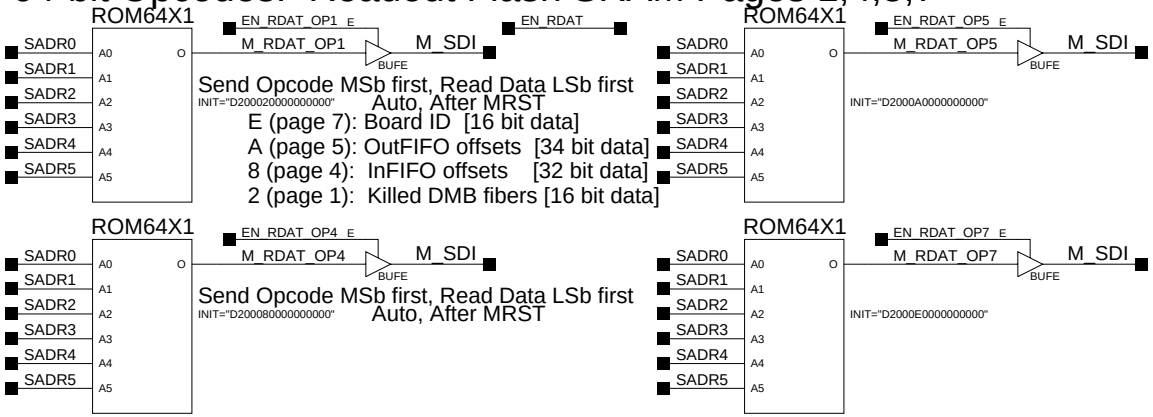


Send Opcode MSb first, Read Data LSb first
@INIT="82000200" VME, No Serial Dev
E (page 7): Board ID [16 bit data]
A (page 5): OutFIFO offsets [34 bit data]
8 (page 4): InFIFO offsets [32 bit data]
2 (page 1): Killed DMB fibers [16 bit data]

Send Opcode MSb first, Read Data LSb first
@INIT="82000800" VME, No Serial Dev



64-bit Opcodes: Readout Flash SRAM Pages 1,4,5,7



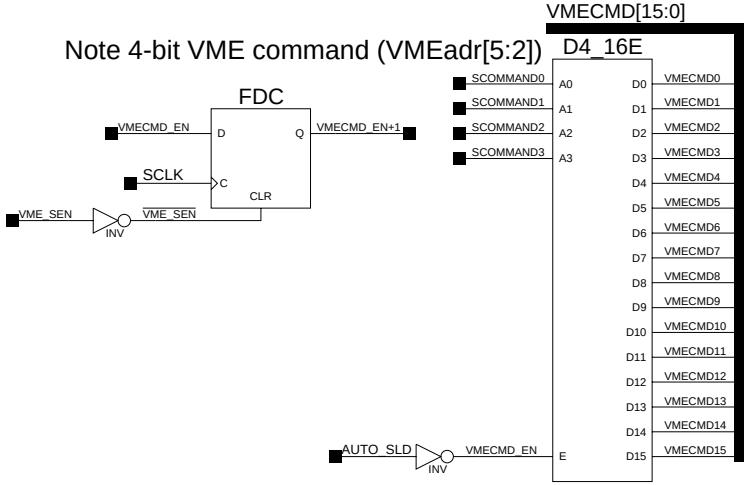
Send Opcode MSb first, Read Data LSb first
INIT="D200020000000000" Auto, After MRST
E (page 7): Board ID [16 bit data]
A (page 5): OutFIFO offsets [34 bit data]
8 (page 4): InFIFO offsets [32 bit data]
2 (page 1): Killed DMB fibers [16 bit data]

Send Opcode MSb first, Read Data LSb first
INIT="D200080000000000" Auto, After MRST

INIT="D2000A0000000000"

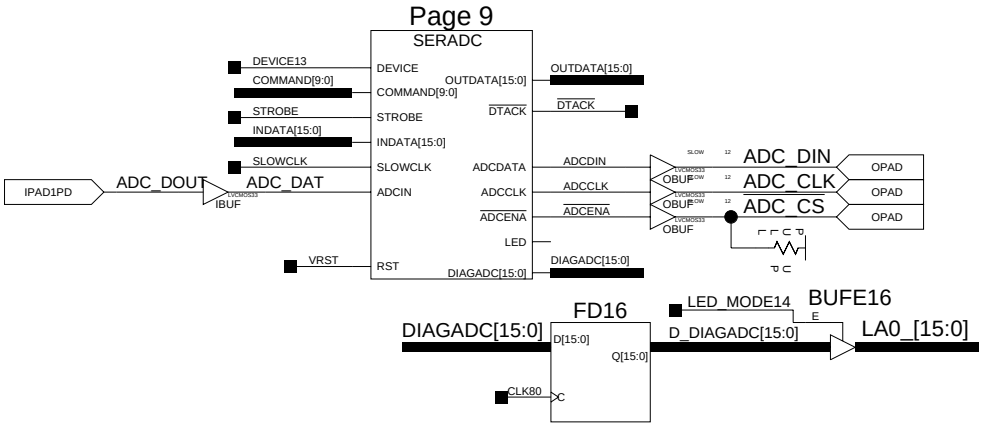
INIT="D2000E0000000000"

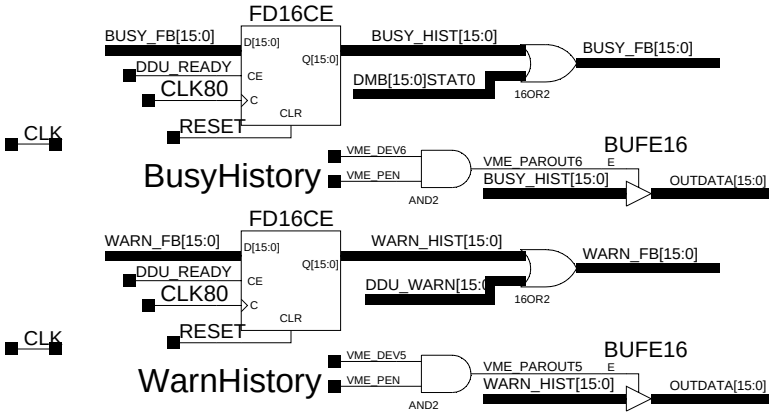
Note 4-bit VME command (VMEadr[5:2])



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785
		DATE: 1-4-2005_17:12	FILE: VMECNTRL . 9	PAGE: 2I

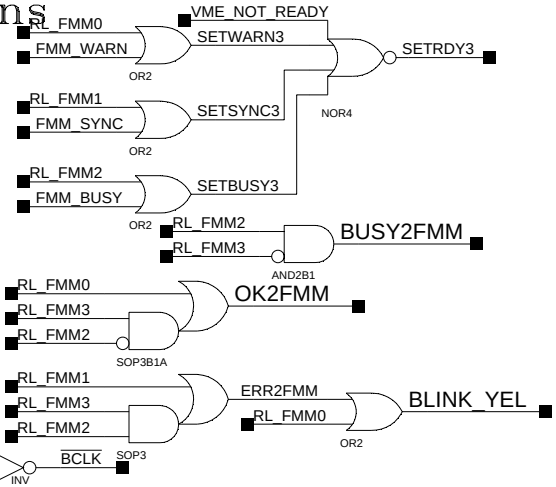
Serial ADC (MAX1270/1271) Interface clock: 1.25MHz (Divided SLOWCLOCK) is used
The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz

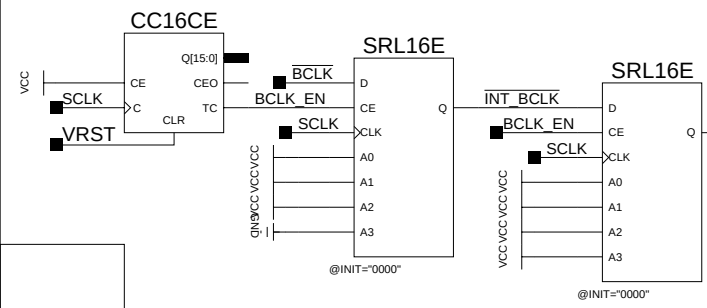


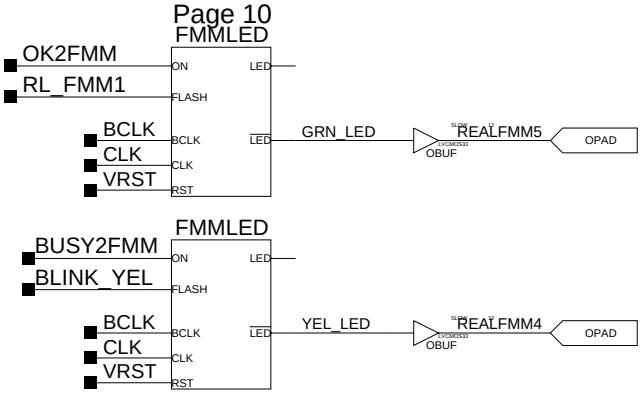


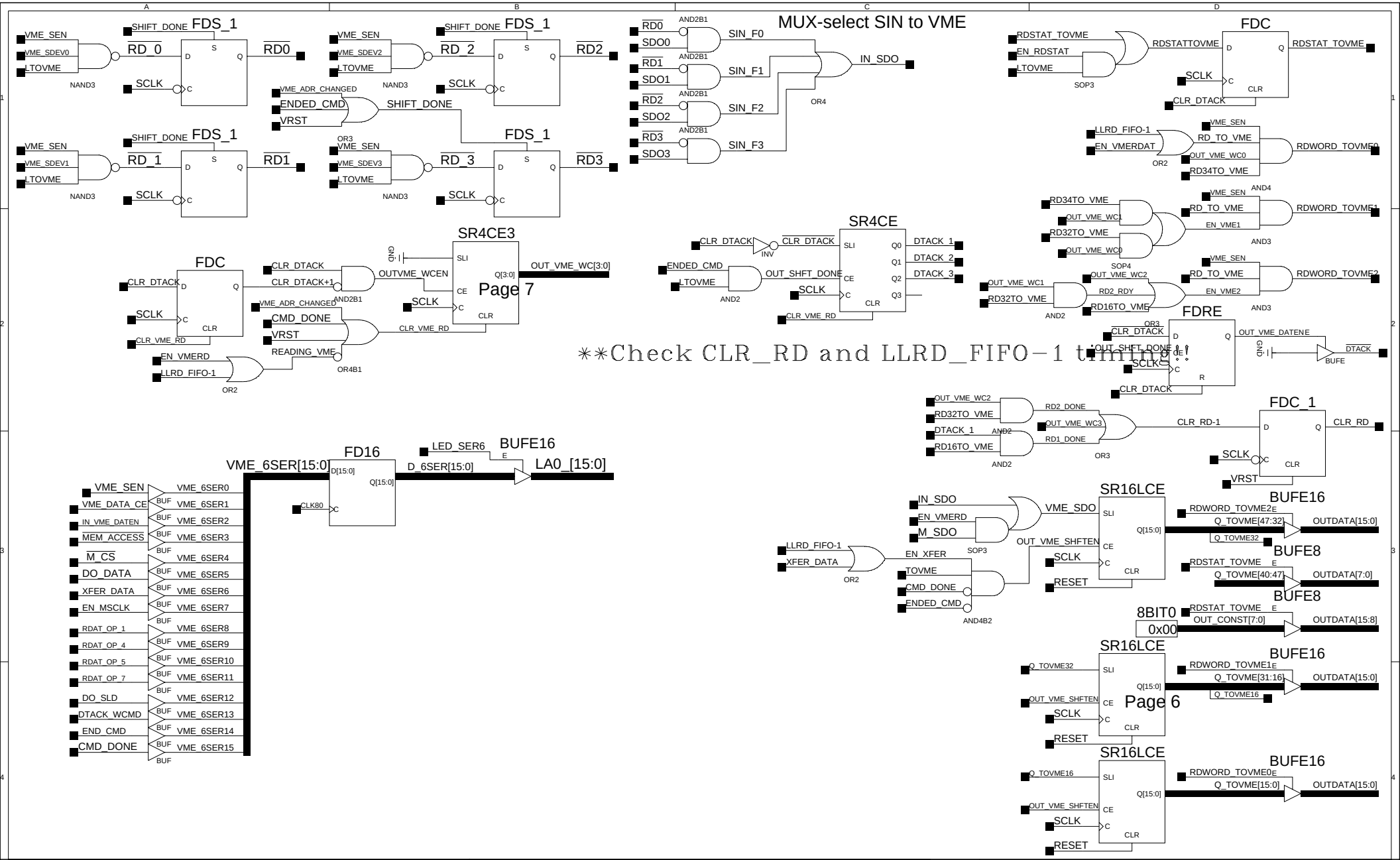
REAL_FMM 4-bit-decode definitions

0001: Warning/NearFULL (Grn ON, Yel BLINK)
0010: Lost Sync, need SyncReset (both BLINK)
0100: BUSY (Yel ON)
1000: Ready {DDU Ready == !Busy} (Grn ON)
1100: Error, need HardReset (Yel BLINK)








MUX-select SIN to VME
FDS_1
SR4CE3
SR4CE
FDC
FDRE
FDC_1
FD16
BUFE16
SR16LCE
BUFE8
Page 7
Page 6
**Check CLR_RD and LLRD_FIFO-1 timing!!
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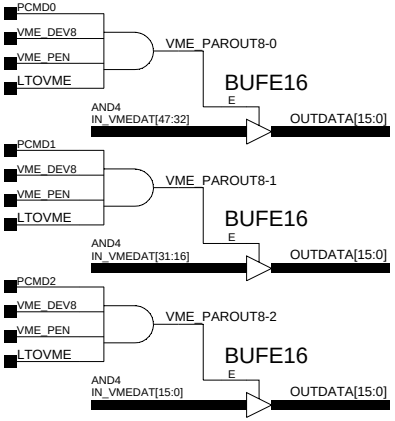
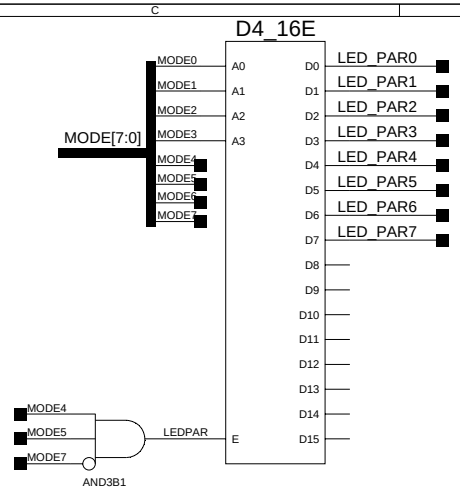
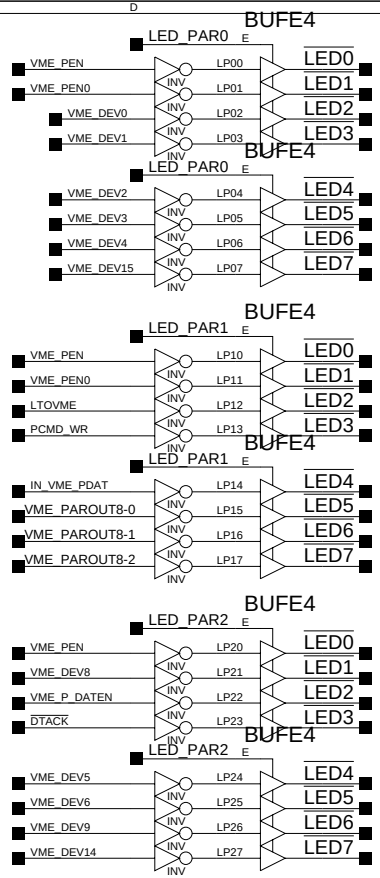
VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics
JRG
1
D785
7-18-2005_17:23
VMECNTRL . 11
2K

Parallel Register Readout



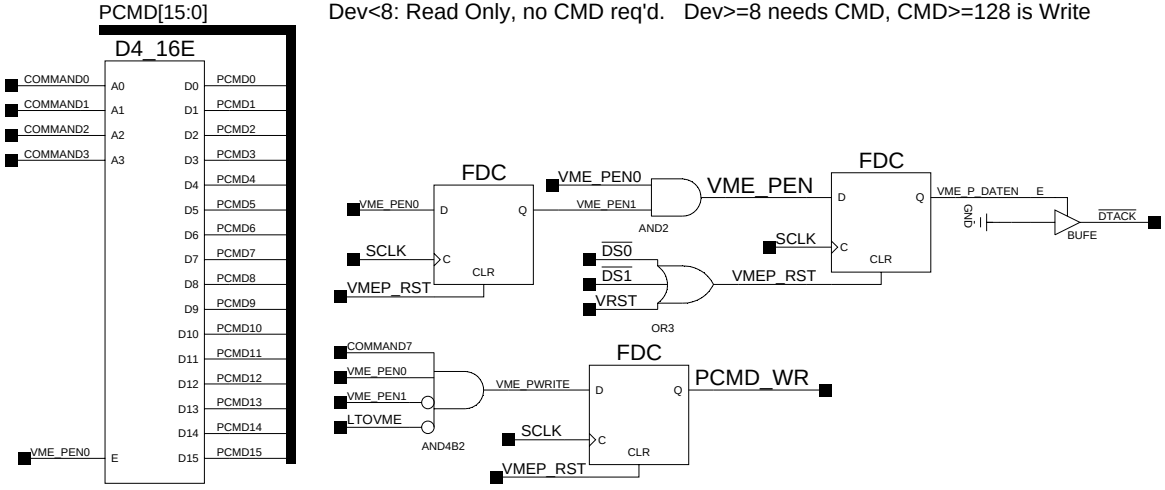




Parallel VME_ADR: slot[23-19]typ[18-16]dev[15-12]free[11-10]cmd[9-2]res[1-0]

PCMD[15:0]

Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write



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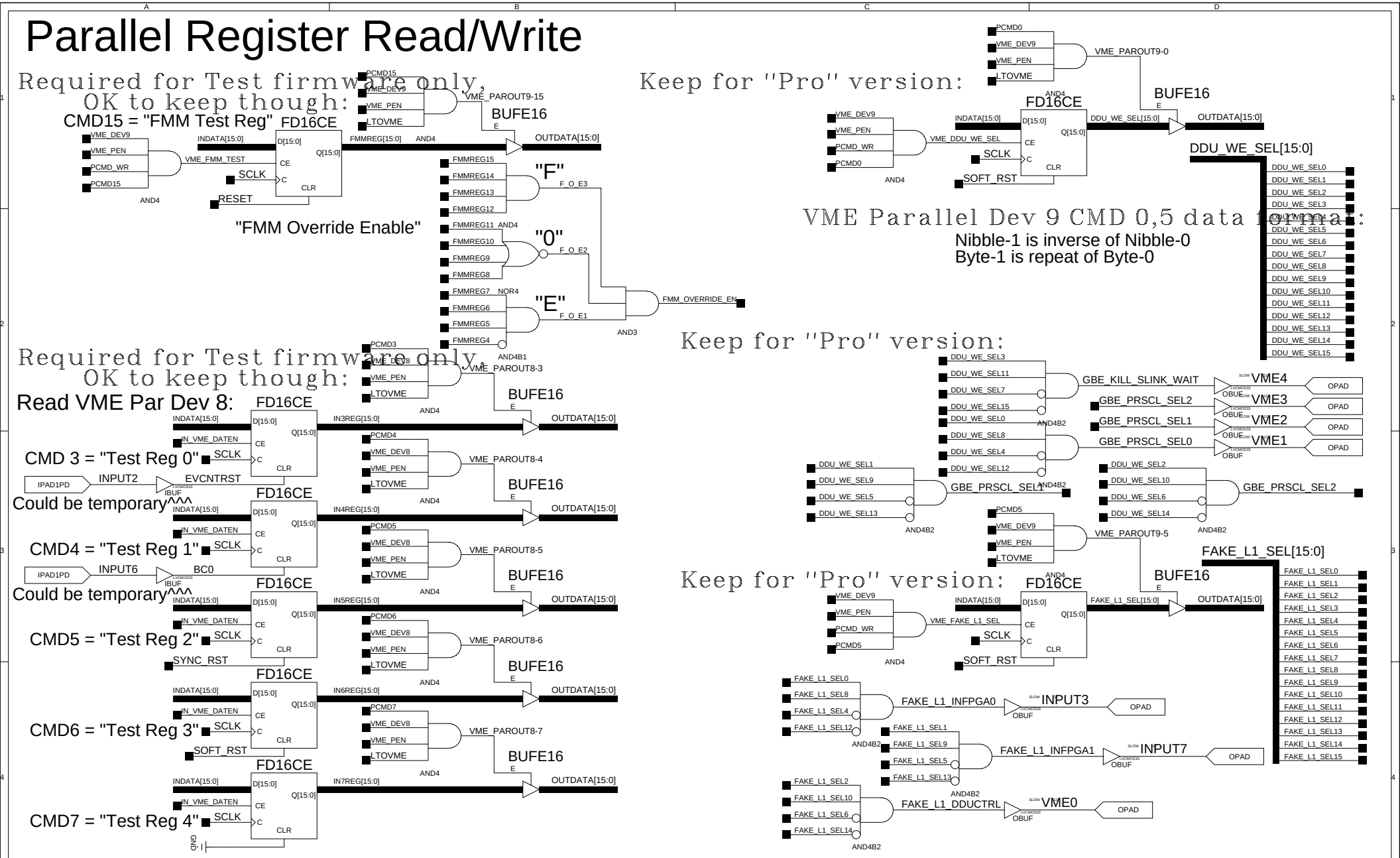
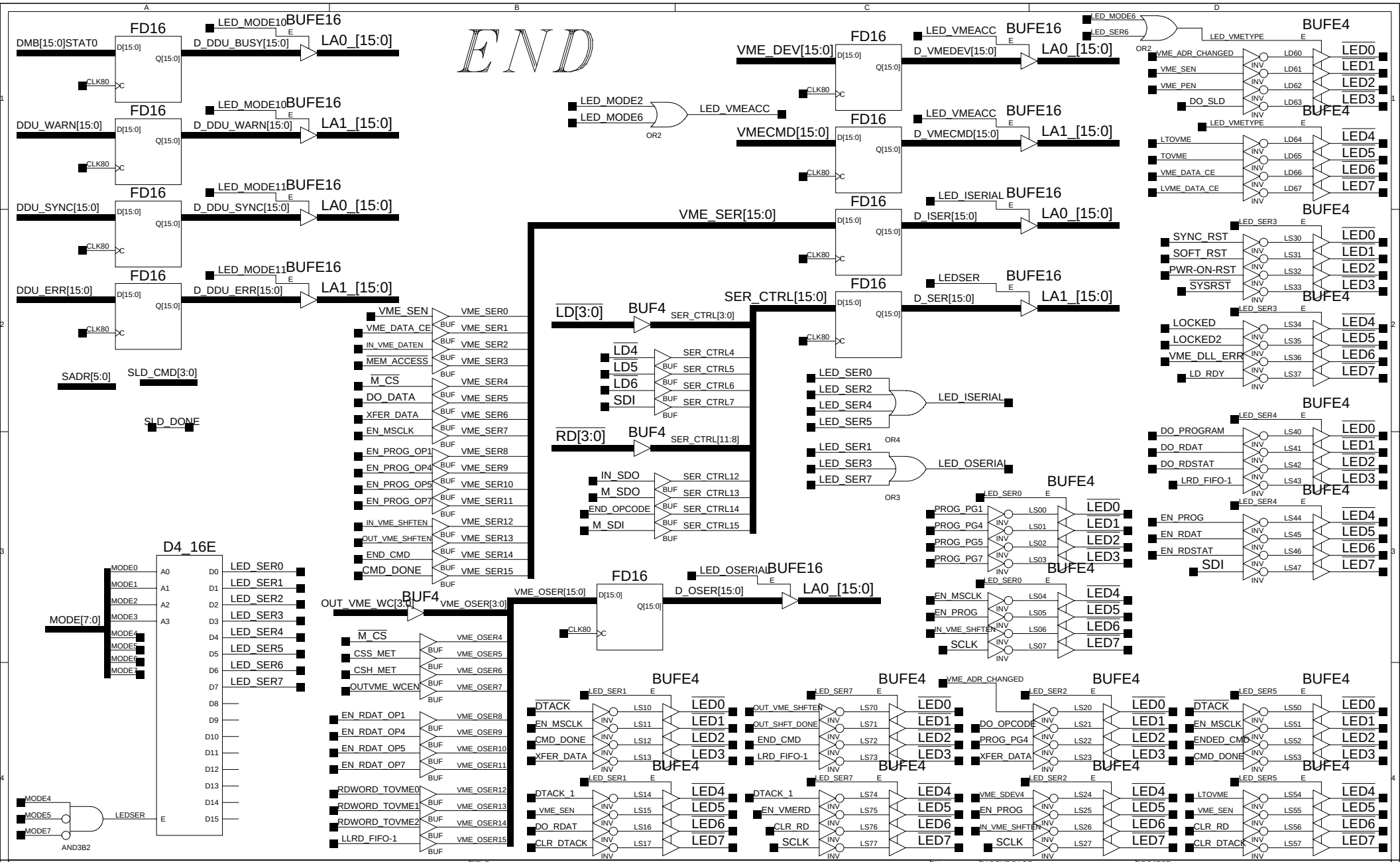
TITLE	VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY	JRG	PARENT PAGE	1
		DATE	9-1-2005_13:25	PROJECT	D785
				FILE	VMECNTRL . 12
				PAGE	2L

Parallel Register Read/Write

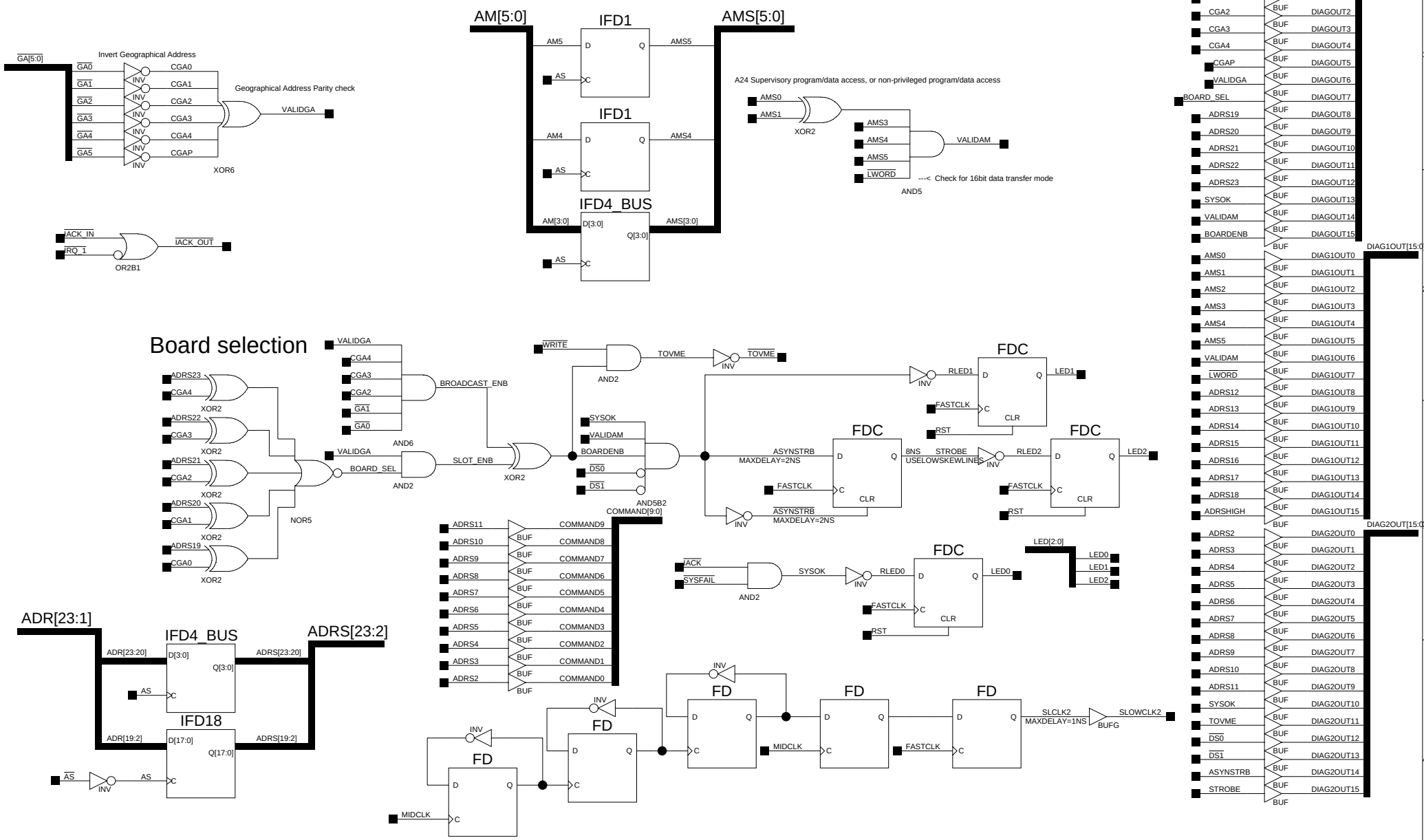


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785
		DATE: 6-30-2005_16:15	FILE: VMECNTRL . 13	PAGE: 2M

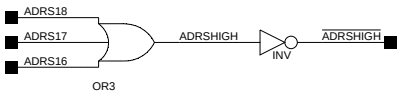


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Communication Interface DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 6-29-2005_17:03	PARENT PAGE: 1 FILE: VMECNTRL . 14
		PROJECT: D785	PAGE: 2N

DDU Broadcast Address = 28 = 0x1C = 11100b



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME-Address Decoder DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 5-25-2005_15:37	PARENT PAGE: 2A FILE: COMMAND . 1	PROJECT: D785B PAGE: 3A



Slot Selection: ADR[23:19] ADR[1:0]=Not Used

Device: ADR[15:12] sets device ID

Type: ADR[18:16]=000b for VME-JTAG

COMMAND[9:0] { ADR[11:8]=bit count
ADR[7:2]=JTAG command

slot[23-19]typ[18-16]dev[15-12]bitcnt[11-8]cmd[7-2]res[1-0]

ADR[18:16]=100b for VME-Serial

COMMAND[9:0] { ADR[11:6]=Not Used
ADR[5:2]=serial command (req'd for dev 4 only)

slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]

Dev>=8: Write Only. Dev=4 needs CMD, CMD>=9 is Write. Otherwise Read

ADR[18:16]=011b for VME-Parallel

Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write

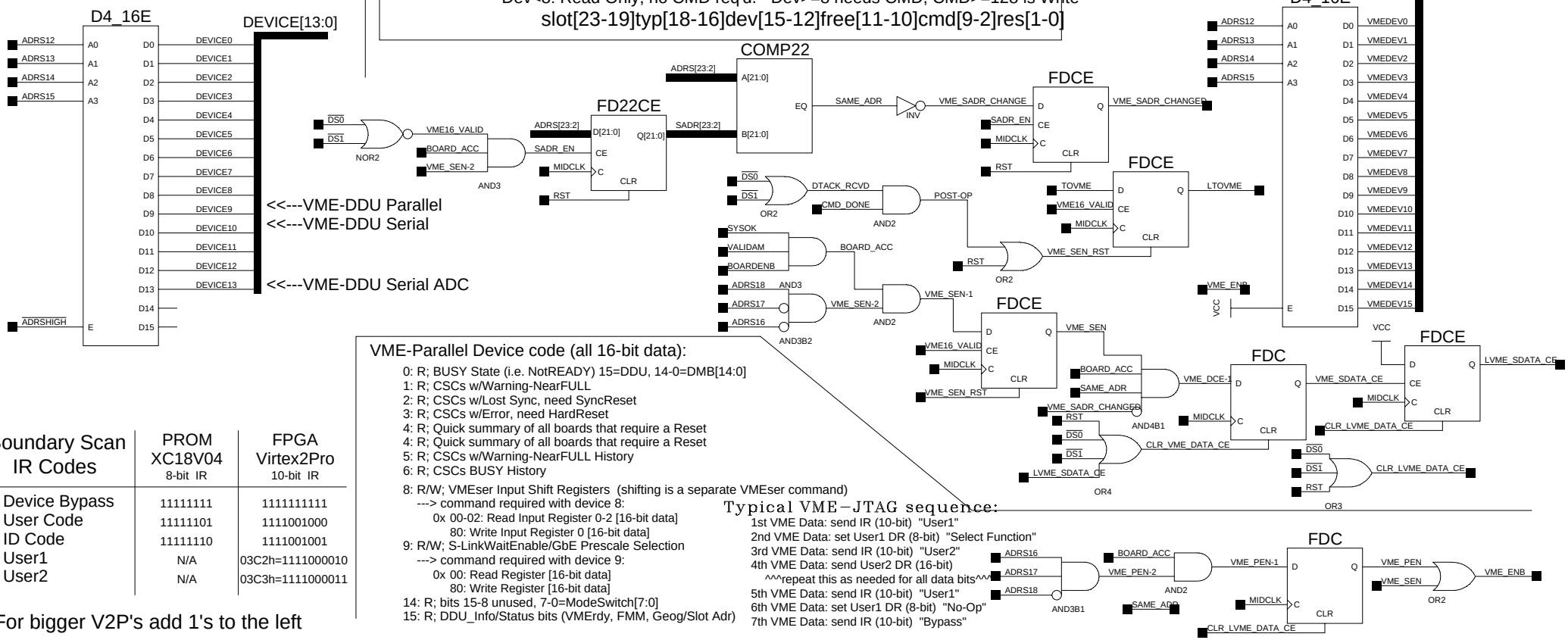
slot[23-19]typ[18-16]dev[15-12]free[11-10]cmd[9-2]res[1-0]

VME-JTAG Device code: Path IR bit length

00 ||	
01 || Output FIFO **FIX**	4
02 || VME_Ctrl PROM (all PROMs=XC18V04)	8
03 || DDU_Ctrl PROMs 1 & 0	8+8
04 || InCtrl PROMs 1 & 0	8+8
05 || DDU_Ctrl FPGA (V2P7)	10
06 || InCtrl FPGA 0 (V2P20)	14
07 || InCtrl FPGA 1 (V2P20)	14
08 || Input FIFOs 0-3	4+4+4+4
09 || Serial ADC (...not JTAG...)	N/A
0F || Emergency PROM Programming via VME	8

VME-Serial Device code:

00 || Read Input FIFO 0 (32-bit data, no Command req'd)
01 || Read Input FIFO 1 (32-bit data, no Command req'd)
02 || Read Input FIFO 2 (32-bit data, no Command req'd)
03 || Read Input FIFO 3 (32-bit data, no Command req'd)
04 || Flash SRAM (RdStat or Program Page), NEEDS COMMAND
---> command required with device 4:
0x 00: Read Status Register [8-bit data]
09: Program page 1 (Kill Ch.) [16 bit data]
0C: Program page 4 (DDR offsets) [32 bit data]
0D: Program page 5 (GBE offsets) [34 bit data]
0F: Program page 7 (Board ID) [16 bit data]
0C || Load GBE Output FIFO (SEN=LD, set HI during MRST)--N/A
0D || Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.)--N/A
0E || Load DDU_Ctrl FPGA (Board ID)--N/A
0F || Load all 4 DDR InFIFOs



VME-Parallel Device code (all 16-bit data):

0: R; BUSY State (i.e. NotREADY) 15=DDU, 14-0=DMB[14:0]
1: R; CSCs w/Warning-NearFULL
2: R; CSCs w/Lost Sync, need SyncReset
3: R; CSCs w/Error, need HardReset
4: R; Quick summary of all boards that require a Reset
4: R; Quick summary of all boards that require a Reset
5: R; CSCs w/Warning-NearFULL History
6: R; CSCs BUSY History
8: R/W; VMEser Input Shift Registers (shifting is a separate VMEser command)
---> command required with device 8:
0x 00-02: Read Input Register 0-2 [16-bit data]
80: Write Input Register 0 [16-bit data]
9: R/W; S-LinkWaitEnable/GbE Prescale Selection
---> command required with device 9:
0x 00: Read Register [16-bit data]
80: Write Register [16-bit data]
14: R; bits 15-8 unused, 7-0=ModeSwitch[7:0]
15: R; DDU_Info/Status bits (VMErdy, FMM, Geog/Slot Adr)

Typical VME-JTAG sequence:

1st VME Data: send IR (10-bit) "User1"
2nd VME Data: set User1 DR (8-bit) "Select Function"
3rd VME Data: send IR (10-bit) "User2"
4th VME Data: send User2 DR (16-bit)
^^^repeat this as needed for all data bits^^^
5th VME Data: send IR (10-bit) "User1"
6th VME Data: set User1 DR (8-bit) "No-Op"
7th VME Data: send IR (10-bit) "Bypass"

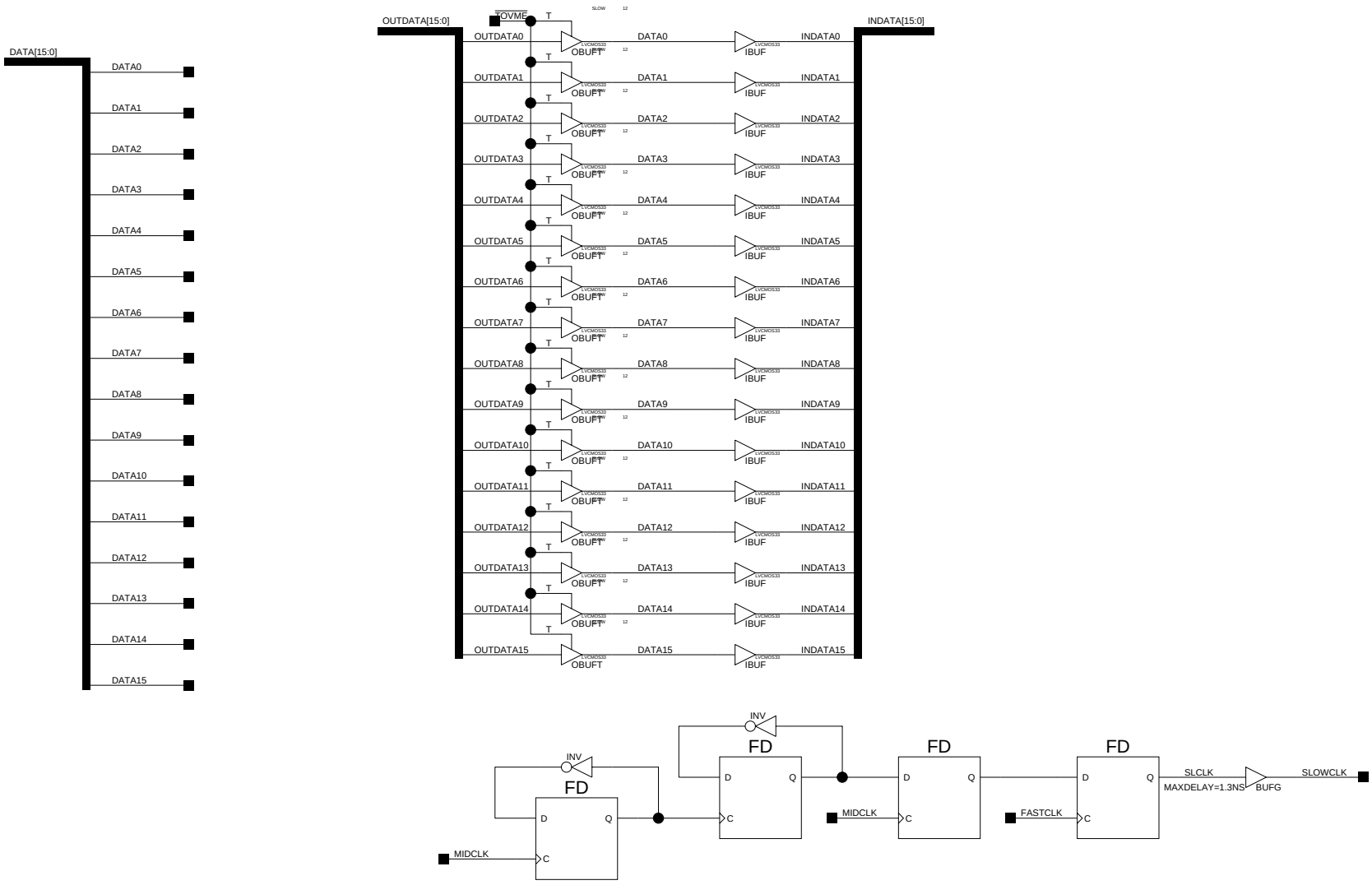
Boundary Scan IR Codes	PROM XC18V04 8-bit IR	FPGA Virtex2Pro 10-bit IR
Device Bypass	11111111	1111111111
User Code	11111101	1111001000
ID Code	11111110	1111001001
User1	N/A	03C2h=1111000010
User2	N/A	03C3h=1111000011

For bigger V2P's add 1's to the left

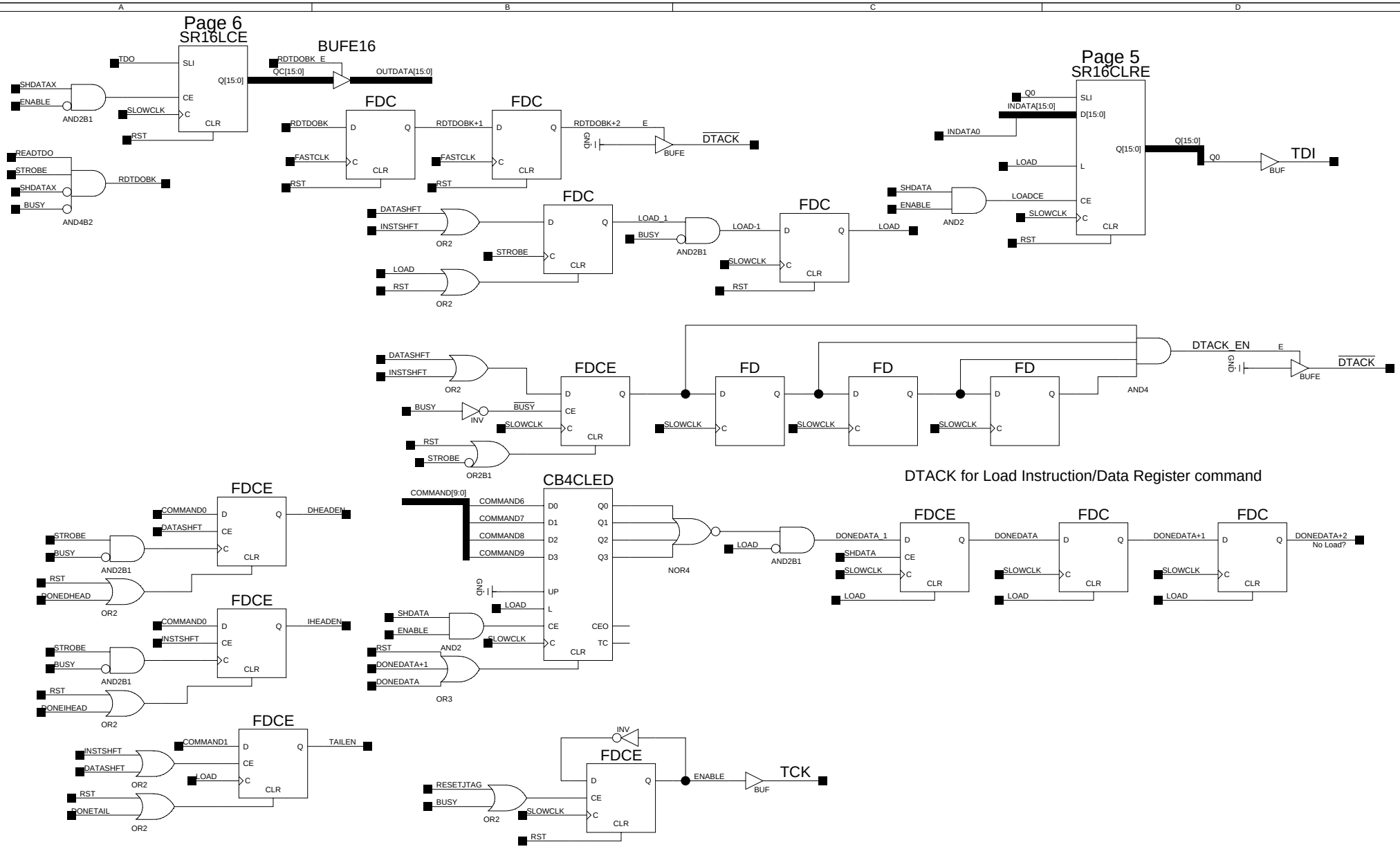
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: VME-Read Command Decoder
DDU VME Controller Logic
CMS CSC Electronics

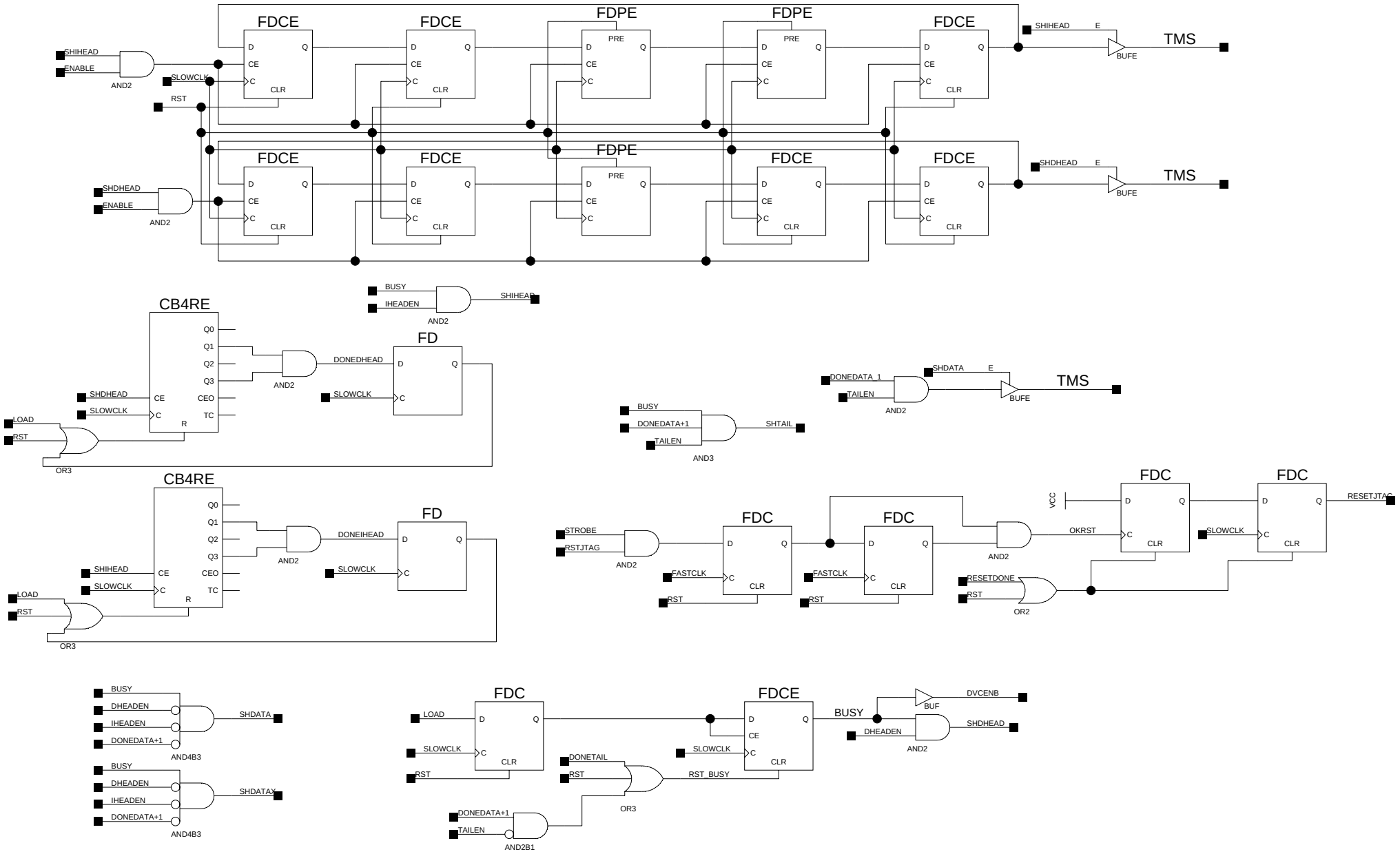
BY	PARENT PAGE	PROJECT
JRG	2A	D785B
DATE	FILE	PAGE
9-1-2005_14:27	COMMAND . 2	3B



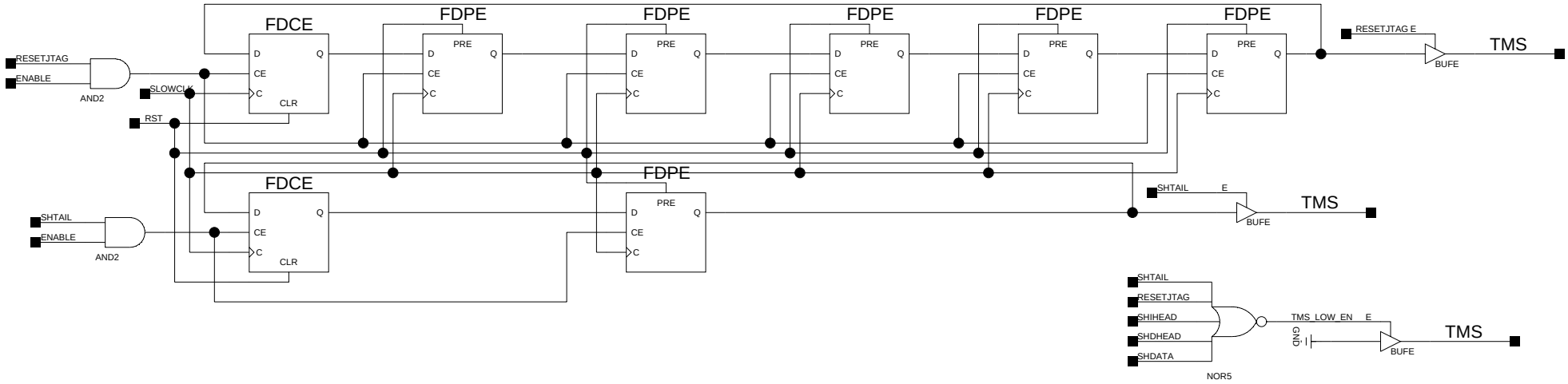
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME-Write Command Decoder DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2A	PROJECT: D785B
		DATE: 5-13-2005_11:36	FILE: COMMAND . 3	PAGE: 3C

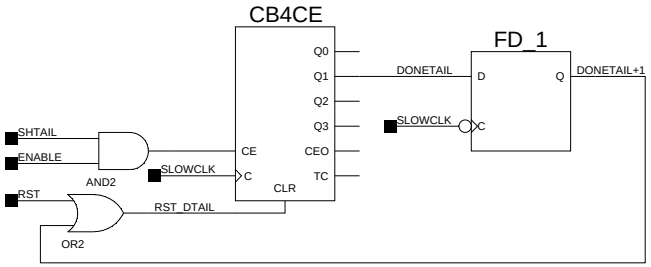


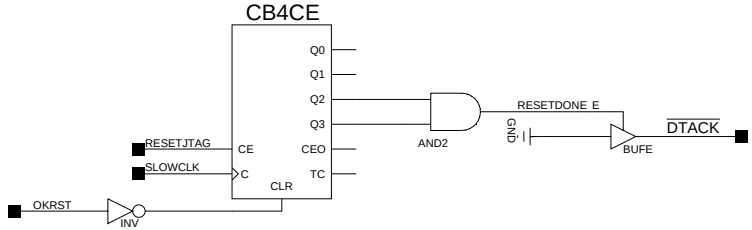
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785B
		DATE: 7-18-2005_17:25	FILE: VME-JTAG . 1	PAGE: 4A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY: JRG DATE: 4-8-2005_11:32	PARENT PAGE: 2 FILE: VME-JTAG . 2
		PROJECT: D785B	PAGE: 4B

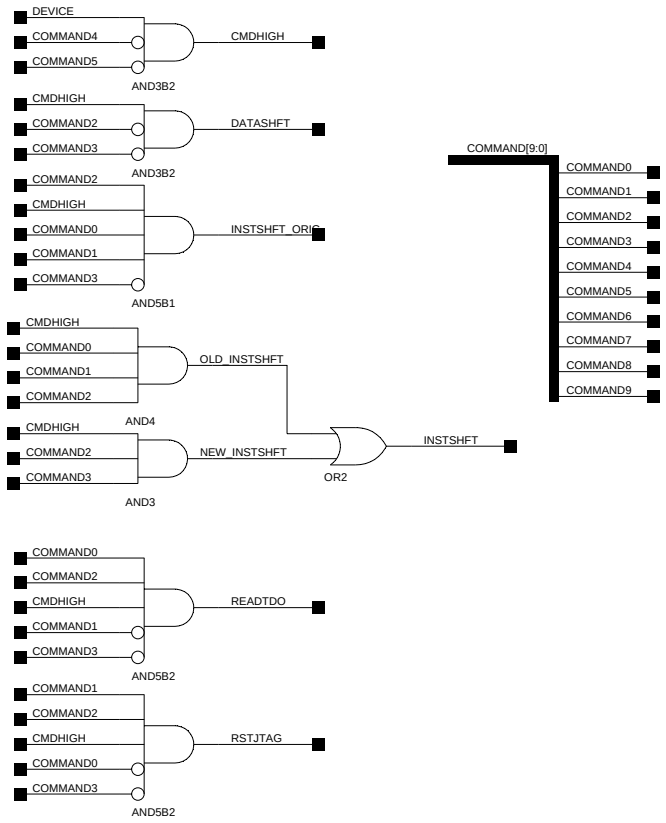






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE VME Interface-JTAG Converter DDU VME Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785B
		DATE 4-8-2005_11:32	FILE VME-JTAG . 3	PAGE 4C

CFEB JTAG command decode



CFEB JTAG commands:

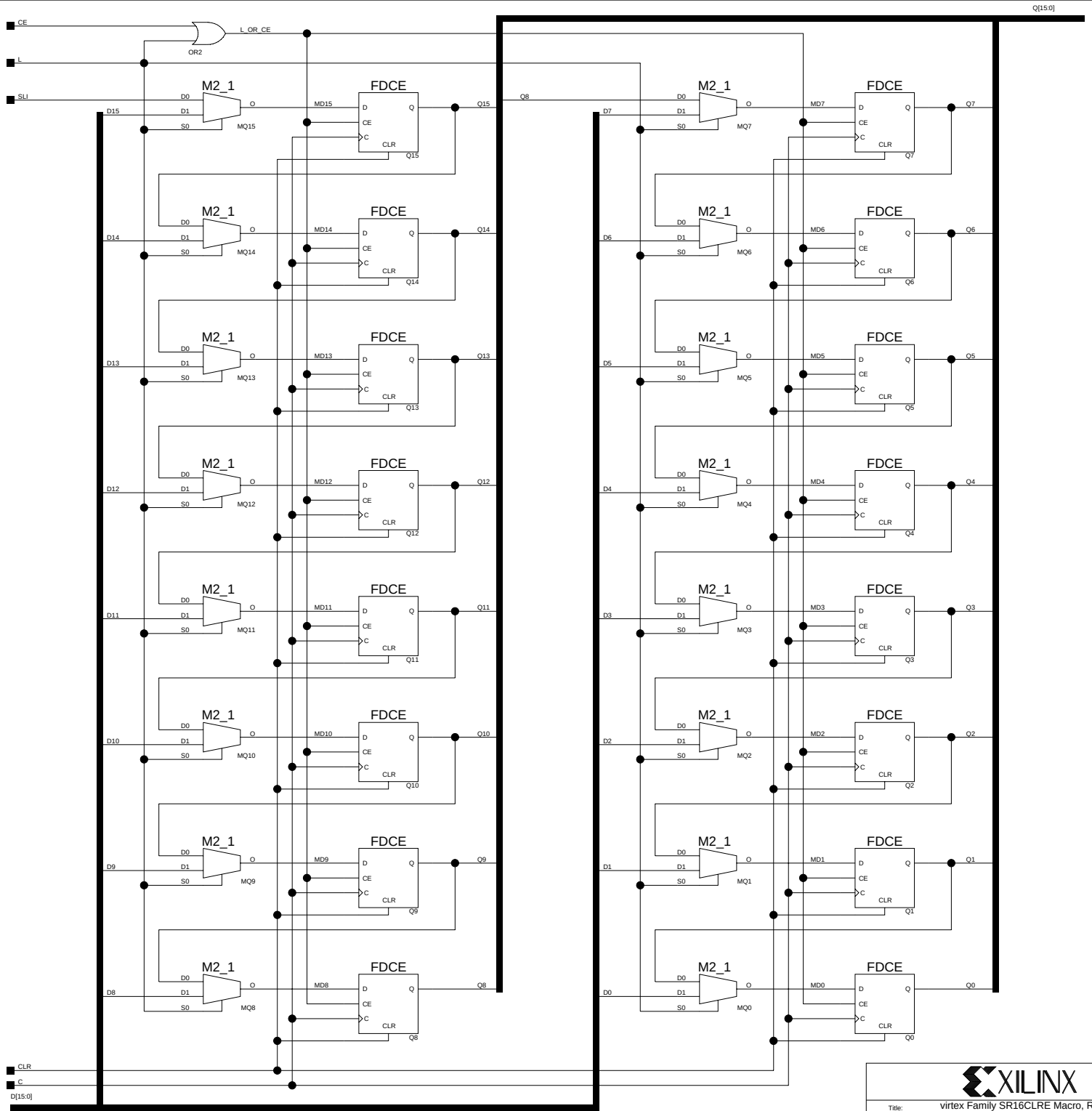
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register with header and tailer

0C || Shift IR, no header, no tailer
0D || Shift IR with header only
0E || Shift IR with tailer only
0F || Shift Instruction register with header and tailer

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: VME Interface-JTAG Converter
DDU VME Controller Logic
CMS CSC Electronics

BY: JRG | PARENT PAGE: 2 | PROJECT: D785B
DATE: 2-7-2005_9:32 | FILE: VME-JTAG . 4 | PAGE: 4D



drawn by KS

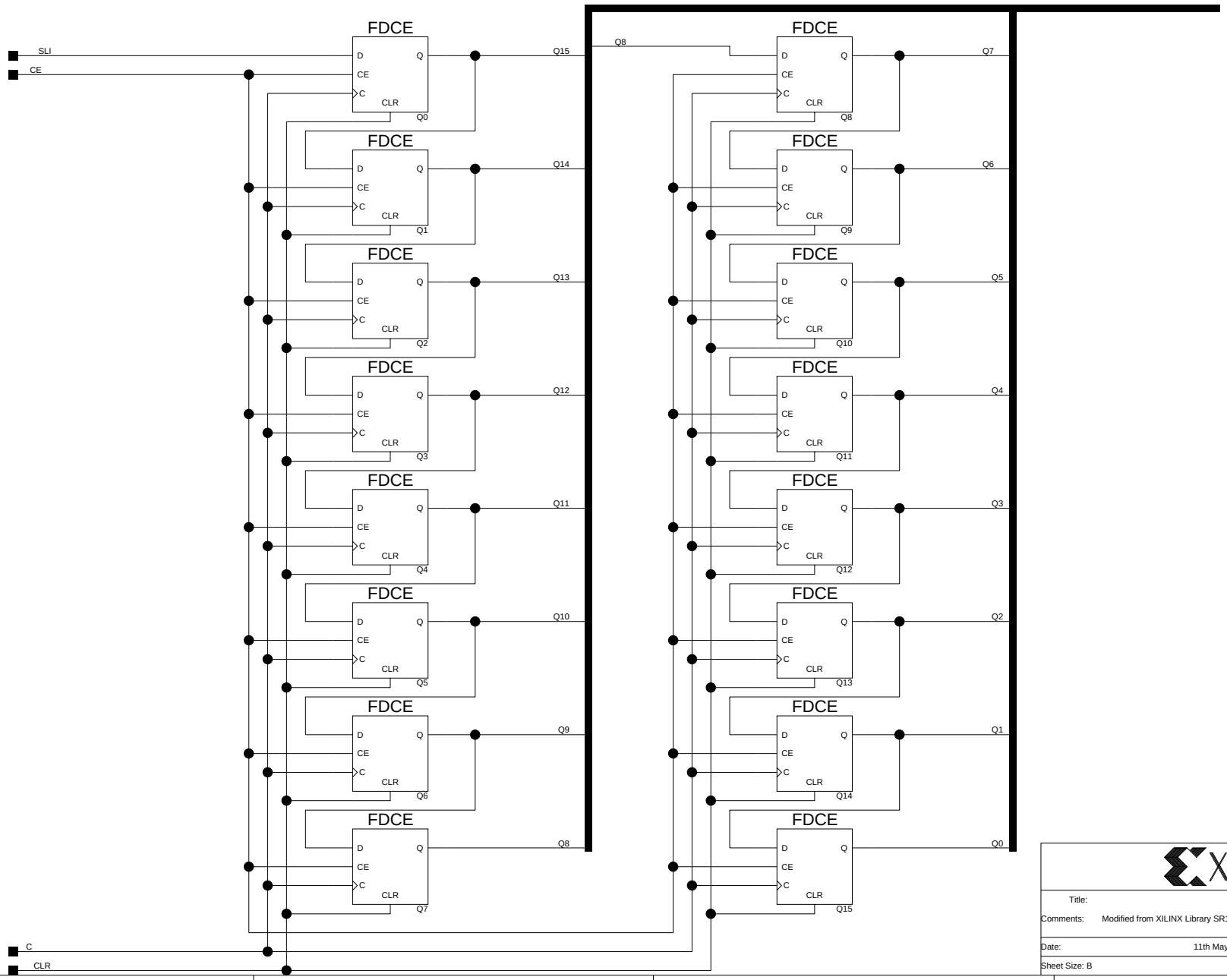
XILINX J. Gu

Title: virtex Family SR16CLRE Macro, Right Shift

Comments: 16-Bit Loadable Ser/Para-In, right shift
Para-Out Shift Reg w/ Enable & Async Clr

Date: 13th January 1993 | Ver: 1, Modified from XILINX, SR16CLE

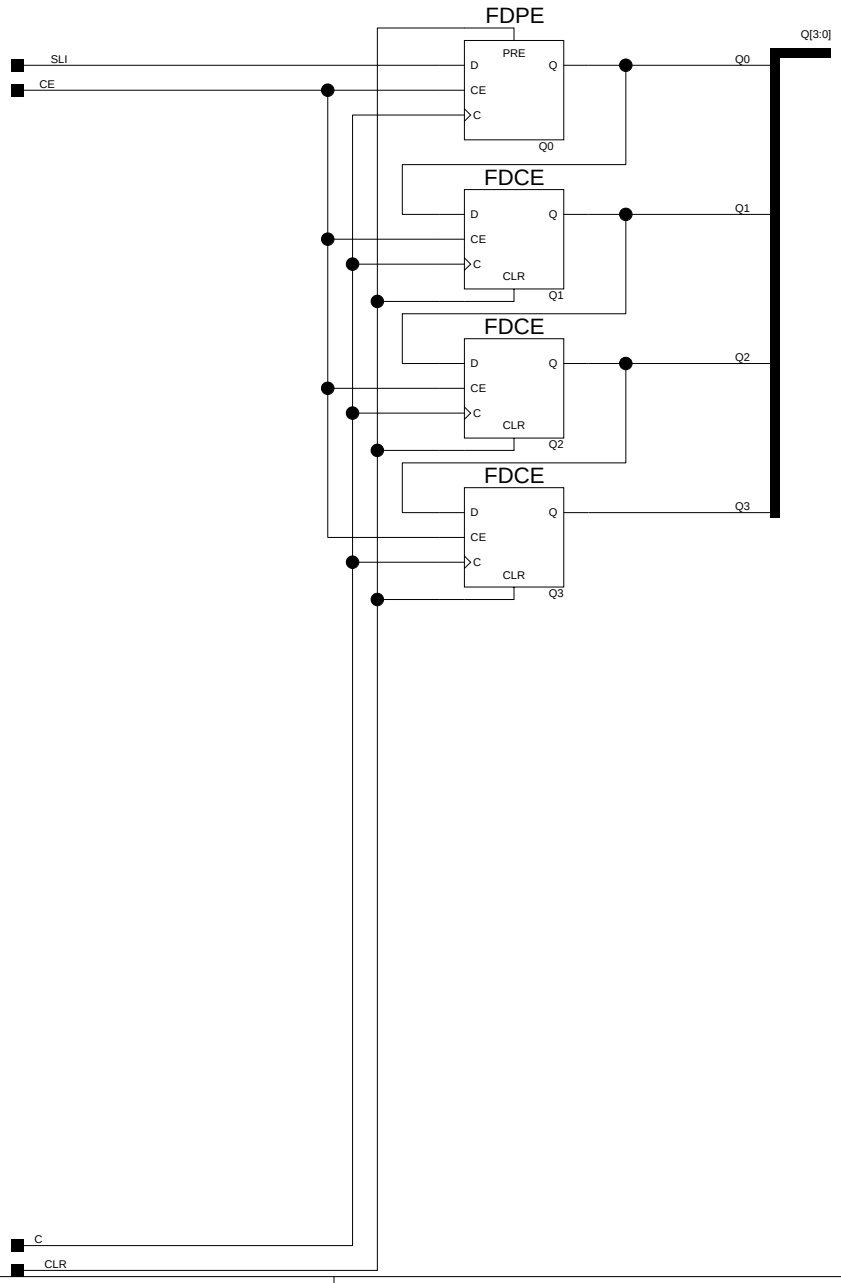
Sheet Size: C | Rev: A



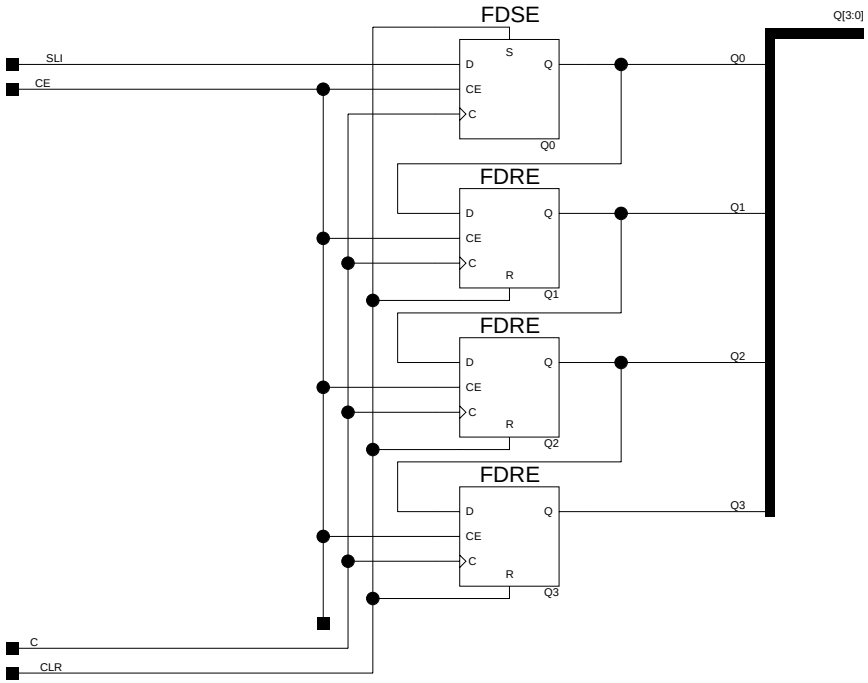
XILINX J. Gu

Title:	virtex Family SR16LCE Macro
Comments:	Modified from XILINX Library SR16CE, shift right 16-bit Serial-In Parallel-Out Shift Register w/ Enable and Async Clr
Date: 11th May 2001	Ver: 1
Sheet Size: B	Rev:

drawn by KS



Title:	VIRTEX Family SR4CE3 Macro (Set 1, Clear 3)	JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/Enable, 1 Preset & 3 Async Clr	
Date:	13th October 2003	Ver: 1
Sheet Size: B		Rev: A



drawn by KS

XILINX

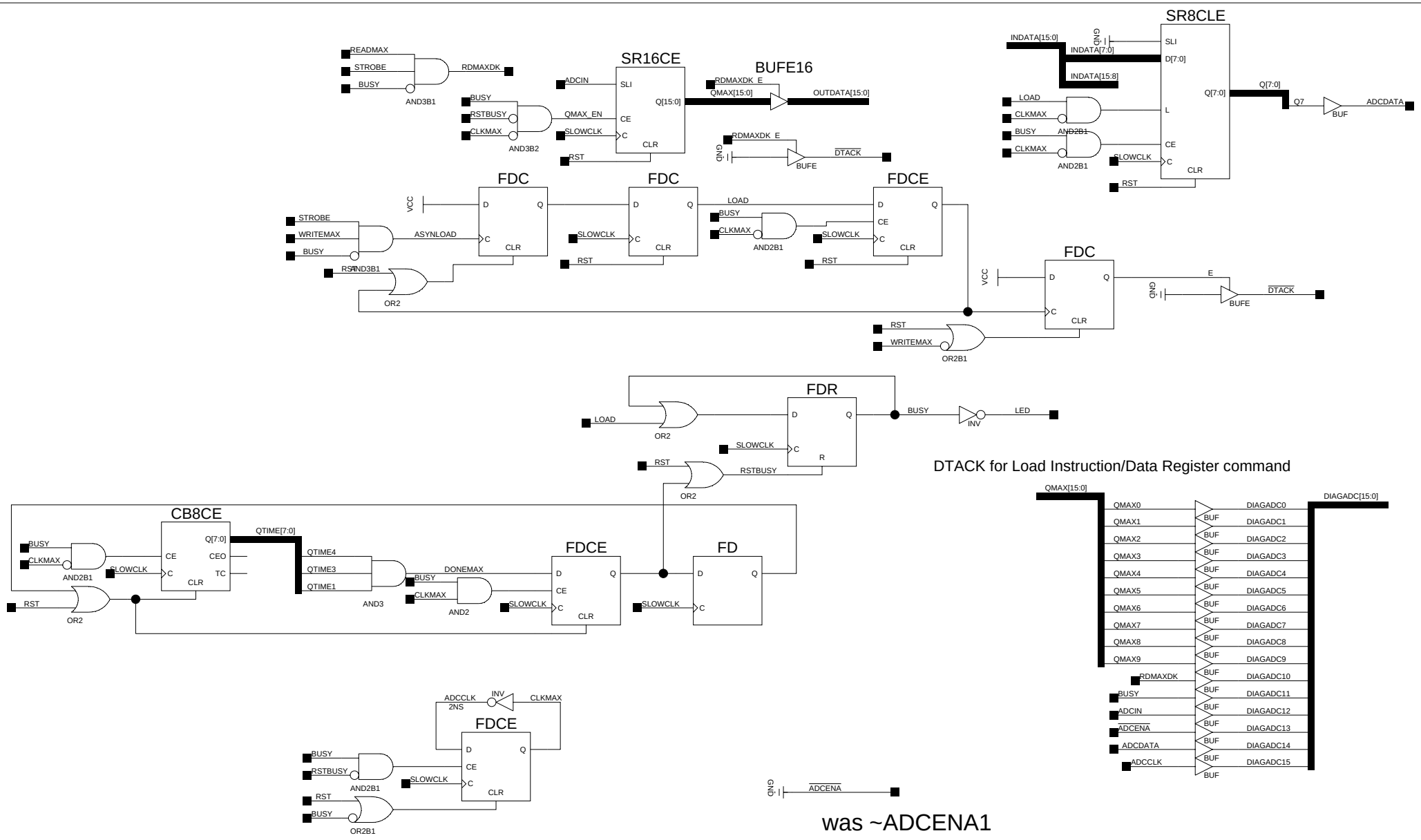
Title: VIRTEX Family SR4RE Macro (SR4E_ONE)

Comments: 4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset

JRG

Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A

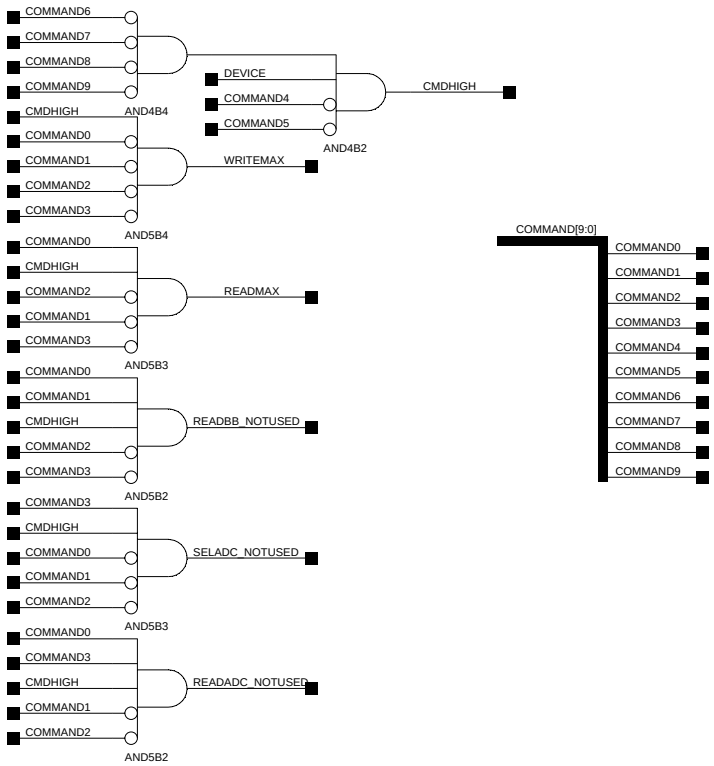


Serial ADC Interface MAX1271
DDU VME Controller Logic
CMS CSC Electronics

GU 2J D785

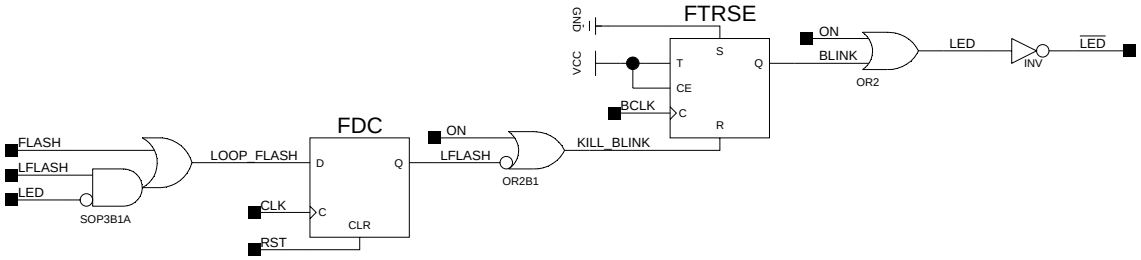
5-13-2005_10:48 SERADC 1 9A

CFEB JTAG command decode



Serial ADC Command Decoder:

00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 || Read Data Back from Burr-Brown Register; Not Used
04 ||
05 ||
06 ||
08 || Write Serial ADC Chip Select Register; Not Used
09 || Read Serial ADC Chip Select Register; Not Used



XILINX			JRG
Title:	FMMLED		
Comments:	Custom LED Slow-Blink Control for FMM Outputs		
Date:	27th January 2004	Ver:	1
Sheet Size: B		Rev:	A