New Ideas: Store & check DMB source ID's from each fiber?
Feed SLINK status into FMM logic (for UF).
Set DMB CRC OK flag for DDU Empty Events? no

DDU5CTRL (file 0dductrl) 10-5-2005_15:31

CMS CSC DDU5, Central Control FPGA CF026A01 Version 26

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits
Last w/DDU_FOV=4 --->> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Klll option
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VMEctrl
v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV=5
v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 bytes
v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--->rev2: SLOW8
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_Stat
v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDDR
Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisable,
Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/1
v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critical)
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB

Set All I/O to 3.3V

DDUCNTRL

PART=XC2VP7-6-FF672
PROM=2*XC18V04-VQ44 (PARALLEL)

TST	Clock	BUFGMUX		
0P	drck1	5P	*4P	-TR
2P	2clk	5S	*1S	
3S	clk	7S	*7S	
0S	clk625	2S-	*2S	
7P	ck125	1P	*0S	-BL
5P	clk40	0S	*3P	
4S-	clk156	4S-	*4S	
1S	drck2	3P	*5S	
6S-	sclk	6S-	*6S	

* denotes LOCed position

DDU5ctrl\DDU5ctrl\ddu5ctrl
C026DD99
C126DD99

PromID: 05026093h
FPGAid: 2124A093h

1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GbE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/CMD if SW8 is off
8: FPGA version on LEDs

LED0 on top, pins on away-side from LEDs
RST_1=Asynchronus Reset for FPGA1 and ALL FIF

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COLUMBUS OHIO 43210

To Do:
- COMPARE BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Determine correct values to store in Flash Mem
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case
- No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL

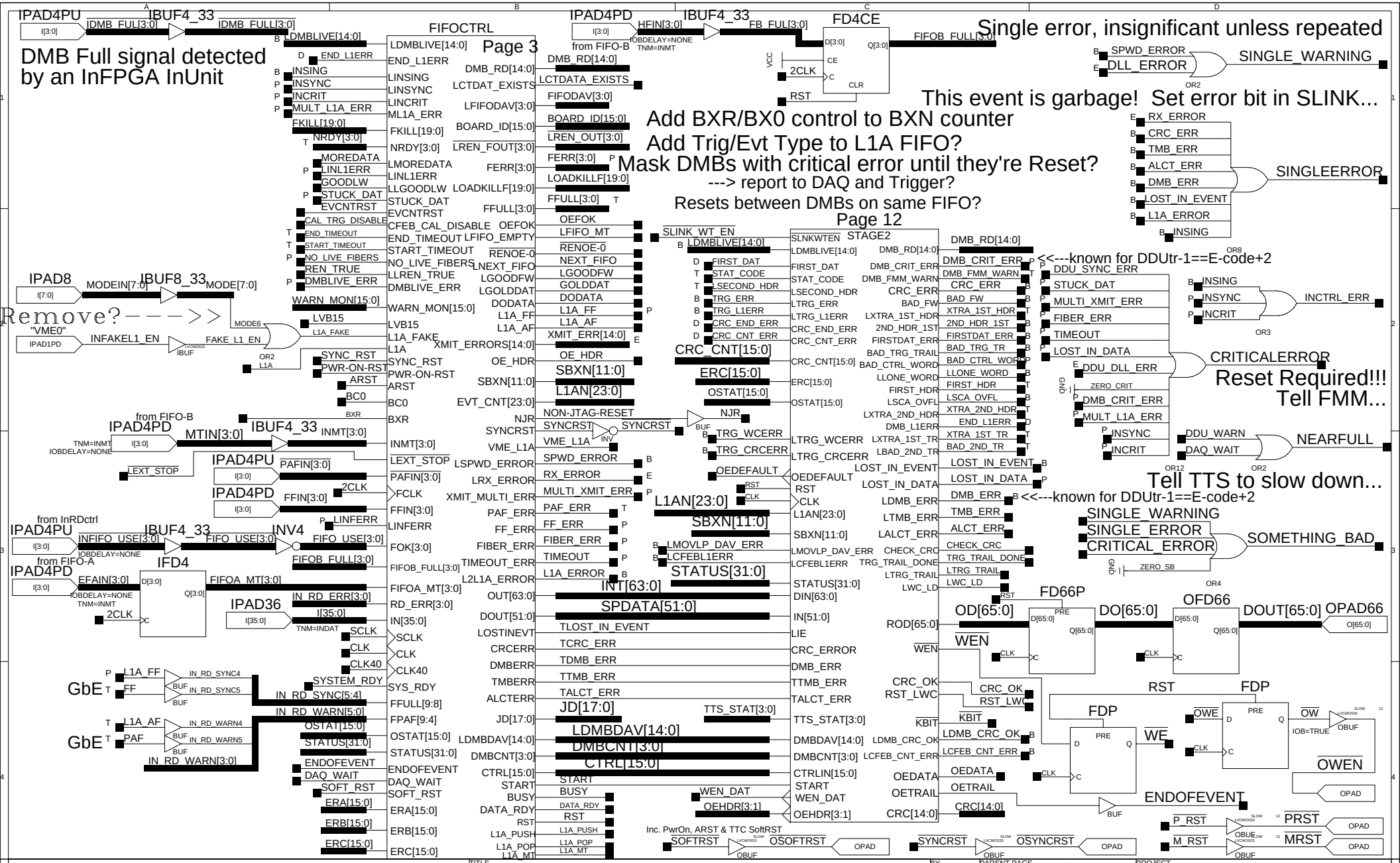
DDU Format Since DDUctrl v15:
BOE1_type L1A_Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK
49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH
LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000
DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP
EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

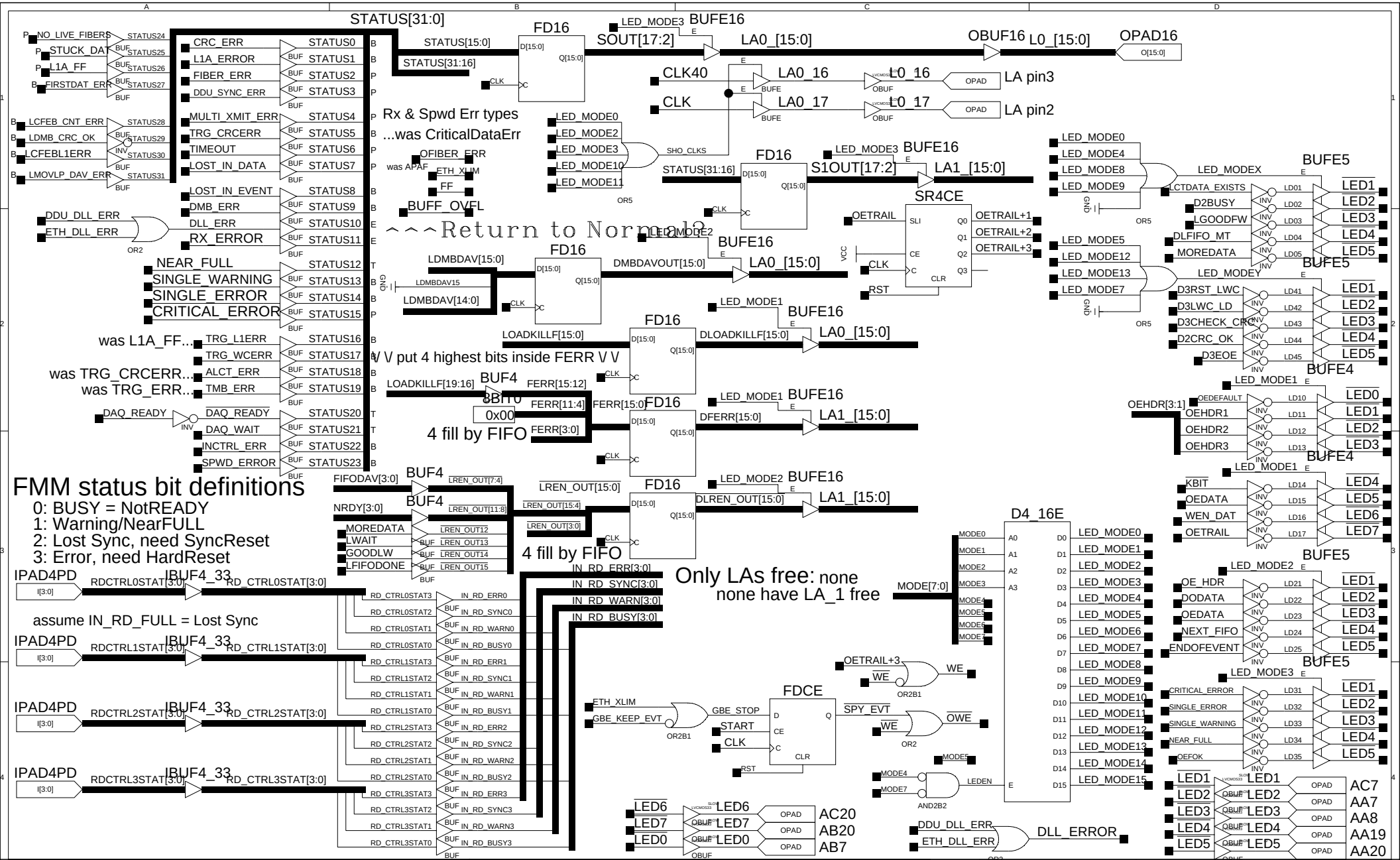
DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount 8 TS assumed

mojo

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-19-2005_11:28	PARENT PAGE: 1 FILE: DDUCNTRL . 1	PROJECT: D785C PAGE: 2


STATUS[31:0]
NO_LIVE_FIBERS
STUCK_DAT
L1A_FF
FIRSTDAT_ERR
LCFEB_CNT_ERR
LDMB_CRC_OK
LCFEBL1ERR
LMOVLP_DAV_ERR
CRC_ERR
L1A_ERROR
FIBER_ERR
DDU_SYNC_ERR
MULTI_XMIT_ERR
TRG_CRCERR
TIMEOUT
LOST_IN_DATA
LOST_IN_EVENT
DMB_ERR
DLL_ERR
RX_ERROR
NEAR_FULL
SINGLE_WARNING
SINGLE_ERROR
CRITICAL_ERROR
TRG_L1ERR
TRG_WCERR
ALCT_ERR
TMB_ERR
DAQ_READY
DAQ_WAIT
INCTRL_ERR
SPWD_ERROR
DDU_DLL_ERR
ETH_DLL_ERR
Rx & Spwd Err types
...was CriticalDataErr
OFIBER_ERR
was APAF
ETH_XLIM
FF
BUFF_OVFL
^^^Return to Normal?
was L1A_FF...
was TRG_CRCERR...
was TRG_ERR...
V V put 4 highest bits inside FERR V V
8BIT0
0x00
4 fill by FIFO
4 fill by FIFO
FMM status bit definitions
0: BUSY = NotREADY
1: Warning/NearFULL
2: Lost Sync, need SyncReset
3: Error, need HardReset
assume IN_RD_FULL = Lost Sync
Only LAs free: none
none have LA_1 free
FD16
BUFE16
BUFE5
BUFE4
BUF4
IBUF4_33
SR4CE
FDCE
D4_16E
OR5
OR2
OR2B1
AND2B2
OR3
IPAD4PD
OPAD
OBUF
BUFE
BUF
INV
LA pin3
LA pin2
AC20
AA7
AB20
AA8
AB7
AA19
AA20
DLL_ERROR
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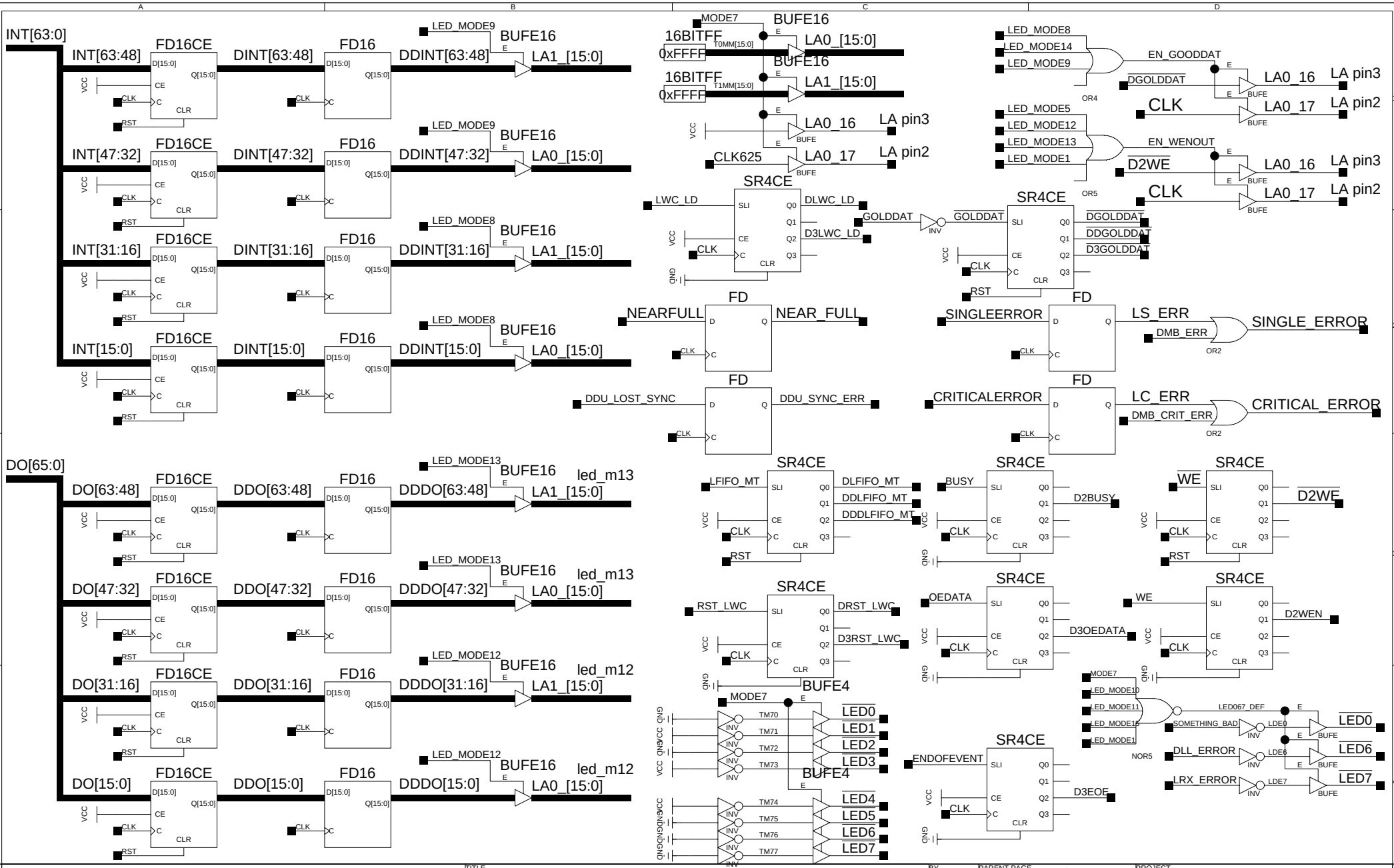
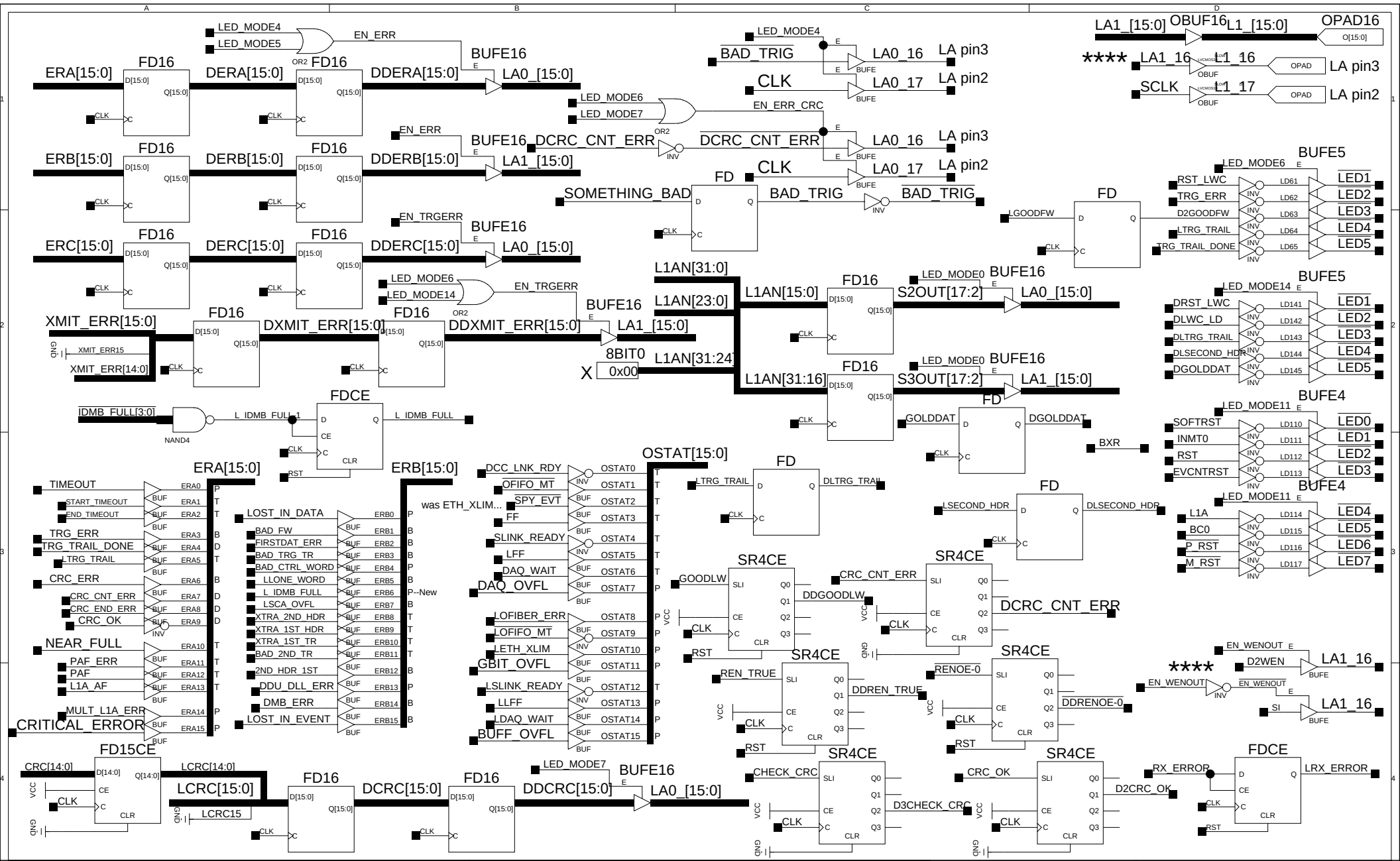
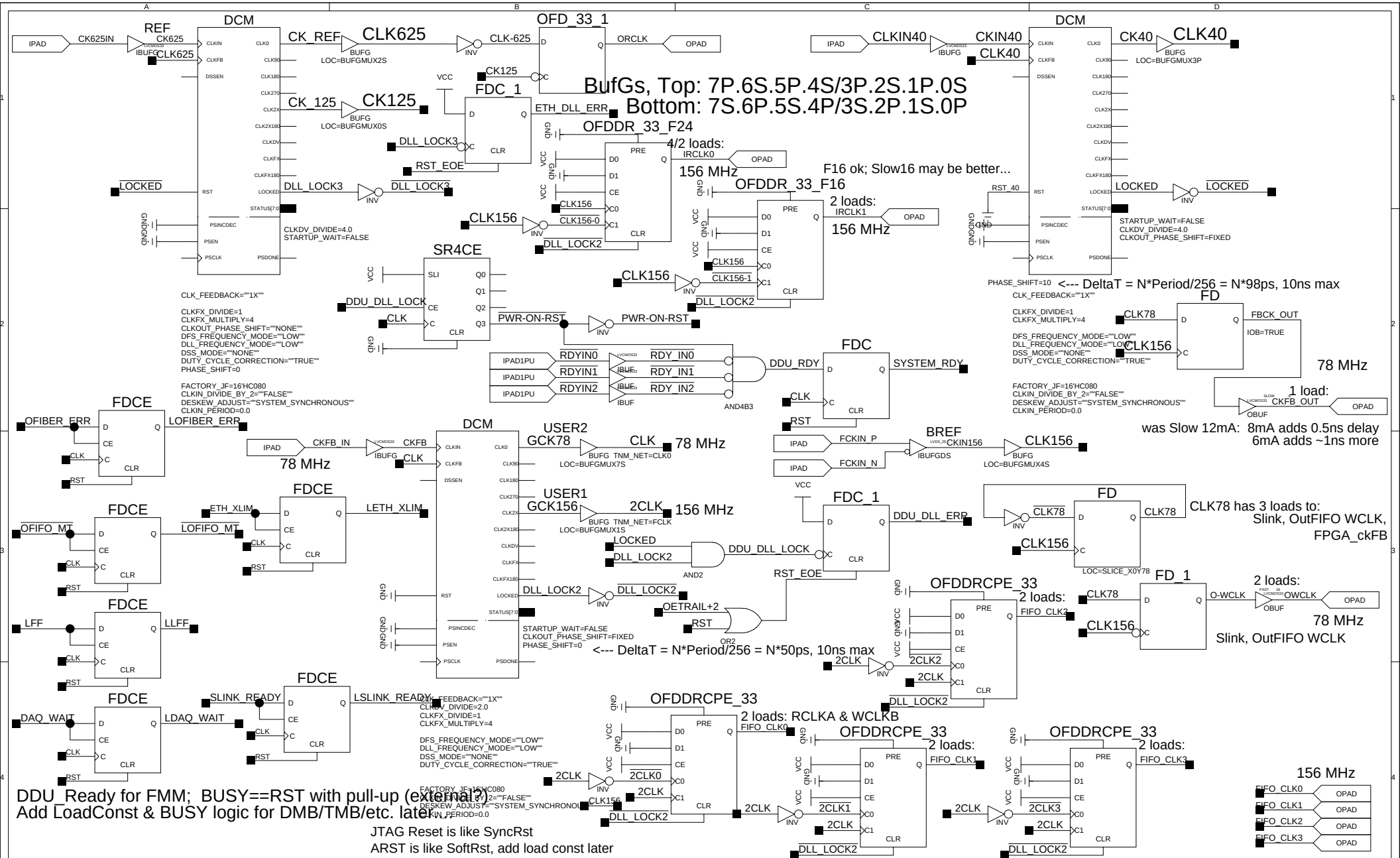
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
DDU Control
DDU Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
1
PROJECT
D785C
DATE
9-13-2005_14:48
FILE
DDUCNTRL . 2
PAGE
2A



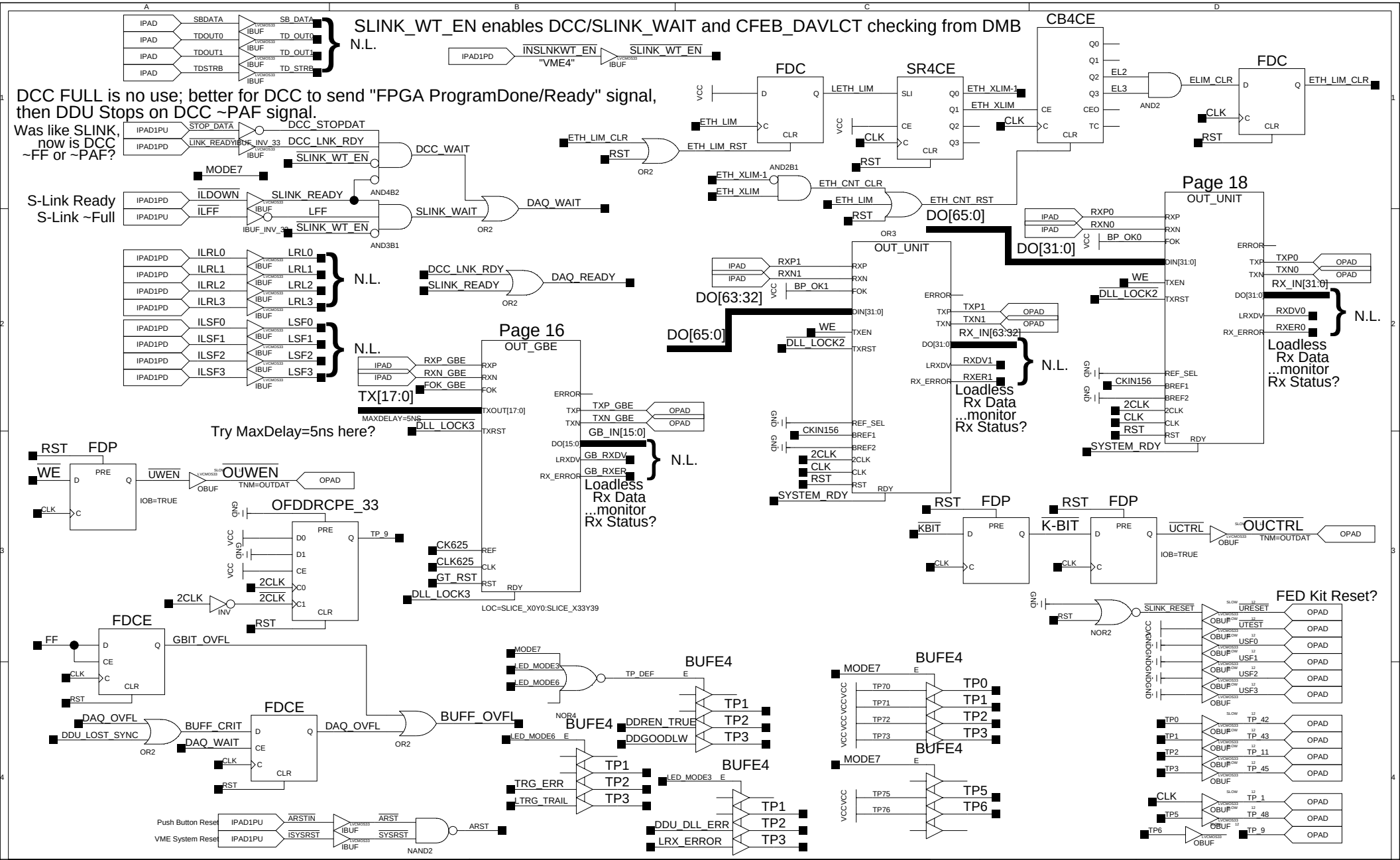
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-19-2005_9:57	PARENT PAGE: 1 PROJECT: D785C FILE: DDUCNTRL . 3 PAGE: 2B



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 9-19-2005_11:28	PARENT PAGE: 1 PROJECT: D785C FILE: DDUCNTRL . 4 PAGE: 2C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785C	
		DATE: 9-13-2005_14:40	FILE: DDUCNTRL . 5	PAGE: 2D	


SLINK_WT_EN enables DCC/SLINK_WAIT and CFEB_DAVLCT checking from DMB
N.L.
DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal, then DDU Stops on DCC ~PAF signal.
Was like SLINK, now is DCC ~FF or ~PAF?
S-Link Ready
S-Link ~Full
Page 16
Page 18
Try MaxDelay=5ns here?
Loadless Rx Data ...monitor Rx Status?
FED Kit Reset?
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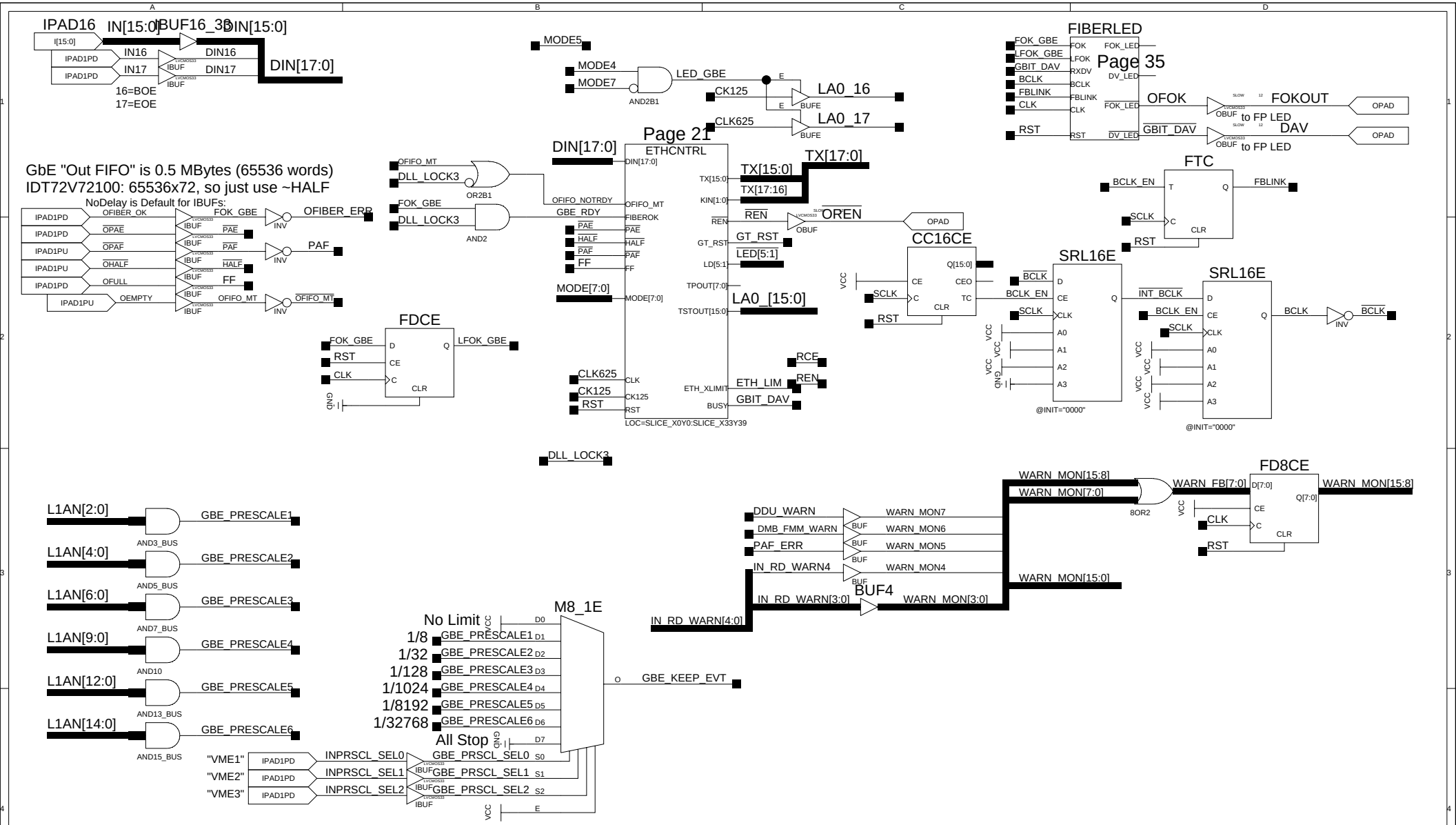
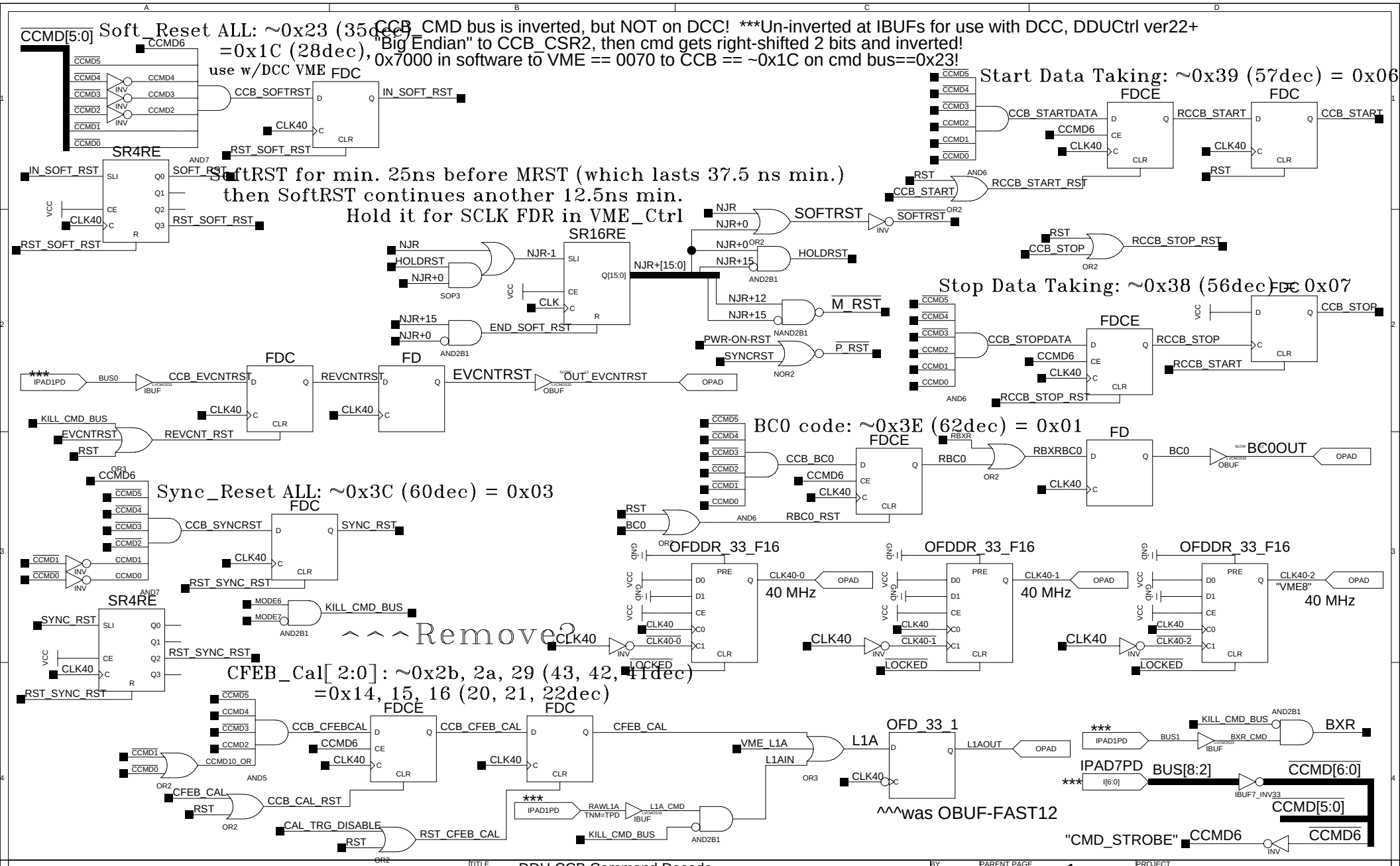
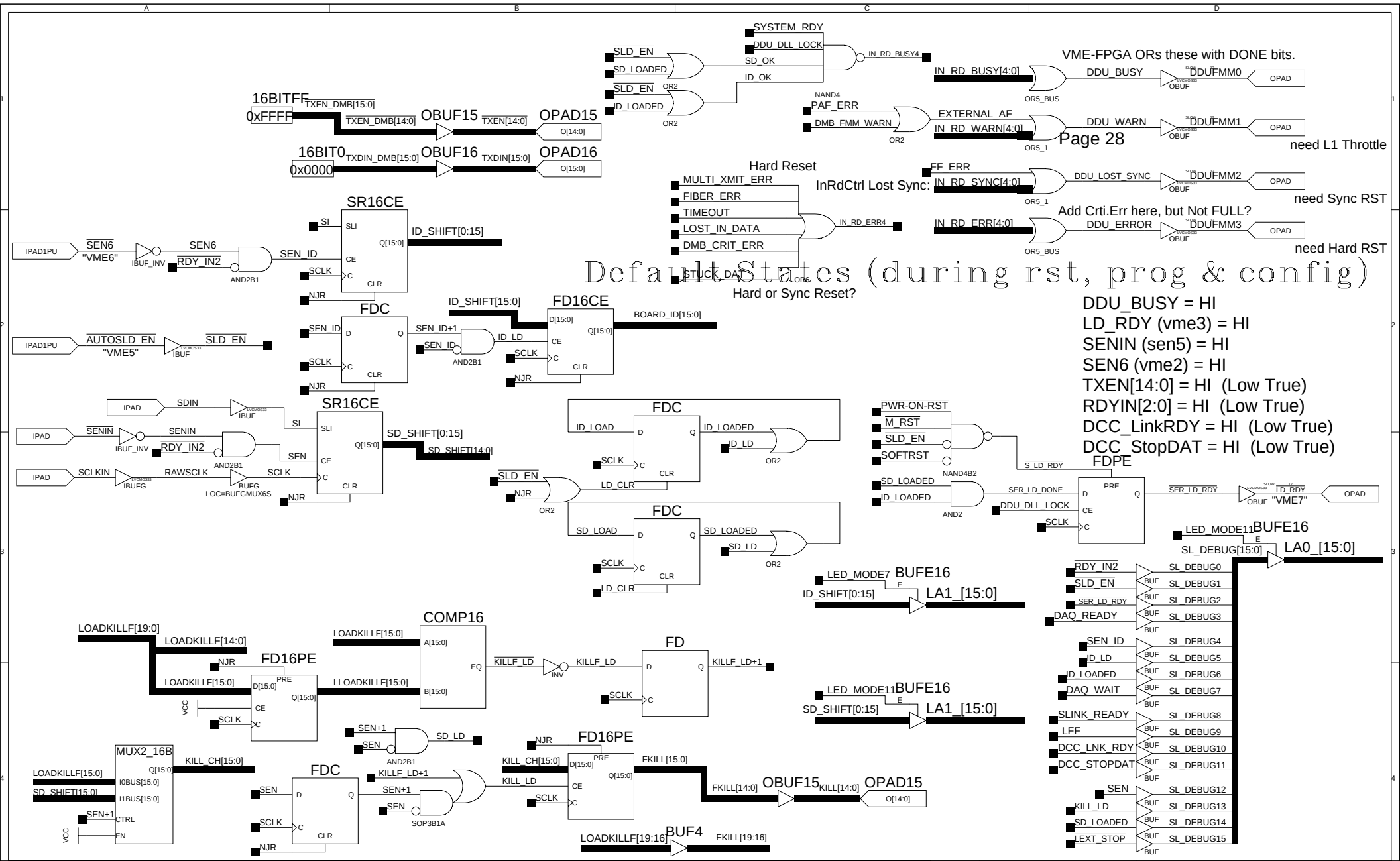
174 WEST 18TH AVE, COLUMBUS OH 43210
DDU Control
DDU Controller Logic
CMS CSC Electronics
JRG
1
D785C
7-18-2005_16:33
DDUCNTRL . 6
2E

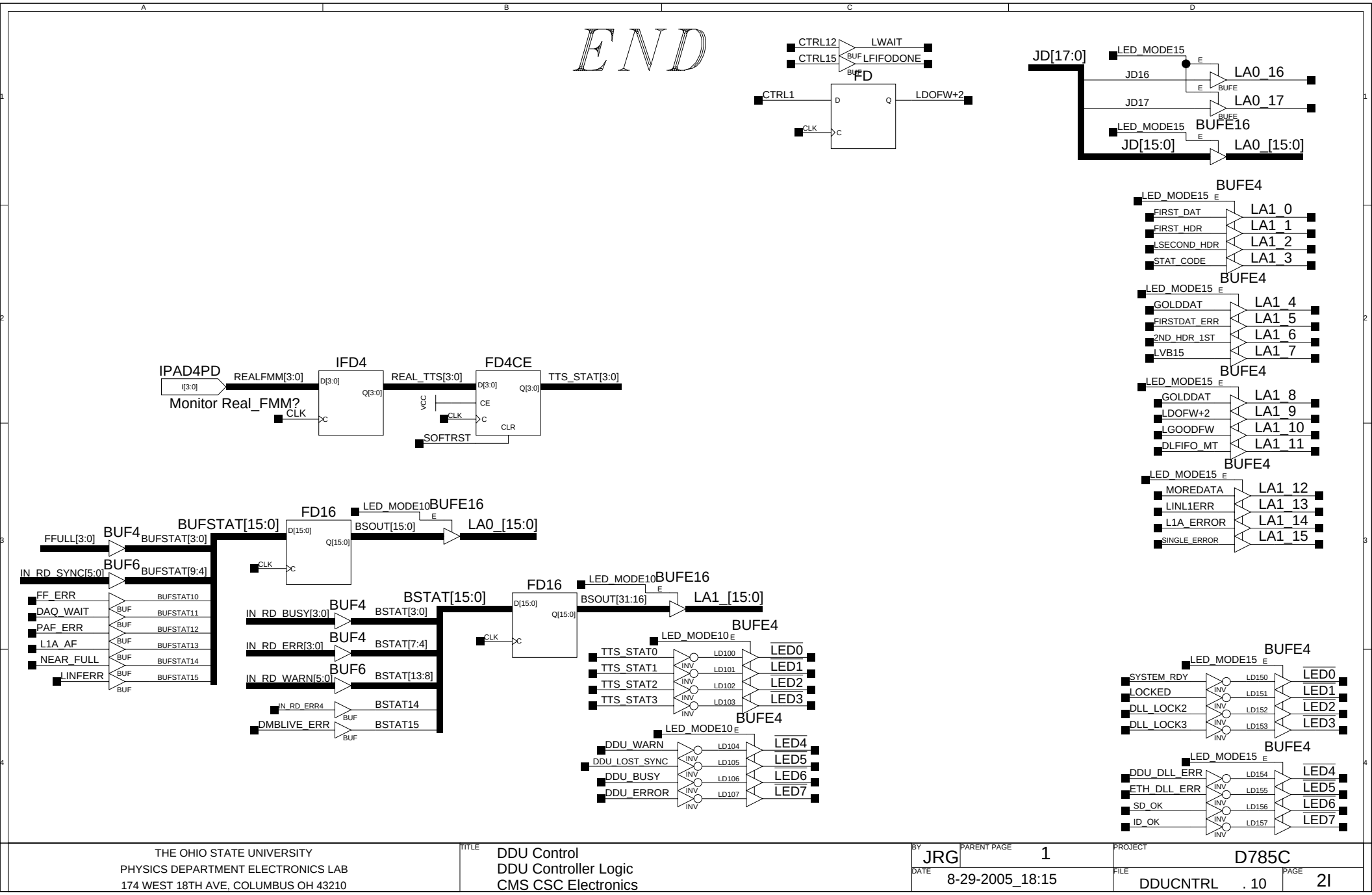


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 8-16-2005_10:30	PARENT PAGE: 1 FILE: DDUCNTRL . 7
		PROJECT: D785C	PAGE: 2F


CCMD[5:0]
Soft_Reset ALL: ~0x23 (35dec) =0x1C (28dec), use w/DCC VME
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
"Big Endian" to CCB_CSR2, then cmd gets right-shifted 2 bits and inverted!
0x7000 in software to VME == 0070 to CCB == ~0x1C on cmd bus==0x23!
Start Data Taking: ~0x39 (57dec) = 0x06
SoftRST for min. 25ns before MRST (which lasts 37.5 ns min.)
then SoftRST continues another 12.5ns min.
Hold it for SCLK FDR in VME_Ctrl
Stop Data Taking: ~0x38 (56dec) = 0x07
BC0 code: ~0x3E (62dec) = 0x01
Sync_Reset ALL: ~0x3C (60dec) = 0x03
^^^Remove?
CFEB_Cal[2:0]: ~0x2b, 2a, 29 (43, 42, 41dec)
=0x14, 15, 16 (20, 21, 22dec)
40 MHz
40 MHz
"VME8"
40 MHz
^^^was OBUF-FAST12
"CMD_STROBE"
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
DDU CCB Command Decode
DDU Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 1
PROJECT D785C
DATE 8-8-2005_15:29
FILE DDUCNTRL . 8
PAGE 2G



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Control DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 1	PROJECT D785C
		DATE 8-16-2005_10:27	FILE DDUCNTRL . 9	PAGE 2H



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 8-29-2005_18:15	PARENT PAGE: 1 FILE: DDUCNTRL . 10
		PROJECT: D785C	PAGE: 2I

RXER3:0-->1:0 FEND3:0-->FEND1:0 LW1:0-->LW ~NODAT1:0-->~NODAT

CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

Use these busses for CFEB CRC and Special Word checks-->>

FD4CE next-to-last word on DAT (last DMB E-codes)

LW, OLW1, OLW2, OLW3, LREN_TRUE, GND, CLK, RST → D0..D3, CE, C, CLR → Q0..Q3 → LGOODLW, OLGOODLW1, OLGOODLW2, OLGOODLW3

N.L.

RDAT35, RDAT34, RDAT33, RDAT32 → NAND4 → NODAT

Lowest 36 RDAT bits synched to falling edge of CLK

IN[35:0] → IFDDR36C (D[35:0], CLK, RST, CLR → Q[71:0], QS[71:0]) → RDAT[71:0]

(next-to-last word bits) comes with E-codes of last DMB only, followed by C-codes

Page 5

DAT[71:0]

OEFOK, RDAT35, RDAT34 → AND3B1 → LW

OEFOK, DAT16 → AND2 → RXER0

OEFOK, DAT52 → AND2 → RXER1

RXER[1:0] "FILL Flag"

DAT[15:0] BUF16 OUT[15:0]

DAT[33:18] BUF16 OUT[31:16]

DAT[51:36] BUF16 OUT[47:32]

DAT[69:54] BUF16 OUT[63:48]

OUT[63:0]

GND, OUT38, OUT37, OUT36 → BUF → DCNT3, DCNT2, DCNT1, DCNT0 → DCNT[3:0]

OUT39 → BUF → INL1ERR

FEND appears at end: sometimes never

DAT17, DAT53 → BUF → FEND0, FEND1

set for first 2 E-codes from each DMB should be always zero

EVT_CNT[23:0]

CB16CE: START, CLK, EVCNTRST, RST → OR2 → RST_EVCNT; Q[15:0], CE, CEO, TC, CLR → EVT_CNT[15:0]

CB8CE: CLK, CE, CEO, TC, CLR → Q[7:0] → EVT_CNT[23:16]

EVT_CNT[15:0] → COMP16 A[15:0] EQ; L1AN[15:0] → B[15:0]

EVT_CNT[23:16] → COMP8 A[7:0] EQ; L1AN[23:16] → B[7:0]

INL1ERR, COMP_EV0, COMP_EV1 → OR3B2 → L1A_MISMATCH → FD D Q, CLK C → L1AMISMATCH+1

Valid E-Code detected

FEND0, FEND1 → SOP4; GOLDDAT → DMB_END → FDC D Q, CLK C, RST CLR → DMB_END+1

DMB_END+1 = DMBEND = Ecode

DOFW+2, GOLDDAT, END_L1ERR, GOLDDAT → SOP4; L1A_MISMATCH → OR2 → GOOD_L1A

FDCE: D Q, CE, CLK C, RST_BOE CLR → L0_L1ERR → OR2 (END_L1ERR) → L1A_ERROR

(exclude DMB_Err case?)

^^^From DMB_Trail

LFOK[3:0] → OR4_BUS → SOME_FIBERS_OK → INV → NO_LIVE_FIBERS

DAT[71:0] → DAT[11:0] BUF12 L1AN[11:0]; DAT[29:18] BUF12 L1AN[23:12]; L1AN[23:0]; L1AN[15:0], L1AN[23:16]

DAT[12:0] BUF13 DOUT[12:0]

DAT[30:18] BUF13 DOUT[25:13]

DAT[48:36] BUF13 DOUT[38:26]

DAT[66:54] BUF13 DOUT[51:39]

DOUT[51:0] 4 * 13-bit SCA data bus

Use NEW DMB logic here (old L1AN was [51:40] & [31:20])

GND, DCNT[3:0], DMBCNT[3:0] → ADD4_BUS (CI, A[3:0], B[3:0] → S[3:0], CO, OFL) → DMCNT[3:0]

FD4CE: D[3:0], LOADFDAV, CE, CLK C, CLR, RST_EOE → Q[3:0] → DMBCNT[3:0]

FOE_REN[3:0] → FOE_REN2, FOE_REN3, FOE_REN1 → OR2, OR2 → FOE_B1, FOE_B0

DAQ_WAIT, LEXT_STOP, RST → OR2B1 → SET_LFIFO_EMPTY TIG

INMT[3:0]

WCGE2F[3:0], M4E_BUS D[3:0], FOE_B0 S0, FOE_B1 S1, VCC E → O FIFO_EMPTY TIG

FDS: D S Q, CLK C → LFIFO_EMPTY TIG synched w/DoFW+1,2

DMBLIVE_ERR, LINFERR, FIFO_CHG → OR3 → FIBER_ERR

EMPTYF[3:0] → OR4_BUS → ONE_NOT_MT TIG

FIFO_RDY

WCGE2F[3:0], INMT[3:0], MTIN[3:0], IN_RDY, PAFIN[3:0], FFIN[3:0], FIBEROK[3:0], START_TIMEOUT, END_TIMEOUT, RST, CLK

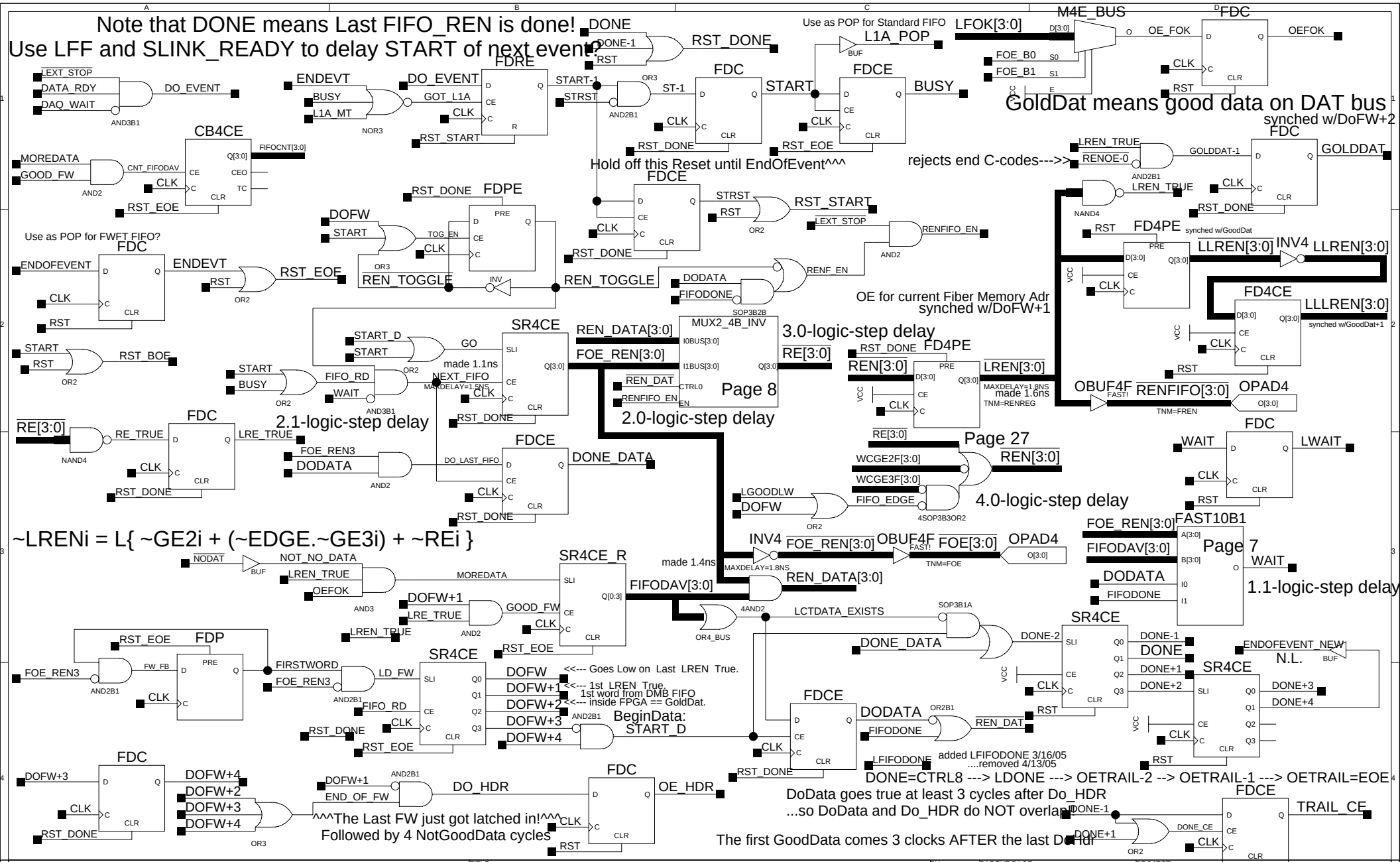
FDCE: SYS_RDY, CLK, RST → D Q, CE, CLR → IN_RDY

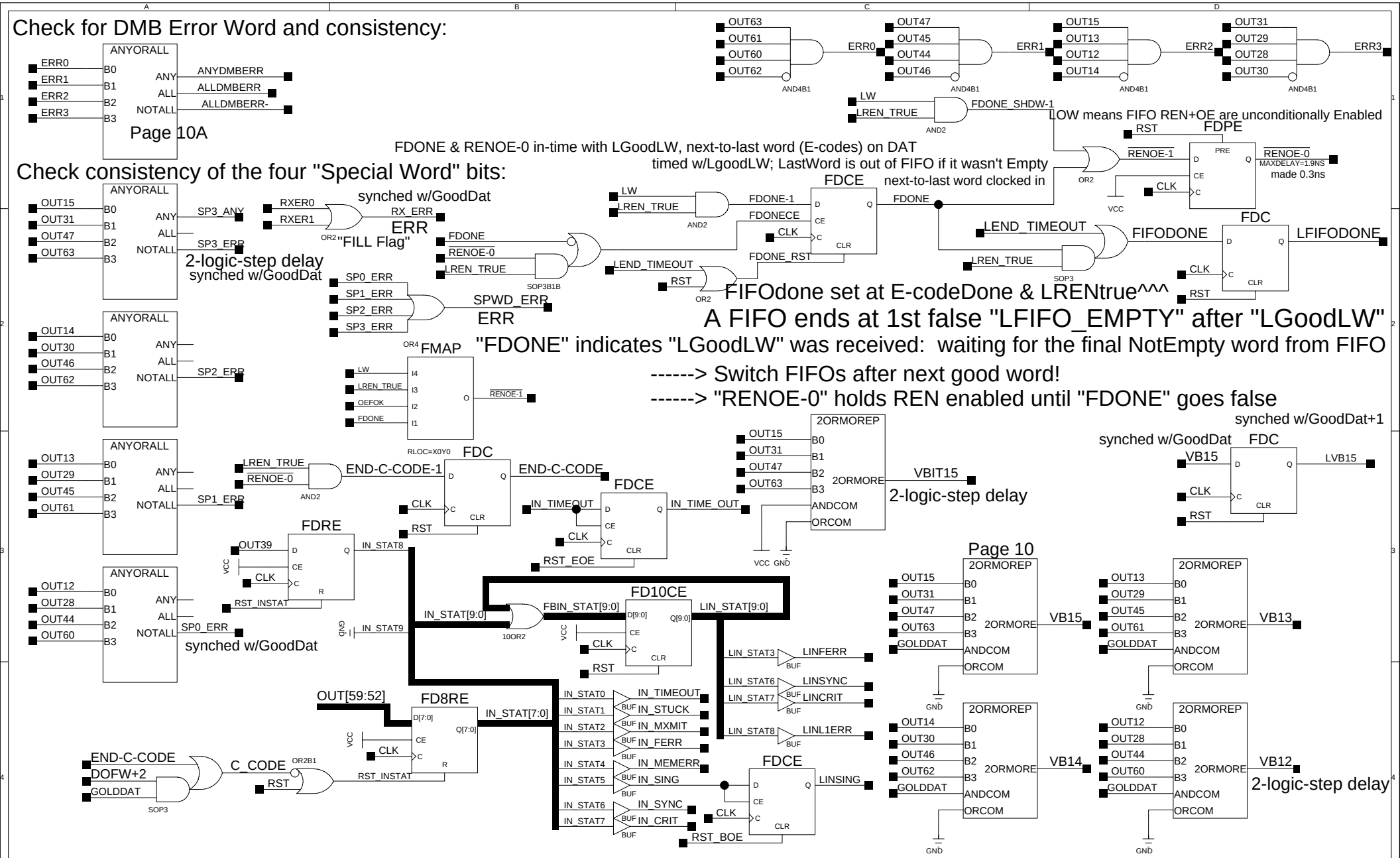
Page 4

EMPTY[3:0], DATA_READY, NOT_READY, ONE_RDY, RDY[3:0], NOTRDY[3:0], LFOK[3:0], MT[3:0], FERR[3:0], FPAF[3:0], FFUL[3:0], PAF_ERROR, FF_ERROR, FIBER_CHANGE

EMPTYF[3:0], DATA_RDY, NOT_RDY, ONE_RDY, RDY[3:0] N.L., NRDY[3:0], LFOK[3:0], MT[3:0], F_ERR[3:0], FPAF[3:0], FFULL[3:0], PAF_ERR, FFERR, FIFO_CHG

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2
		DATE: 9-19-2005_9:55	PROJECT: D785C
		FILE: FIFOCTRL . 1	PAGE: 3

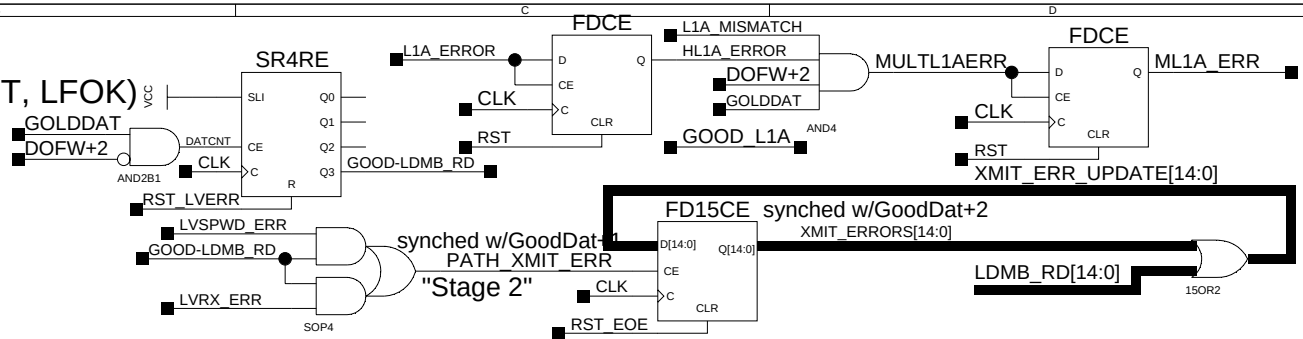

Note that DONE means Last FIFO_REN is done!
Use LFF and SLINK_READY to delay START of next event?
GoldDat means good data on DAT bus
Hold off this Reset until EndOfEvent^^^
rejects end C-codes--->>
Use as POP for FWFT FIFO?
Use as POP for Standard FIFO
OE for current Fiber Memory Adr
synched w/DoFW+2
synched w/DoFW+1
synched w/GoodDat
synched w/GoodDat+1
3.0-logic-step delay
2.0-logic-step delay
2.1-logic-step delay
4.0-logic-step delay
1.1-logic-step delay
Page 8
Page 27
Page 7
~LRENi = L{ ~GE2i + (~EDGE.~GE3i) + ~REi }
<<--- Goes Low on Last LREN True.
<<--- 1st LREN True.
1st word from DMB FIFO
<<--- inside FPGA == GoldDat.
BeginData:
^^^The Last FW just got latched in!^^^
Followed by 4 NotGoodData cycles
DONE=CTRL8 ---> LDONE ---> OETRAIL-2 --> OETRAIL-1 ---> OETRAIL=EOE
DoData goes true at least 3 cycles after Do_HDR
...so DoData and Do_HDR do NOT overlap
The first GoodData comes 3 clocks AFTER the last Do_Hdr
added LFIFODONE 3/16/05
....removed 4/13/05
made 1.1ns
made 1.6ns
made 1.4ns
N.L.
EXT_STOP
DATA_RDY
DAQ_WAIT
AND3B1
DO_EVENT
ENDEVT
BUSY
L1A_MT
NOR3
GOT_L1A
RST_START
FDRE
START-1
STRST
AND2B1
ST-1
START
BUSY
RST_DONE
RST_EOE
L1A_POP
BUF
LFOK[3:0]
FOE_B0
FOE_B1
M4E_BUS
OE_FOK
OEFOK
FDC
FDCE
CB4CE
MOREDATA
GOOD_FW
CNT_FIFODAV
FIFOCNT[3:0]
AND2
RST_EOE
FDPE
DOFW
TOG_EN
REN_TOGGLE
INV
OR3
STRST
RST_START
LEXT_STOP
RENFIFO_EN
RENF_EN
DODATA
FIFODONE
SOP3B2B
LREN_TRUE
RENOE-0
GOLDDAT-1
GOLDDAT
LREN_TRUE
NAND4
FD4PE
LLREN[3:0]
INV4
LLREN[3:0]
FD4CE
LLLREN[3:0]
ENDOFEVENT
RST_BOE
START_D
GO
SR4CE
REN_DATA[3:0]
FOE_REN[3:0]
MUX2_4B_INV
I0BUS[3:0]
I1BUS[3:0]
CTRL0
EN
REN_DAT
RENFIFO_EN
RE[3:0]
FIFO_RD
WAIT
NEXT_FIFO
MAXDELAY=1.5NS
RST_DONE
REN[3:0]
LREN[3:0]
MAXDELAY=1.8NS
TNM=RENREG
OBUF4F
FAST!
RENFIFO[3:0]
OPAD4
TNM=FREN
RE_TRUE
LRE_TRUE
NAND4
FOE_REN3
DONE_DATA
DO_LAST_FIFO
WCGE2F[3:0]
WCGE3F[3:0]
FIFO_EDGE
4SOP3B3OR2
LGOODLW
DOFW
OR2
WAIT
LWAIT
FAST10B1
FIFODAV[3:0]
NODAT
NOT_NO_DATA
LREN_TRUE
OEFOK
AND3
MOREDATA
SR4CE_R
DOFW+1
GOOD_FW
LRE_TRUE
AND2
LREN_TRUE
RST_EOE
FOE_FOK[3:0]
INV4
OBUF4F
FOE[3:0]
OPAD4
TNM=FOE
REN_DATA[3:0]
4AND2
OR4_BUS
LCTDATA_EXISTS
SOP3B1A
DONE_DATA
DONE-2
DONE-1
DONE
DONE+1
DONE+2
DONE+3
DONE+4
ENDOFEVENT_NEW
BUF
FDP
FW_FB
FIRSTWORD
LD_FW
FIFO_RD
DOFW
DOFW+1
DOFW+2
DOFW+3
DOFW+4
DODATA
FIFODONE
OR2B1
REN_DAT
LFIFODONE
DOFW+3
DOFW+4
DOFW+2
DOFW+3
DOFW+4
OR3
DOFW+1
END_OF_FW
DO_HDR
OE_HDR
DONE-1
DONE+1
DONE_CE
TRAIL_CE
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
Read Control
DDU Input Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
2
PROJECT
D785C
DATE
9-13-2005_11:32
FILE
FIFOCTRL . 2
PAGE
3A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 9-13-2005_11:36	PROJECT: D785C FILE: FIFOCTRL . 3 PAGE: 3B

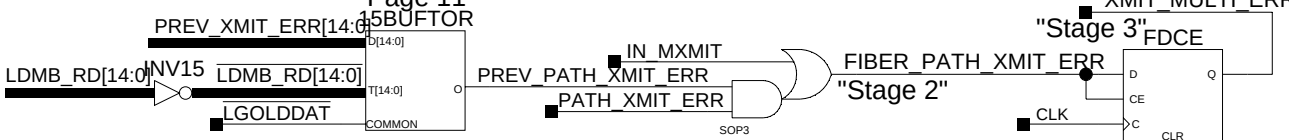
Control Bit List:

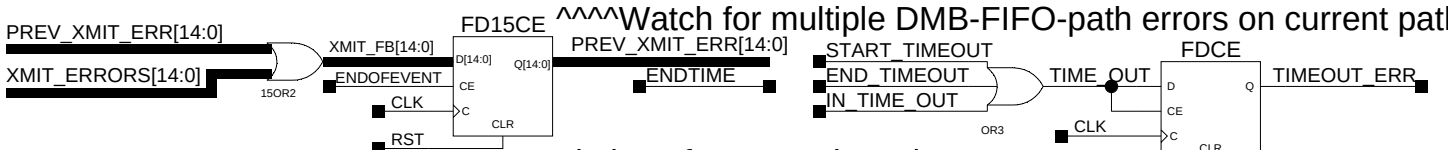
0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE--->OETrail)



^^^^Event accumulation of valid DMB-path-Xmit errors^^^^

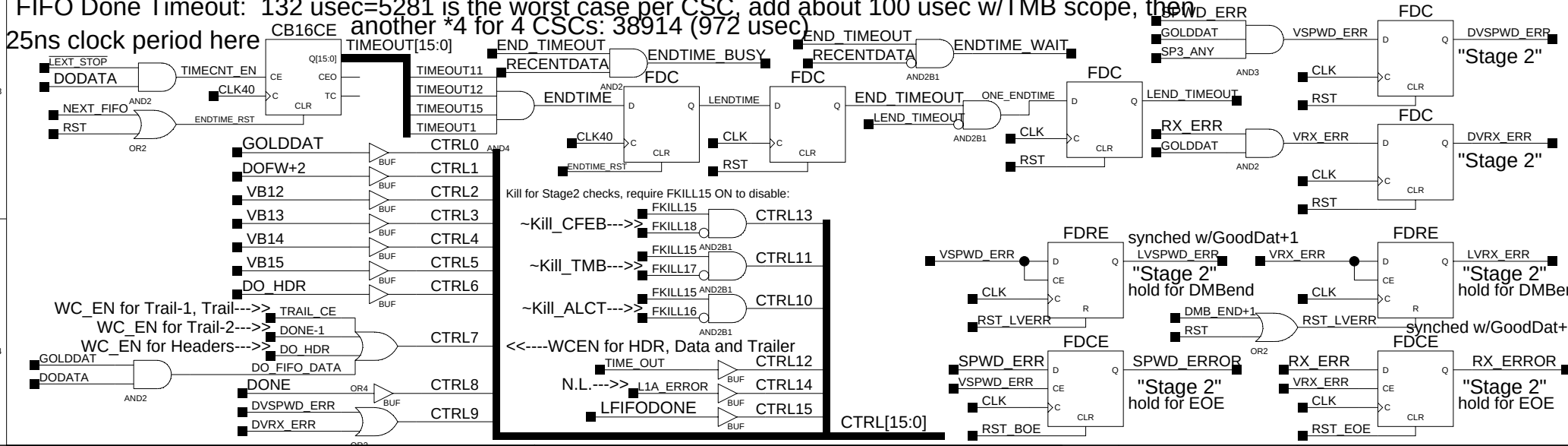
Page 11





FIFO Done Timeout: 132 usec=5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another *4 for 4 CSCs: 38914 (972 usec)

25ns clock period here



THE OHIO STATE UNIVERSITY
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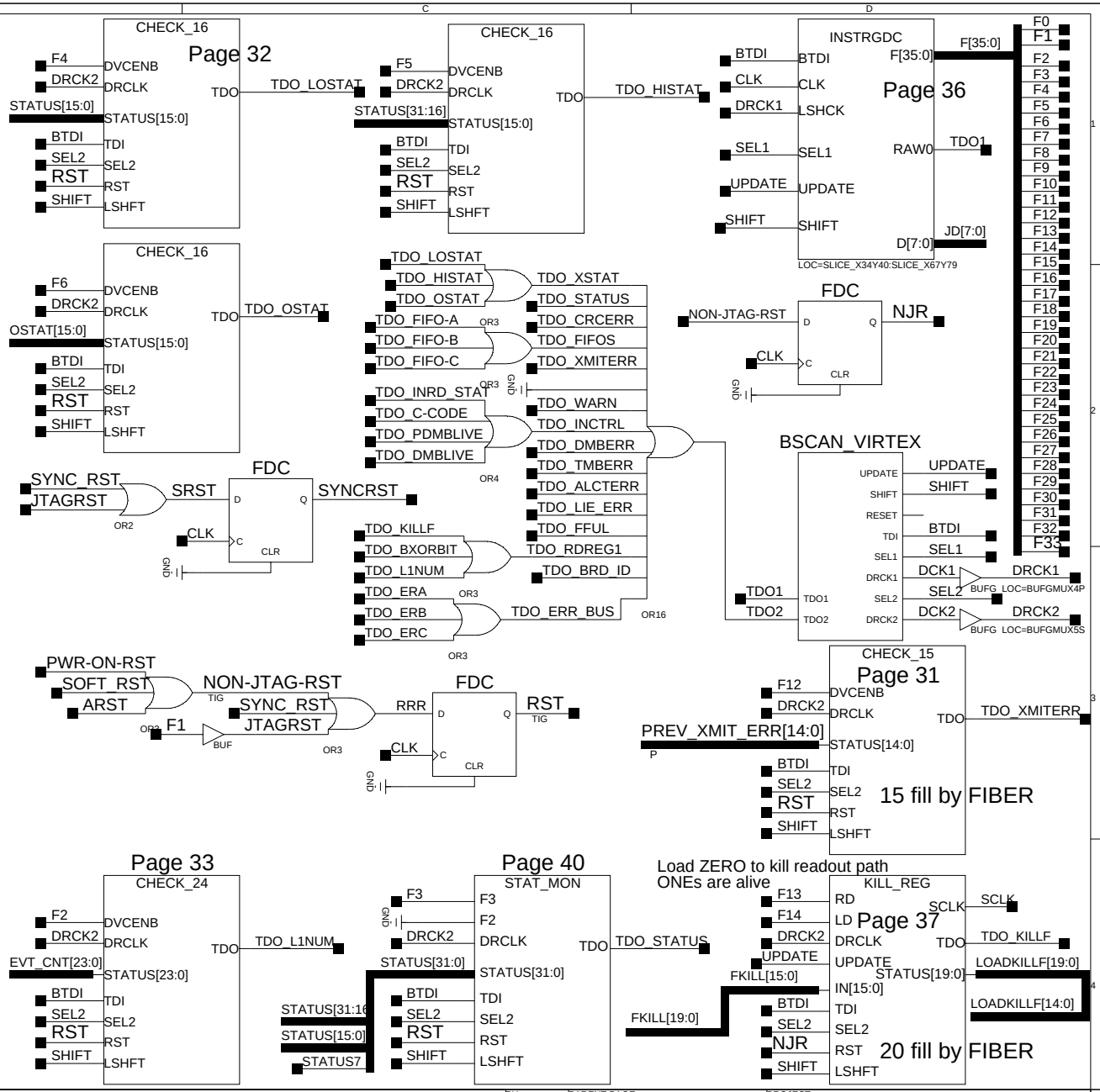
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU Input FIFO Control
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 9-13-2005_13:57 | FILE: FIFOCTRL . 4 | PAGE: 3C

JTAG Instruction Decode

OpCode	Function [OpName]	
0	No Operation [NOOP]	
1	FPGA Reset [toggle]	
2	Read Current DDU L1A Number (24-bit scaler)	
3	Check status (capture and shift) [32 bits]	
4	Check status, low-word [16 bits]	
5	Check status, high-word [16 bits]	
6	Output Path Status [16-bits]	
7a	Check FOK (active input FIFOs) [lowest 4 bits]	
7b	L1A Mismatch (FIFO headers) [4-bits]	check FIFO-A
7c	Check FIFO Err (active FIFO change) [4 bits]	
7d	Stuck Data Errors (input FIFOs) [highest 4-bits]	
8a	Almost Full FIFOs [lowest 10-bits]	check FIFO-B
8b	FIFO Empty/GE2 Status [highest 6-bits]	
9a	Full FIFOs [lowest 10-bits]	FIFO Full/MT (raw)
* 9b	Raw FIFO Empty [highest 6-bits]	
10	CRC Errors [15-bits]	
11a	Lost In Data [lowest 4-bits]	check FIFO-C
11b	Timeout: start [4-bits]	
11c	Timeout: end-wait [4-bits]	
11d	Timeout: end-active [highest 4-bits]	
12	Data Xmit Errors [15-bits]	
13	Check KILL_Register [20 bits]	
14	Load KILL_Register [20 bits]	
15	DMB Errors [15-bits]	
16	TMB Errors [15-bits]	
17	ALCT Errors [15-bits]	
18	Lost In Event [15-bits]	
* 19	InRD Status [16-bits]	free: 21, 28
* 20	InRD C-code & MxmitErr History [16-bits]	
22	Error Register A [16-bits]	
23	Error Register B [16-bits]	
24	Error Register C [16-bits]	
25	Read DMB_LIVE [15-bits]	
26	Read P_DMB_LIVE [15-bits]	
27	Read WARN_MON [16-bits]	
29	Set BX per Orbit [12-bits]	
30	Read BX per Orbit [12-bits]	
31	Toggle CFEB_Cal Auto_L1 [default enable]	
32	Read DDU Board ID [16-bits]	
33	DDU-only VME_L1A	



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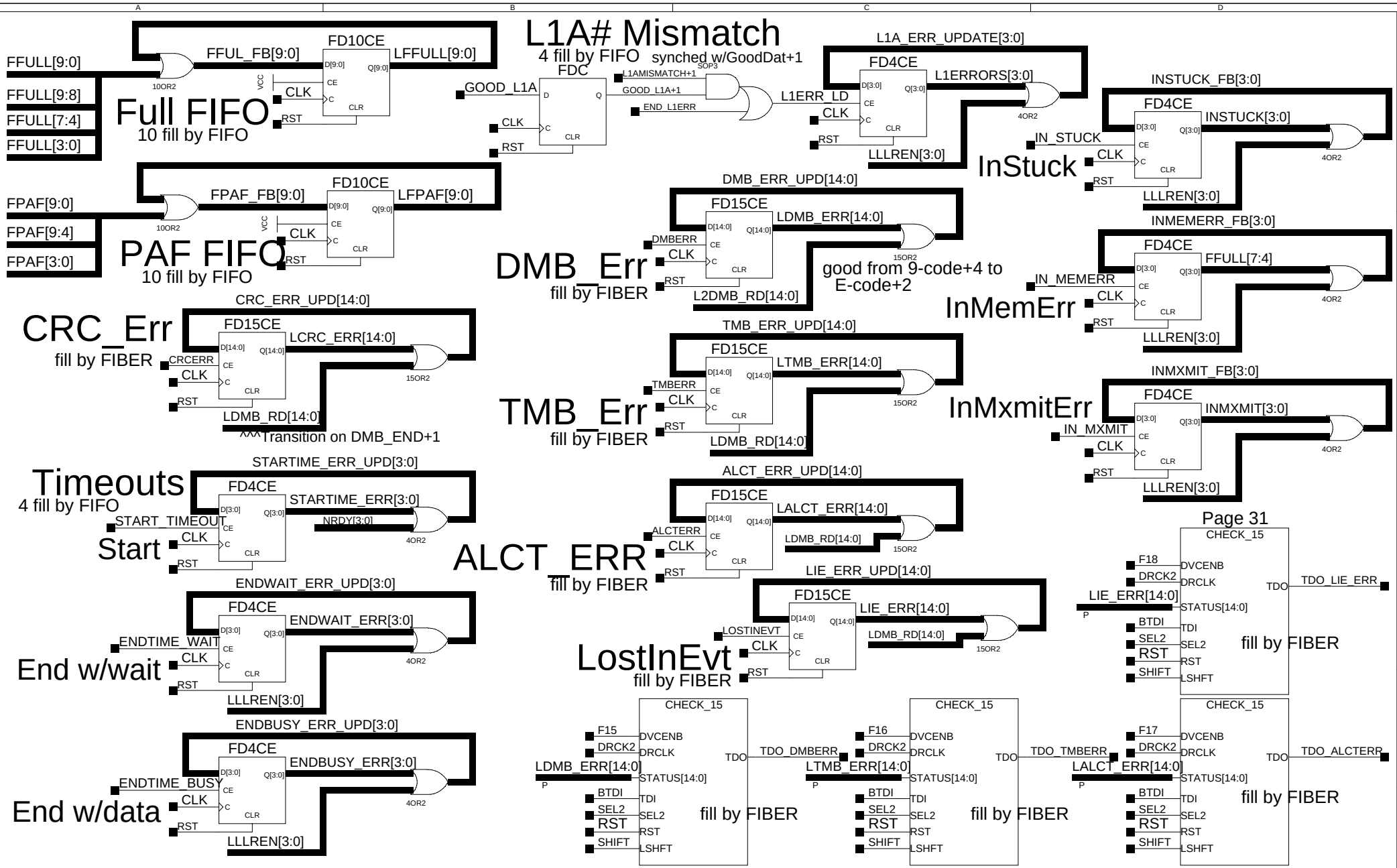
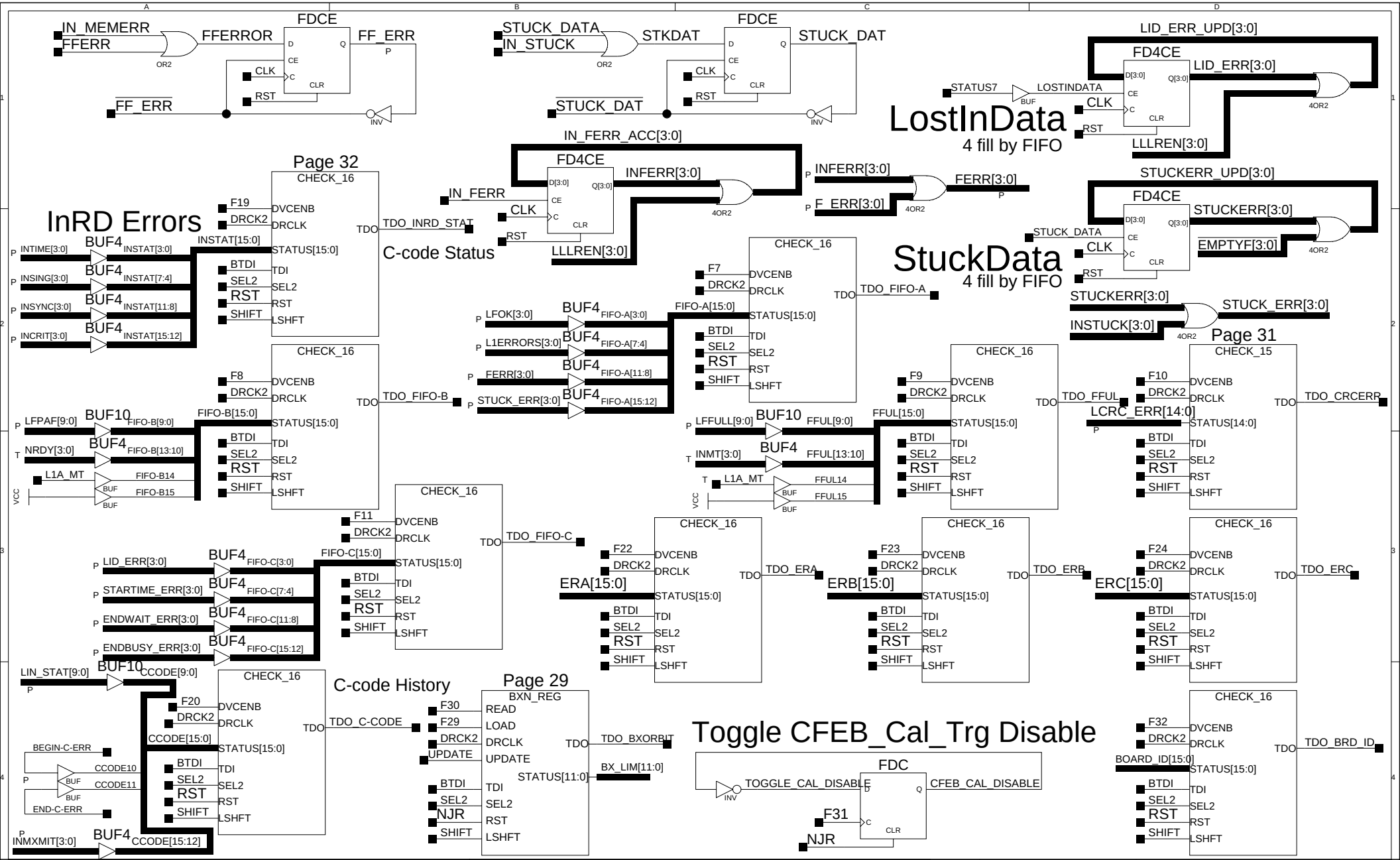
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: JTAG Signals
DDU Controller
CMS CSC Electronics

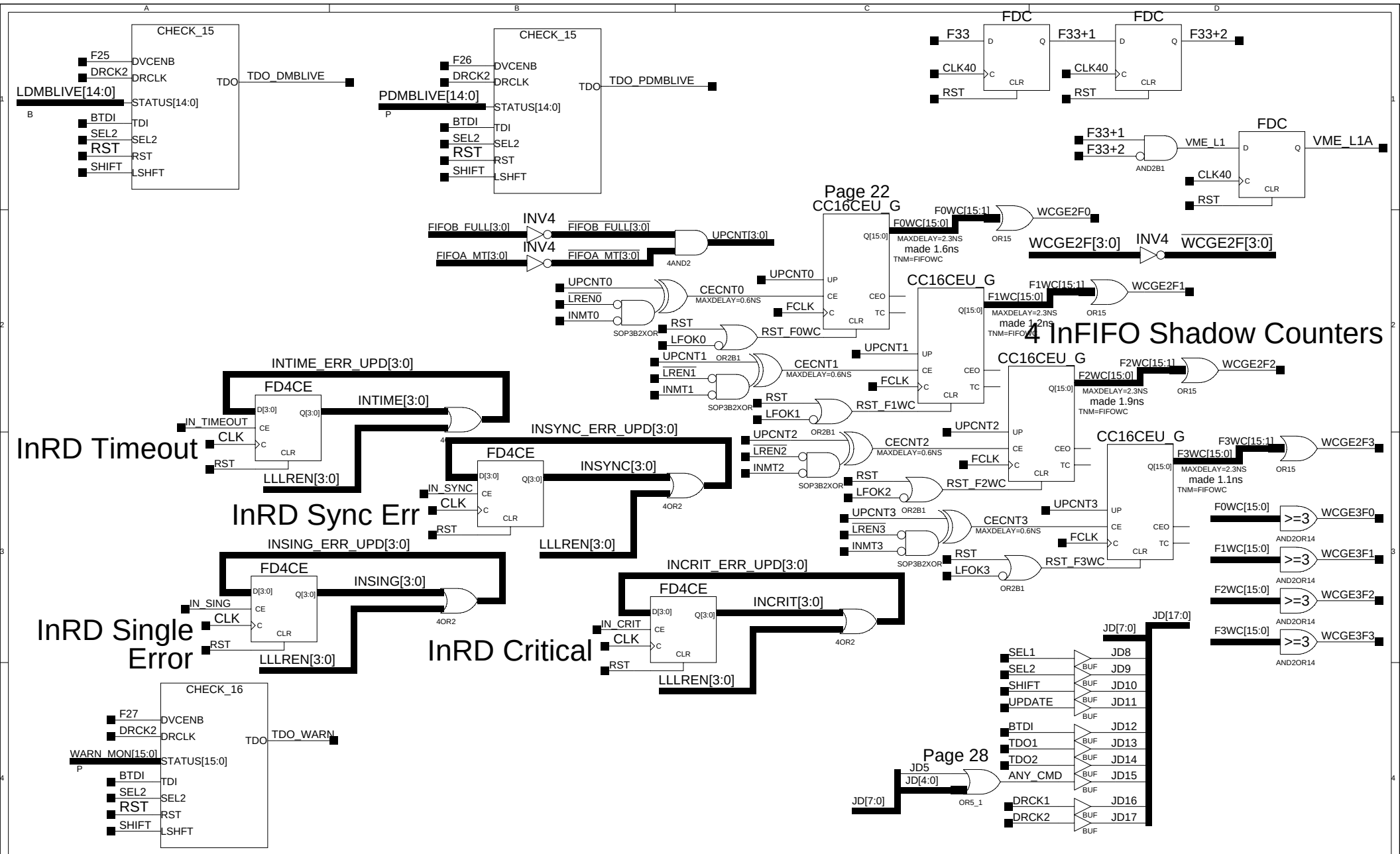
BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 9-13-2005_15:01 | FILE: FIFOCTRL . 5 | PAGE: 3D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 9-13-2005_15:01	PARENT PAGE: 2 PROJECT: D785C FILE: FIFOCTRL . 6 PAGE: 3E

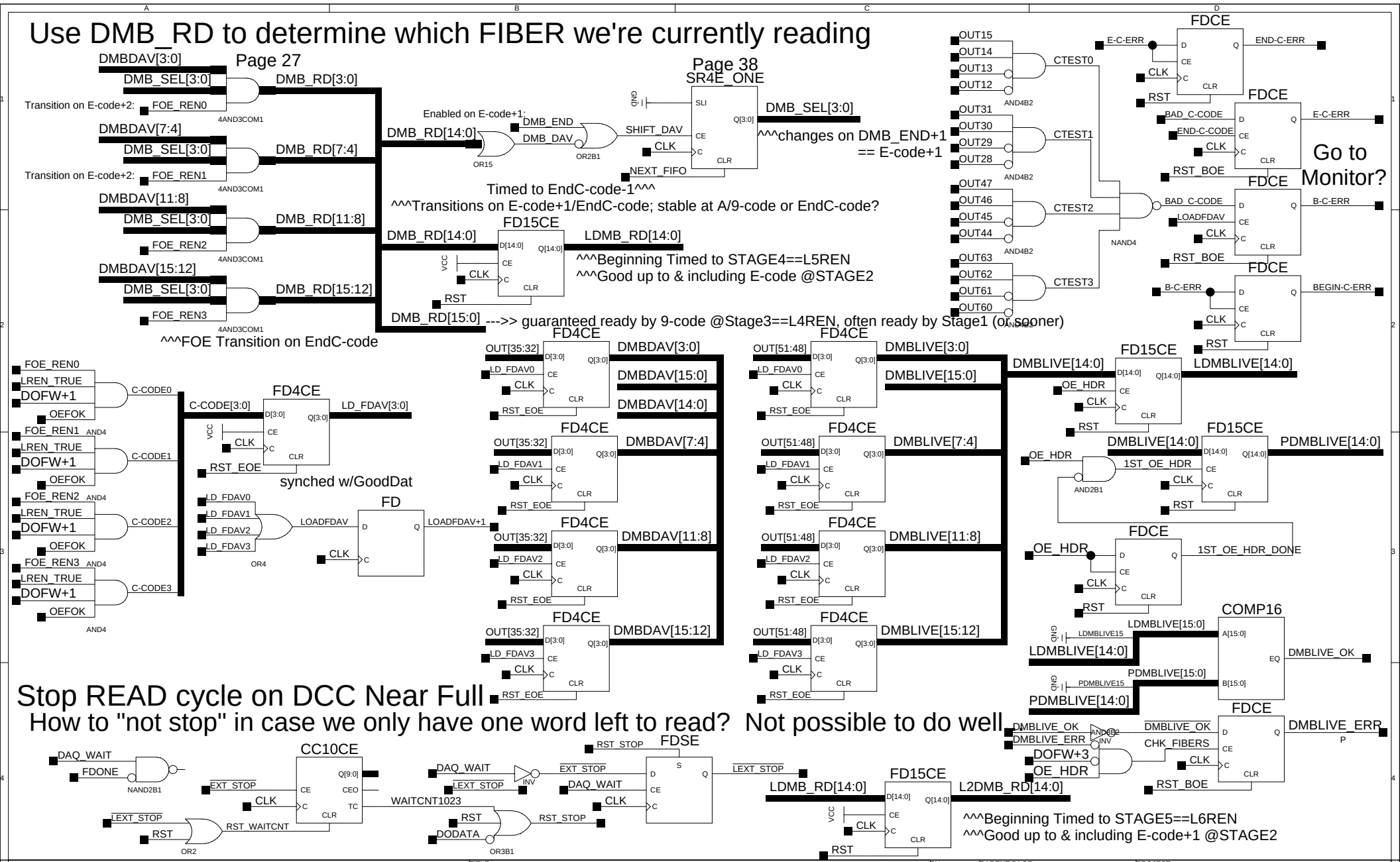


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
		DATE 9-19-2005_9:55	FILE FIFOCTRL . 7	PAGE 3F



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 9-13-2005_15:03	PARENT PAGE: 2 FILE: FIFOCTRL . 8	PROJECT: D785C PAGE: 3G

Use DMB_RD to determine which FIBER we're currently reading



Stop READ cycle on DCC Near Full

How to "not stop" in case we only have one word left to read? Not possible to do well

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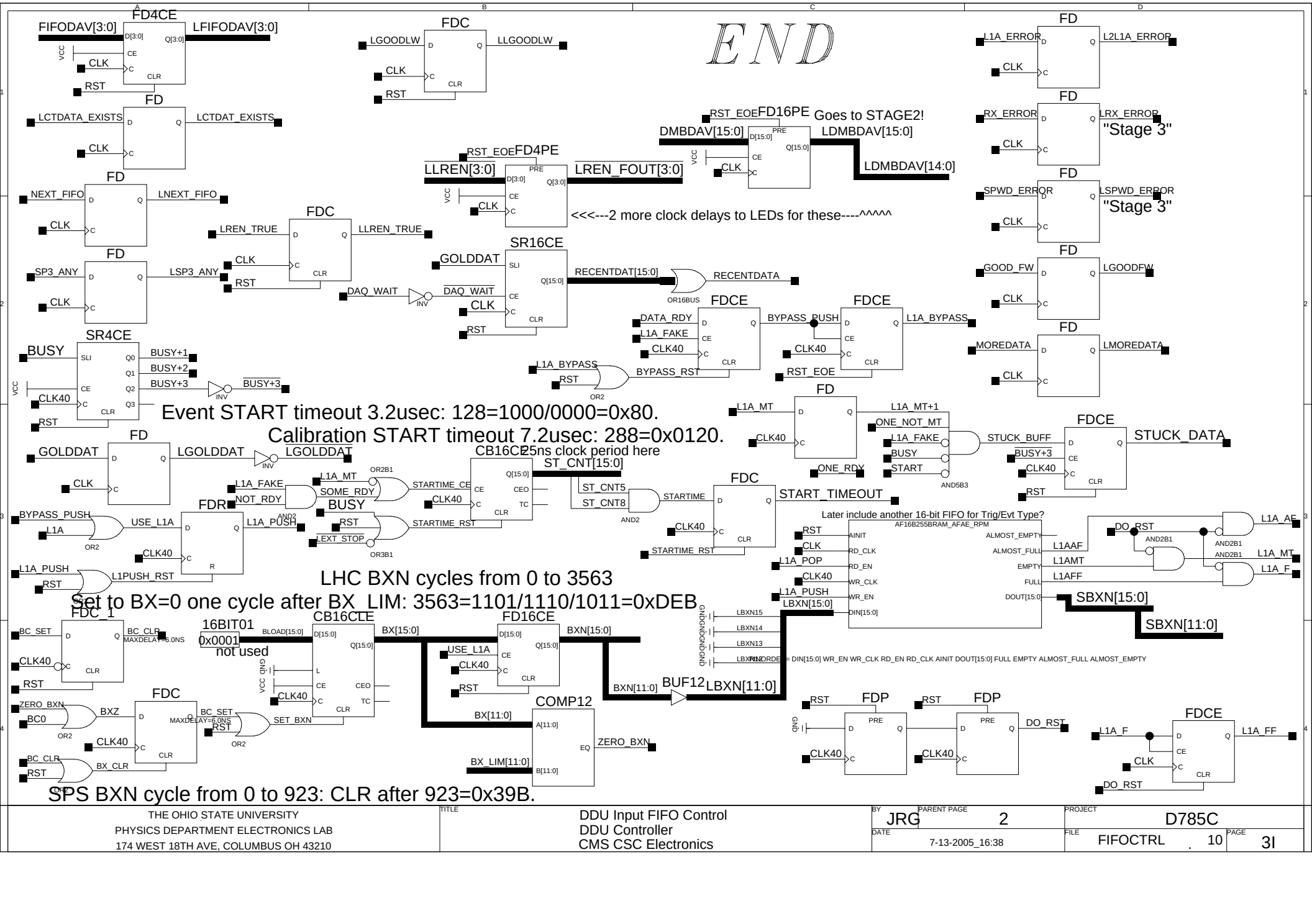
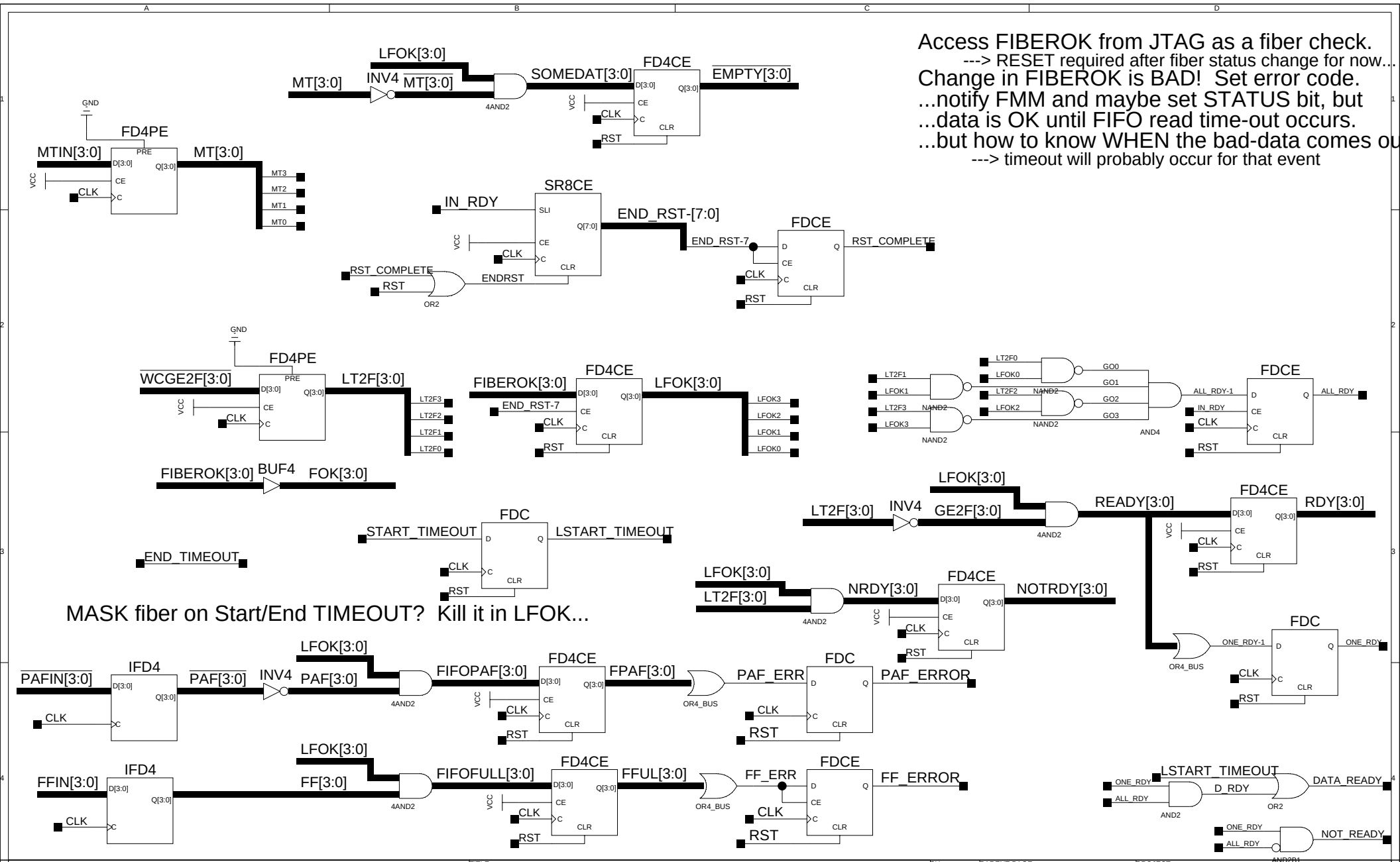
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU Input FIFO Control
DDU Controller
CMS CSC Electronics

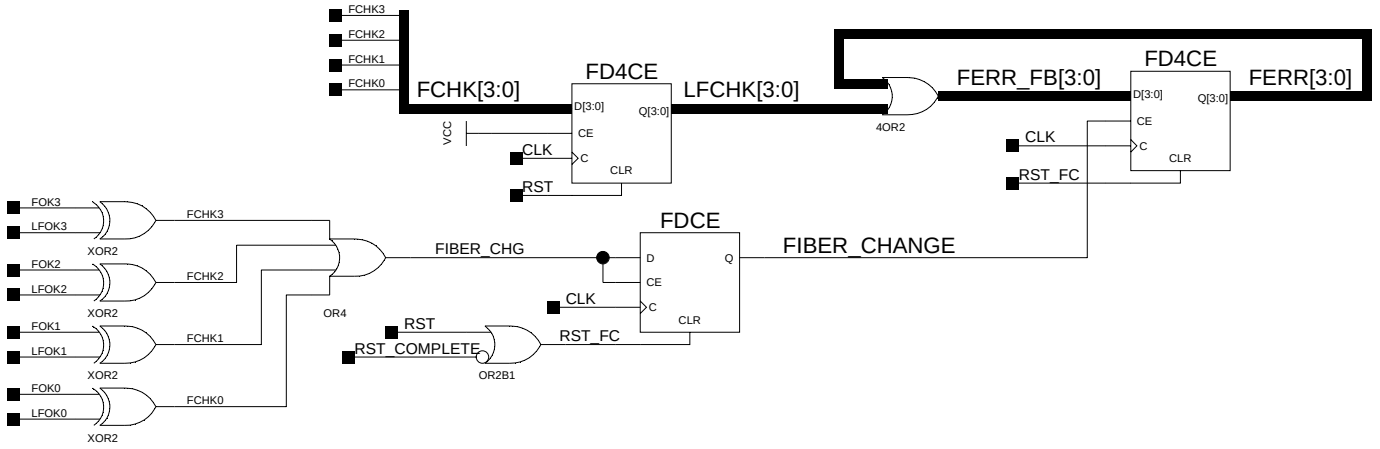
BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 9-13-2005_15:03 | FILE: FIFOCTRL . 9 | PAGE: 3H



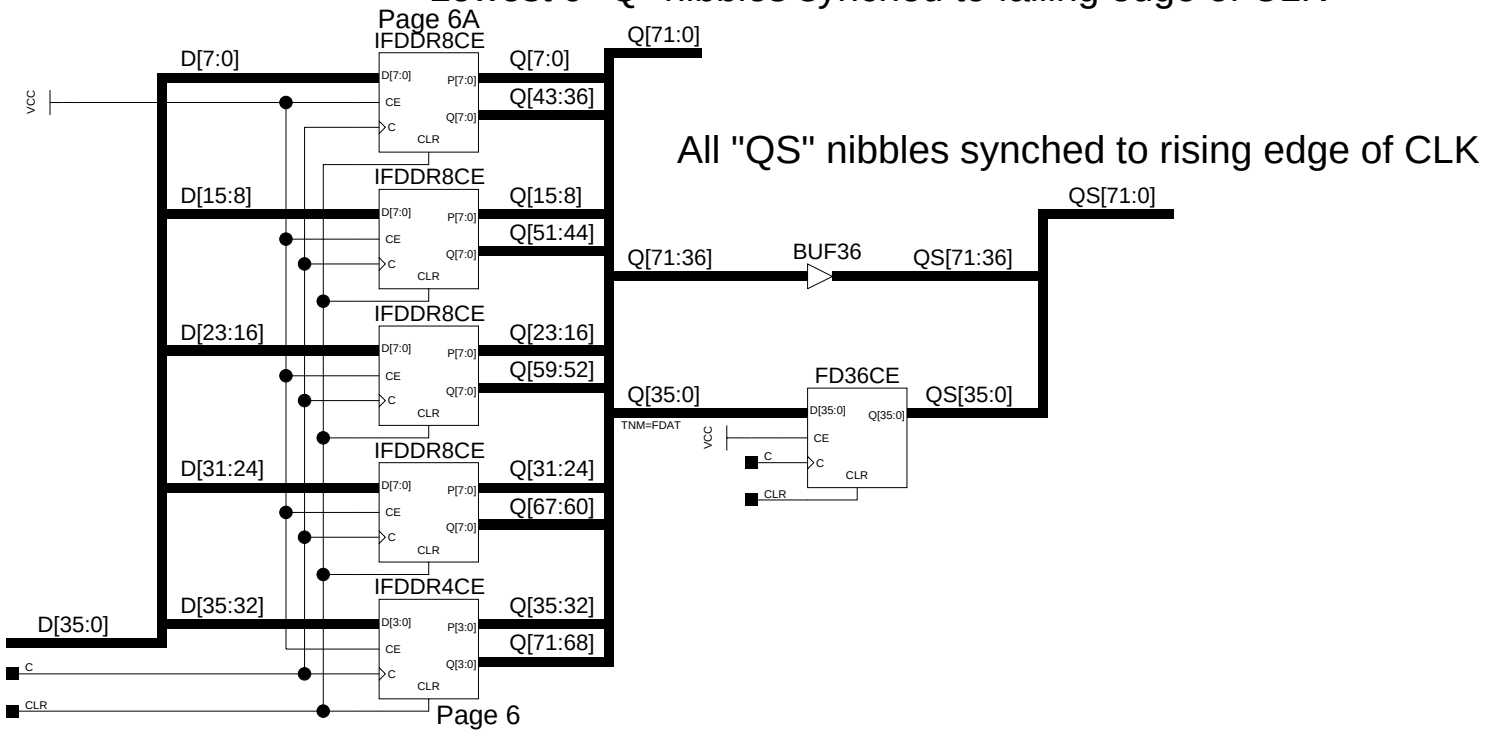
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG DATE 7-13-2005_16:38	PARENT PAGE 2	PROJECT D785C FILE FIFOCTRL . 10 PAGE 3I



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input FPGAs Available for DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 5-25-2005_13:48	FILE: FIFO_RDY . 1	PAGE: 4



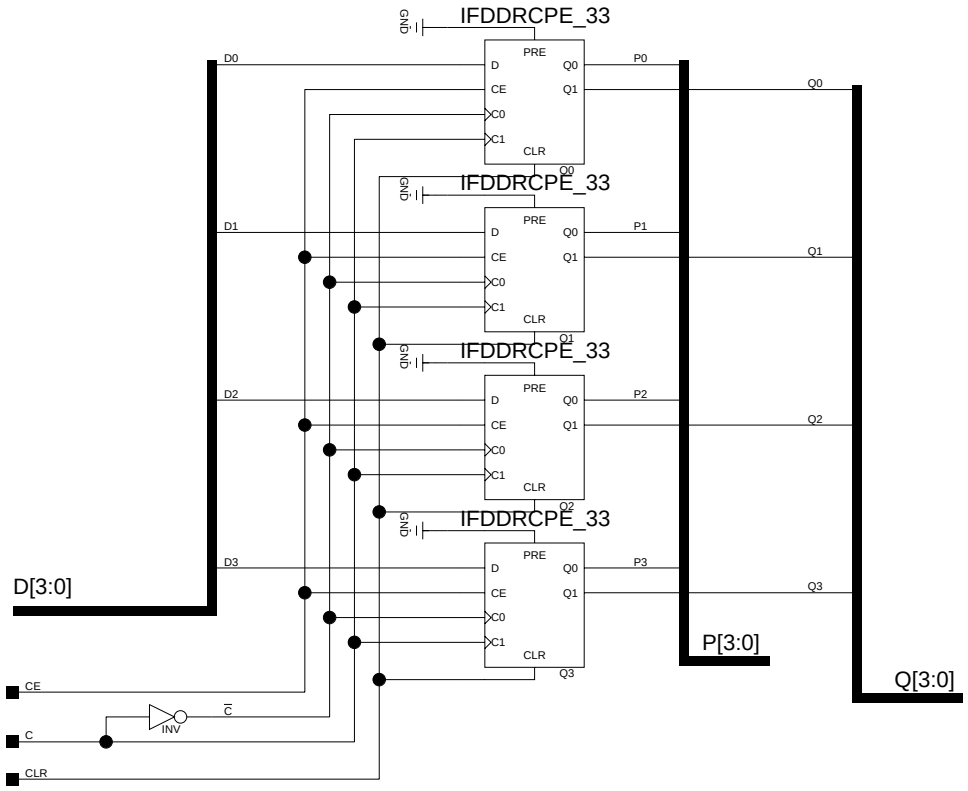
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 3-23-2005_10:32	FILE: FIFO_RDY . 2	PAGE: 4A



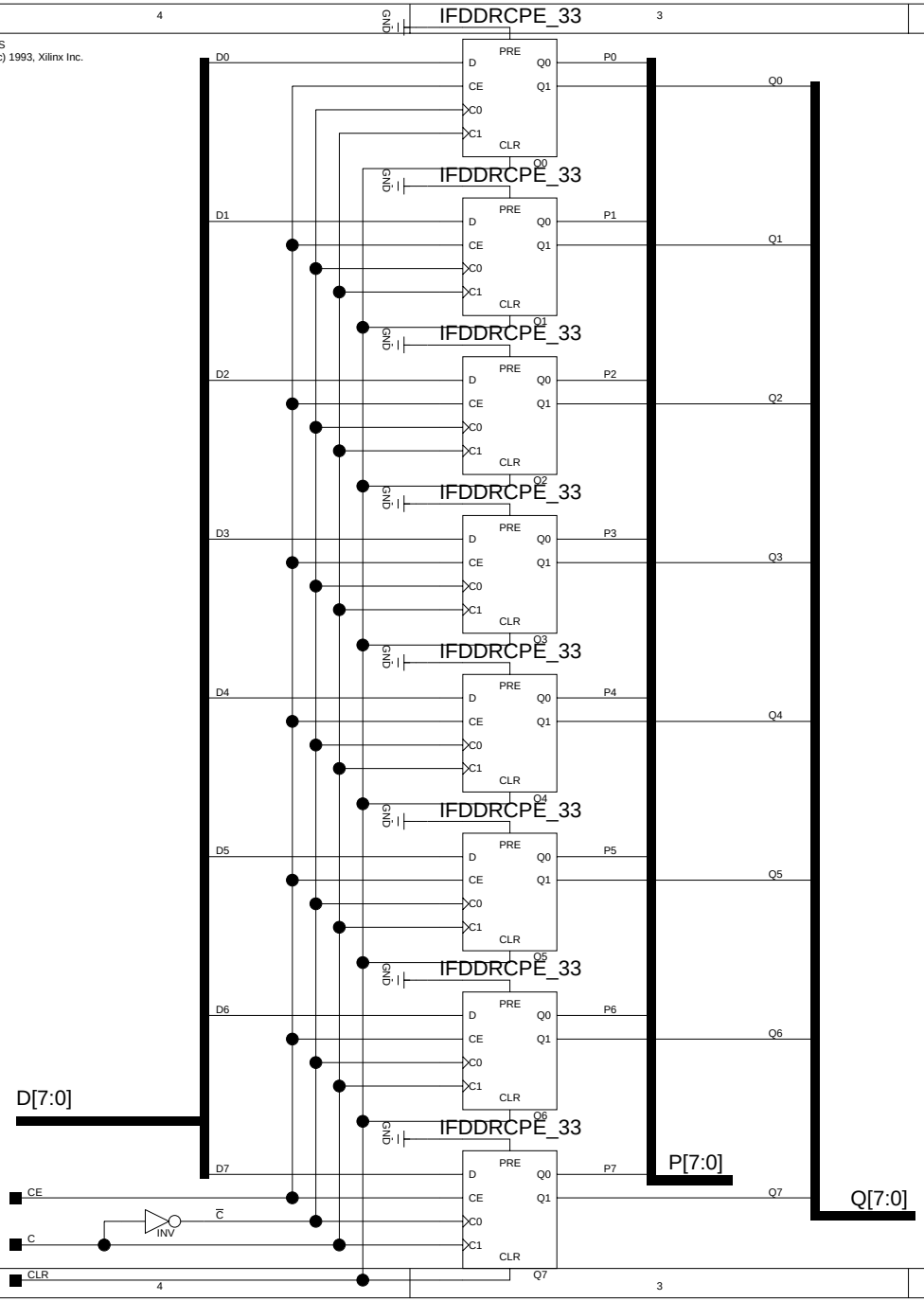
CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

XILINX			
Title:	VIRTEX Family IFDDR36C Macro, LVCMOS33		
Comments:	36-Bit DDR Input Flip-Flop with asynchronus clear	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A

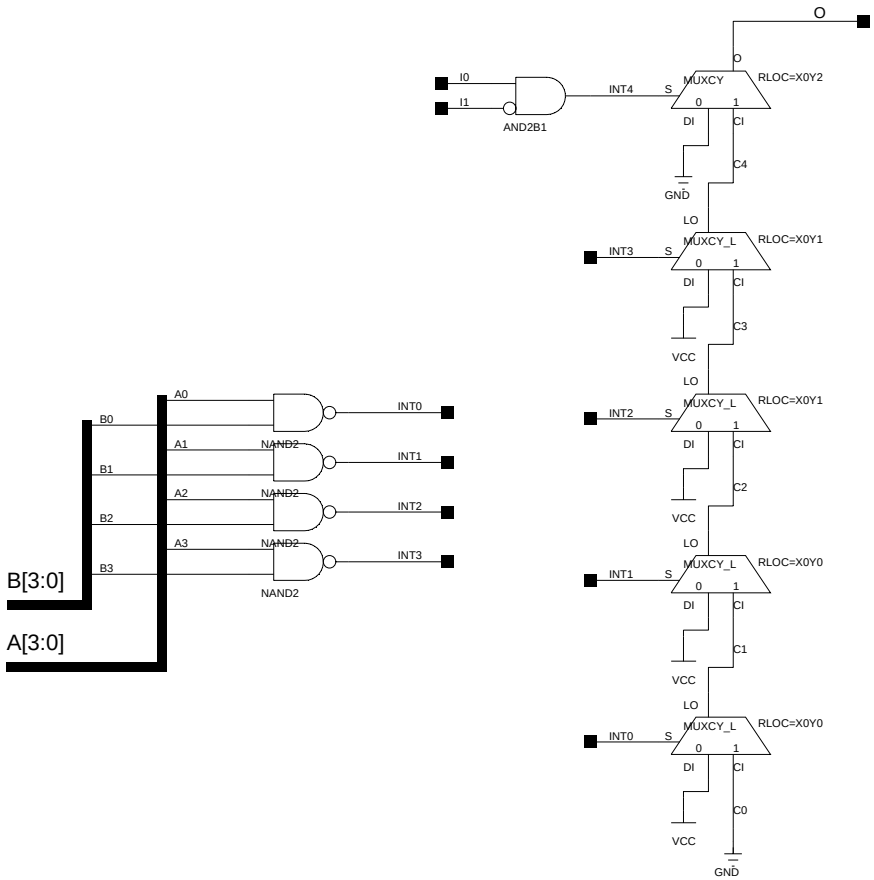
drawn by KS



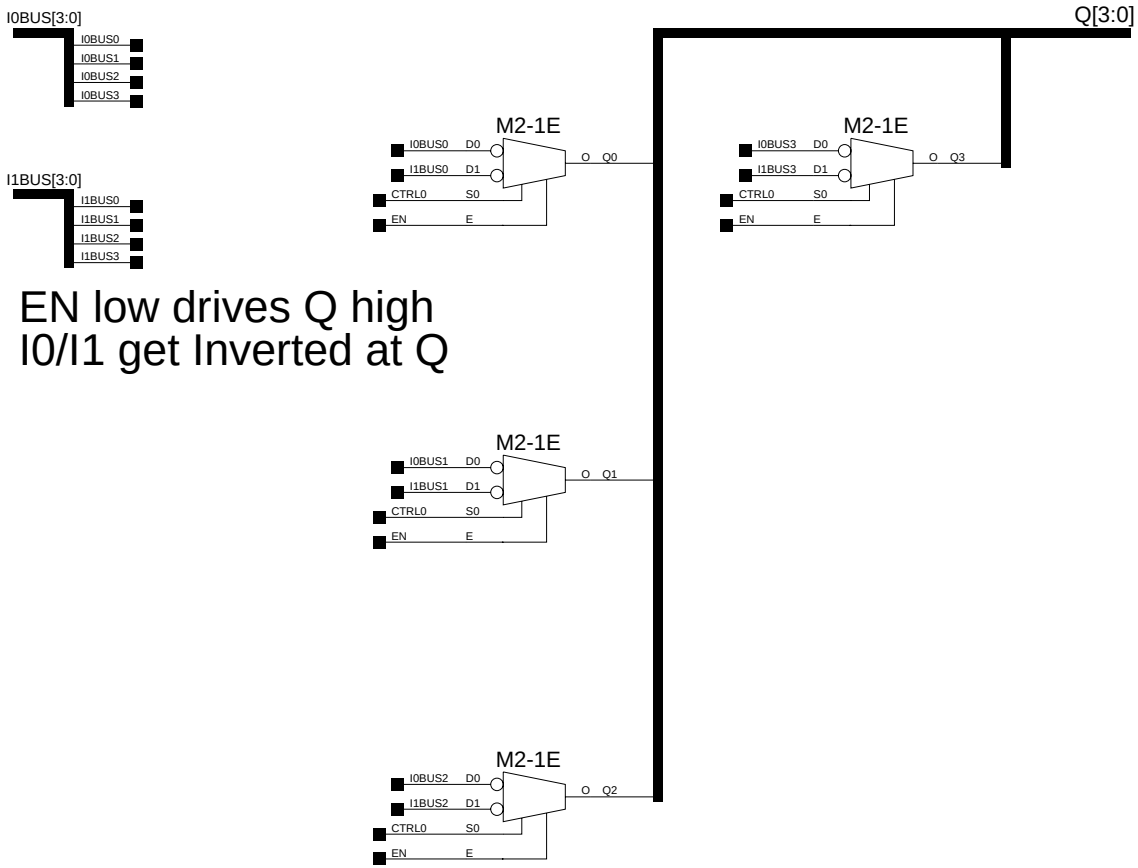
XILINX			
Title:	VIRTEX Family IFDDR4CE Macro, LVCMOS33		JRG
Comments:	4-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



XILINX			
Title:	VIRTEX Family IFDDR8CE Macro, LVCMOS33		
Comments:	8-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



XILINX			JRG
Title:	FAST10B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 .AND. AND2B1		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A



EN low drives Q high
I0/I1 get Inverted at Q

THE OHIO STATE UNIVERSITY
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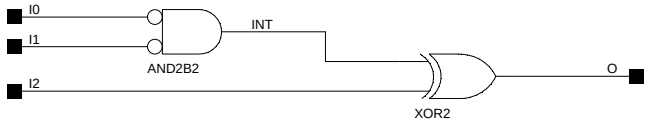
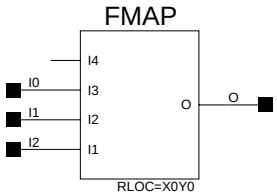
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: 4-bit MUX for 2 4-bit Inputs, w/Enable, invert selected DIN
DDU Input Controller Logic
CMS CSC Electronics

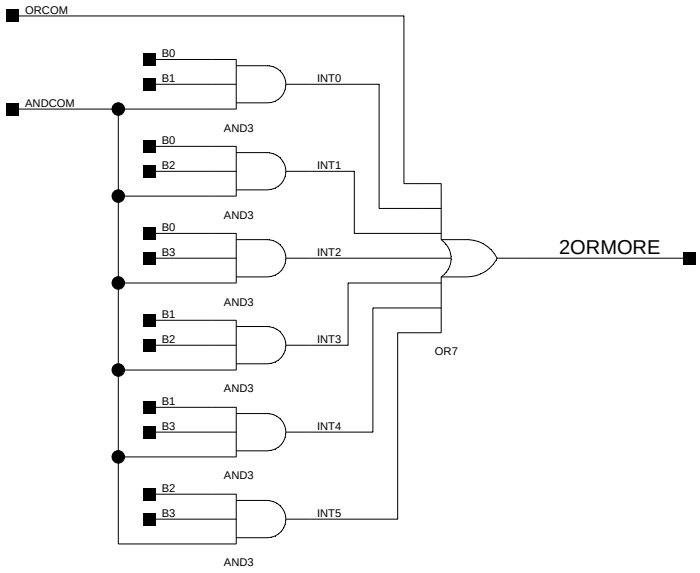
BY	PARENT PAGE	PROJECT
JRG	3	D785C
DATE		FILE / PAGE
5-24-2005_14:02		MUX2_4B_INV . 1 / 8



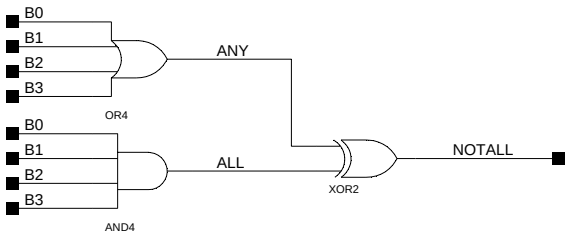


XILINX

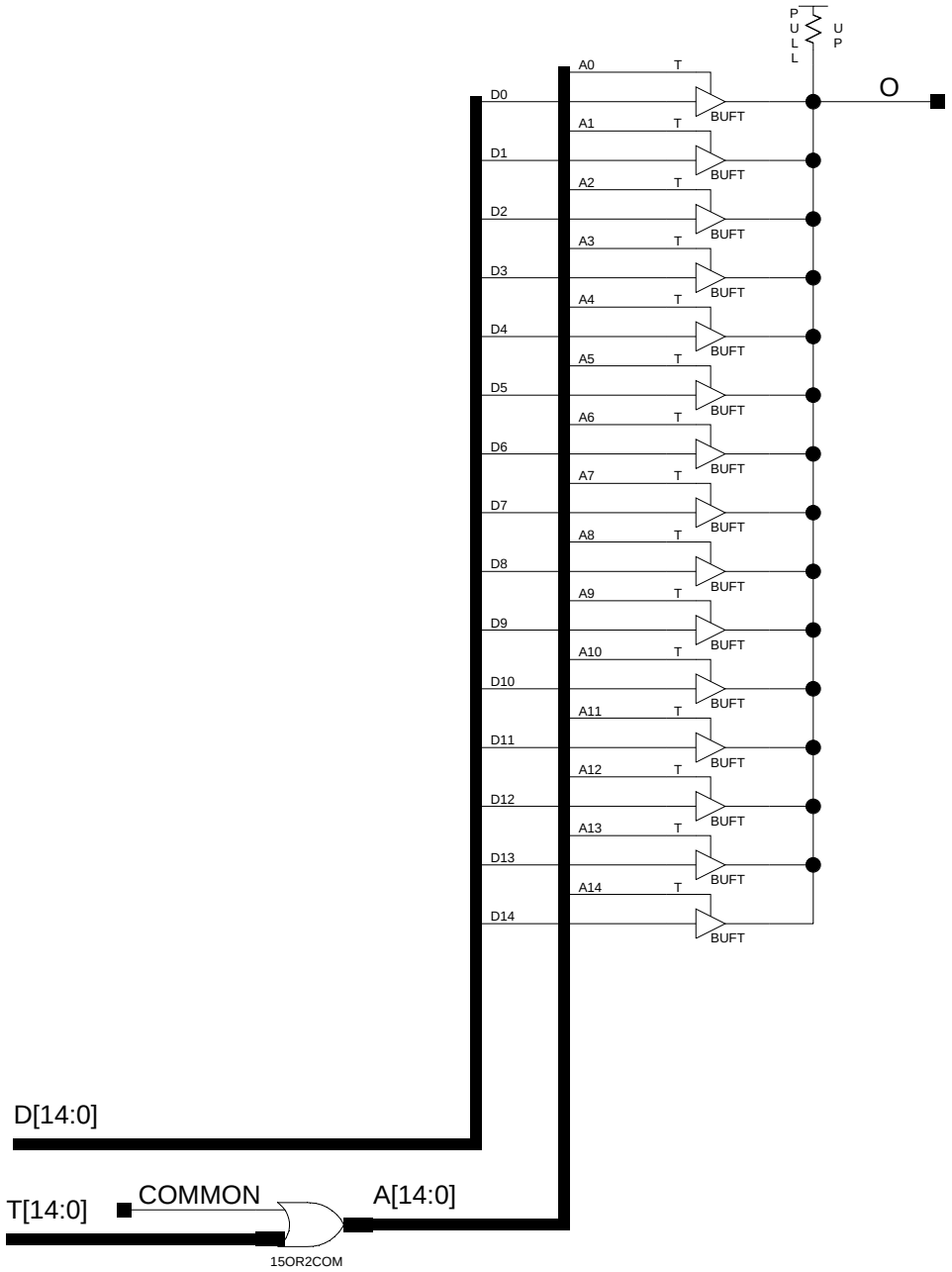
Title:	VIRTEX Family SOP3B2XOR Macro	
Comments:	SOP3B2XOR Gate	JRG
Date:	11th December 2003	Ver: 1
Sheet Size: A		Rev: A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 7-18-2005_17:01	FILE: 2ORMOREP . 1	PAGE: 10



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for ALL bits set, ANY bits set and NOTALL bits set DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_17:01	PARENT PAGE: 3 FILE: ANYORALL . 1
		PROJECT: D785C	PAGE: 10A



XILINX

Title: VIRTEX Family 15-BufTOR Macro

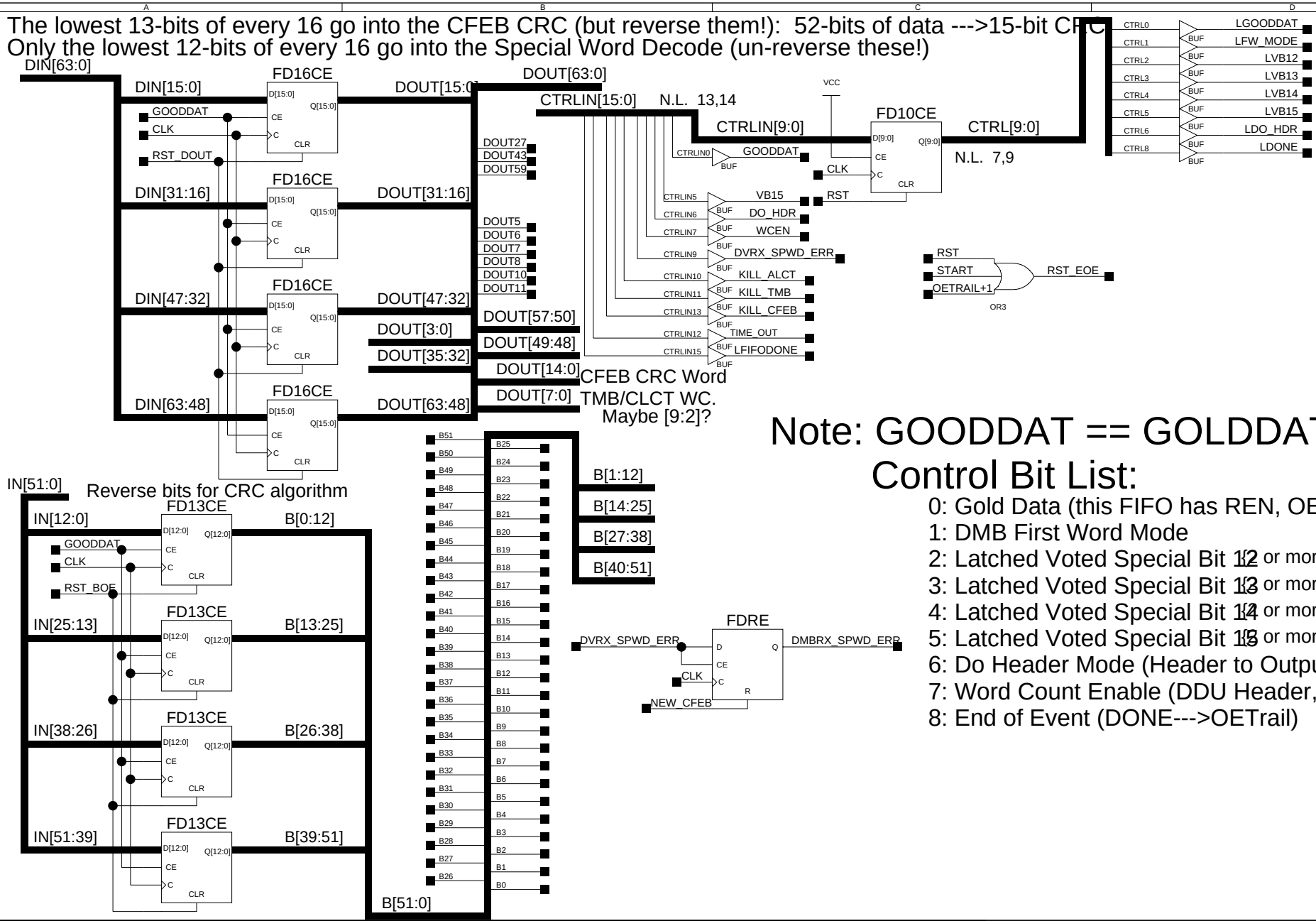
Comments:15-BufT Bus Gate with Bus-OR-Common control

JRG

Date: 27th December 2001 Ver: 1

Sheet Size: A Rev: A

drawn by KS



Note: GOODDAT == GOLDDAT here!

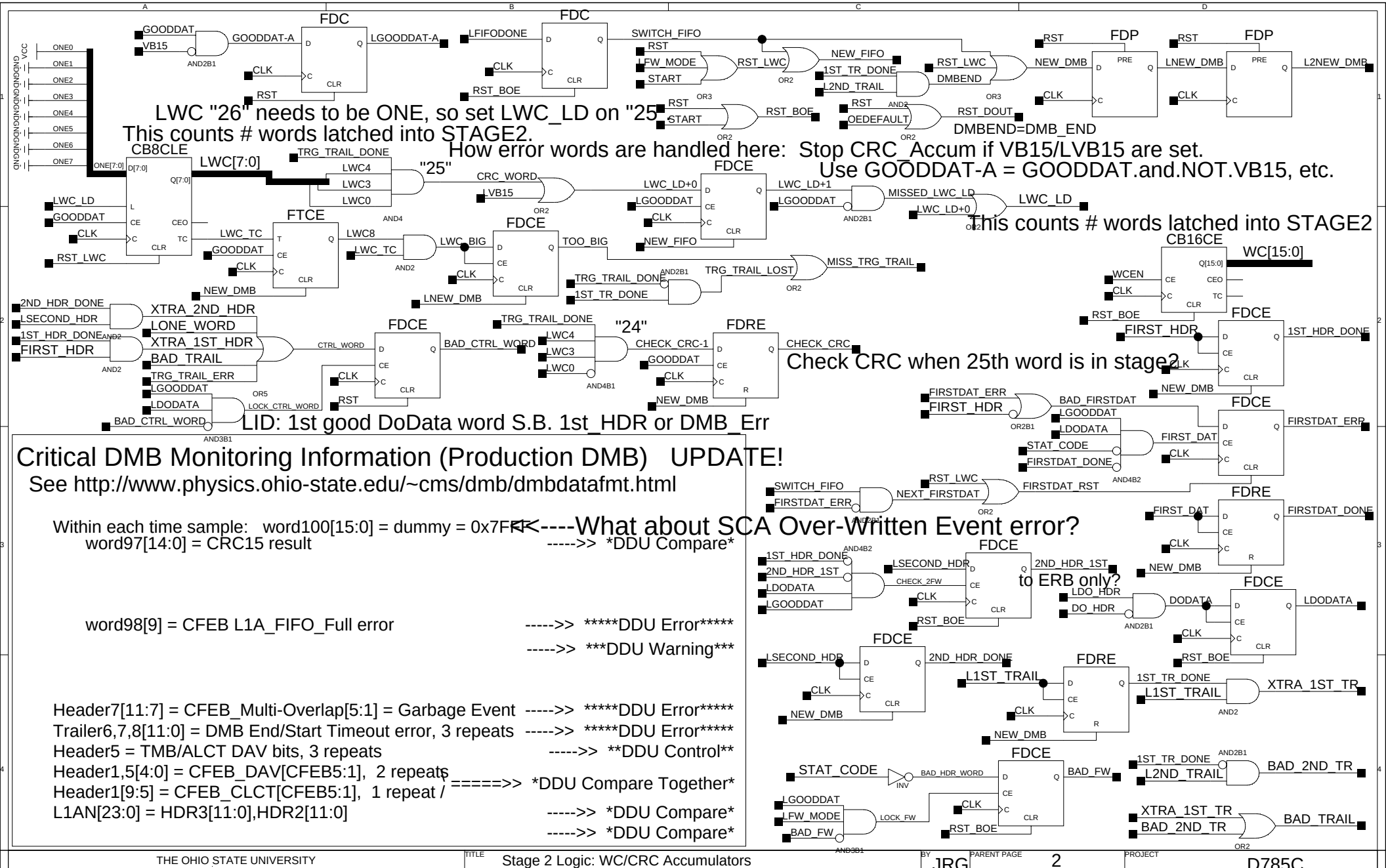
Control Bit List:

0: Gold Data (this FIFO has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB FIFO Data
8: End of Event (DONE--->OETrail)

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

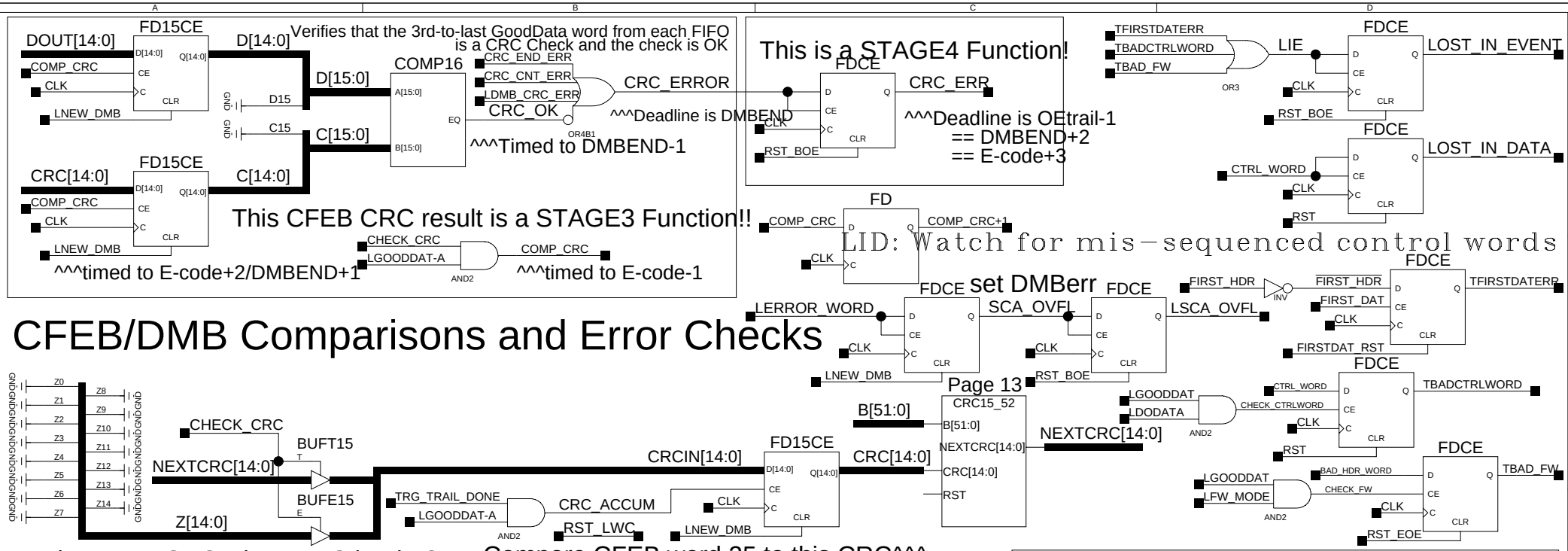
TITLE: Stage 2 Logic: WC/CRC Accumulators
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
9-13-2005_13:59	STAGE2 . 1	12

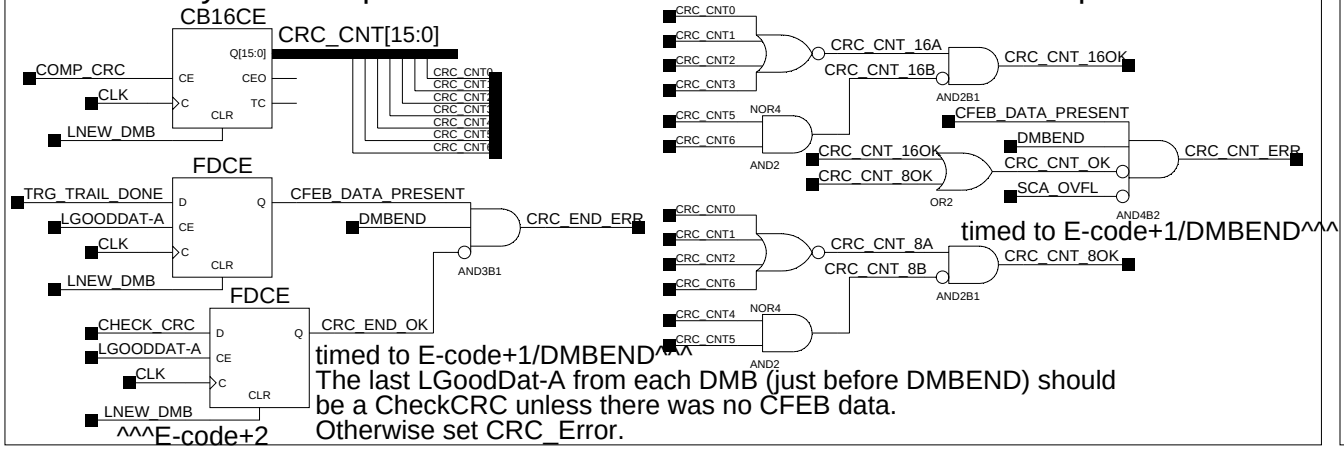


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-13-2005_12:07	FILE: STAGE2 . 2	PAGE: 12A

CFEB/DMB Comparisons and Error Checks

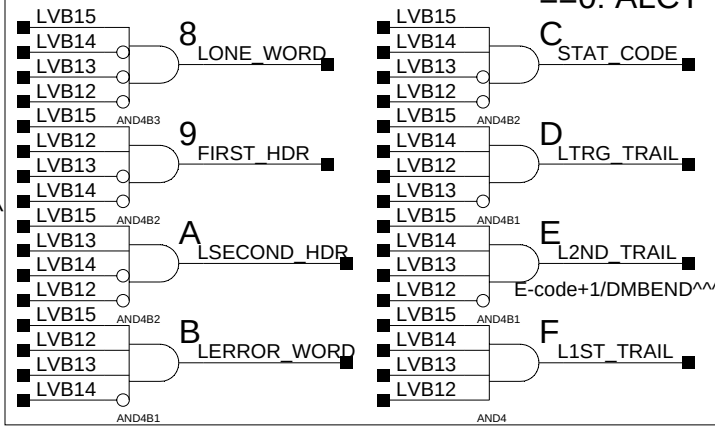


CFEB CRC Checks Done for this FIFO? Last non-control word S.B. CRC check. Verify that multiple of 8 /16 CRC Checks are done if CFEB data present.

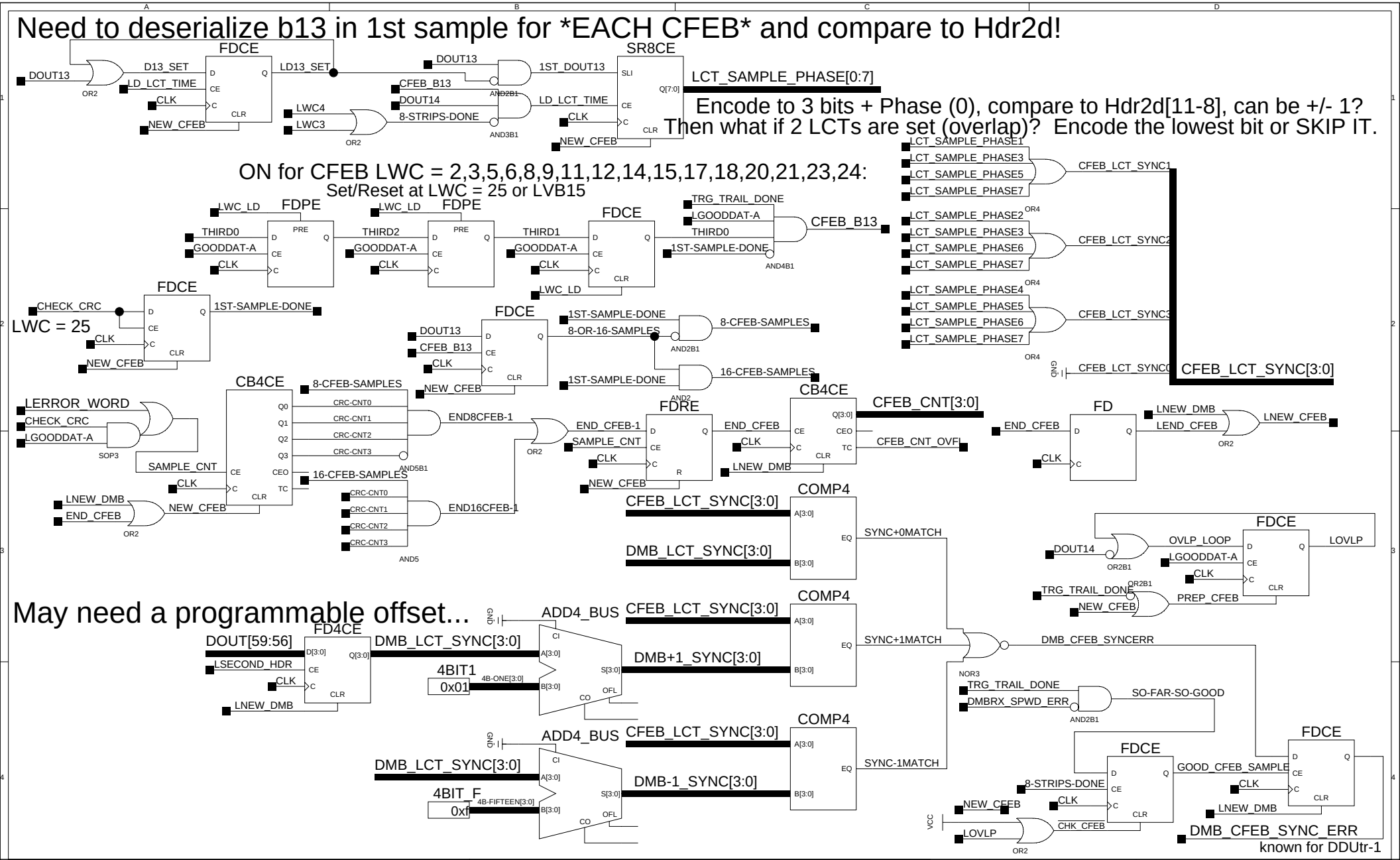


Latched Voted Special Bit Decode
Timed with LgoodData=GoodDat+1

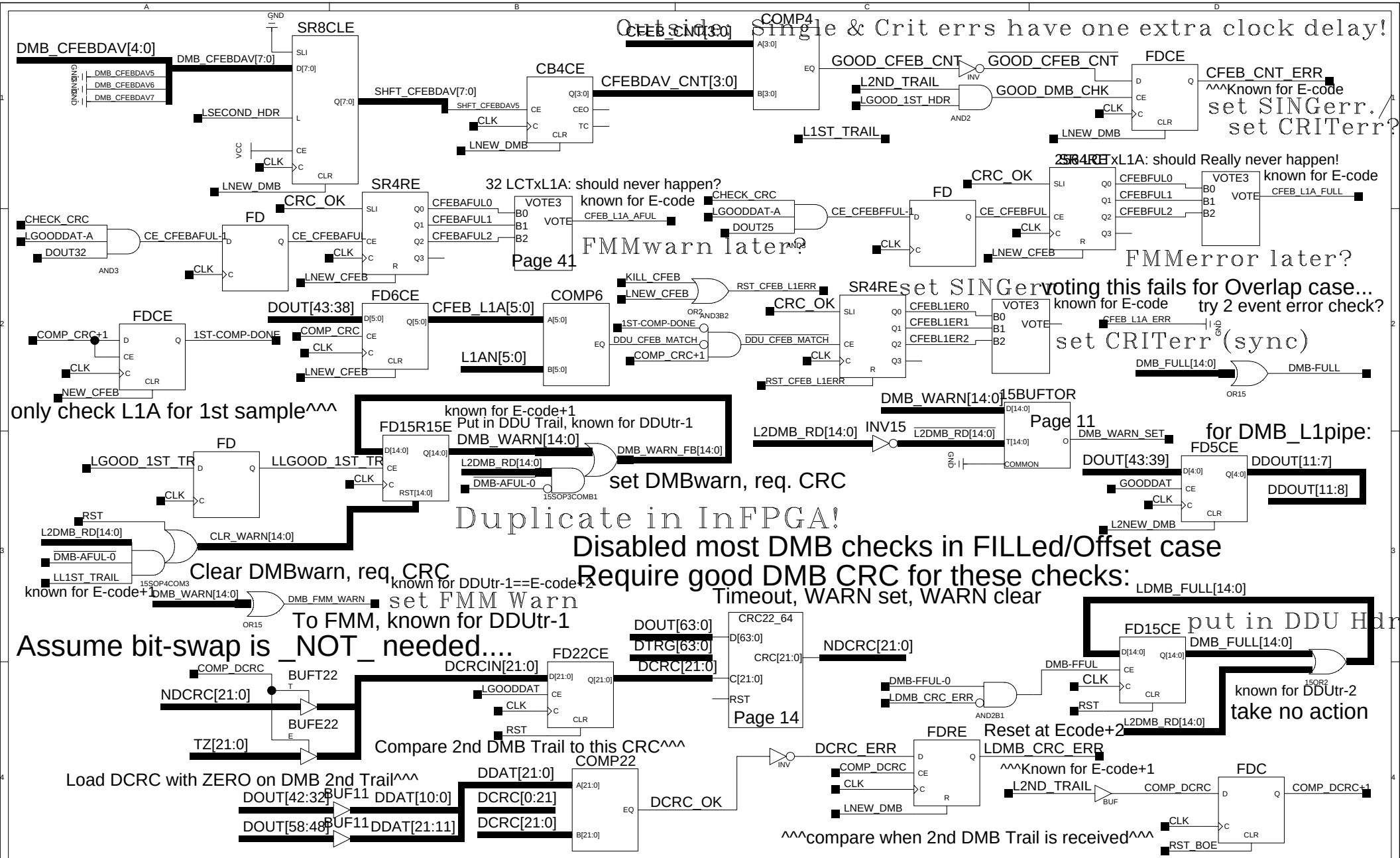
d-code, LVB11==1: TMB
==0: ALCT



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 9-13-2005_12:06	PROJECT: D785C FILE: STAGE2 . 3 PAGE: 12B

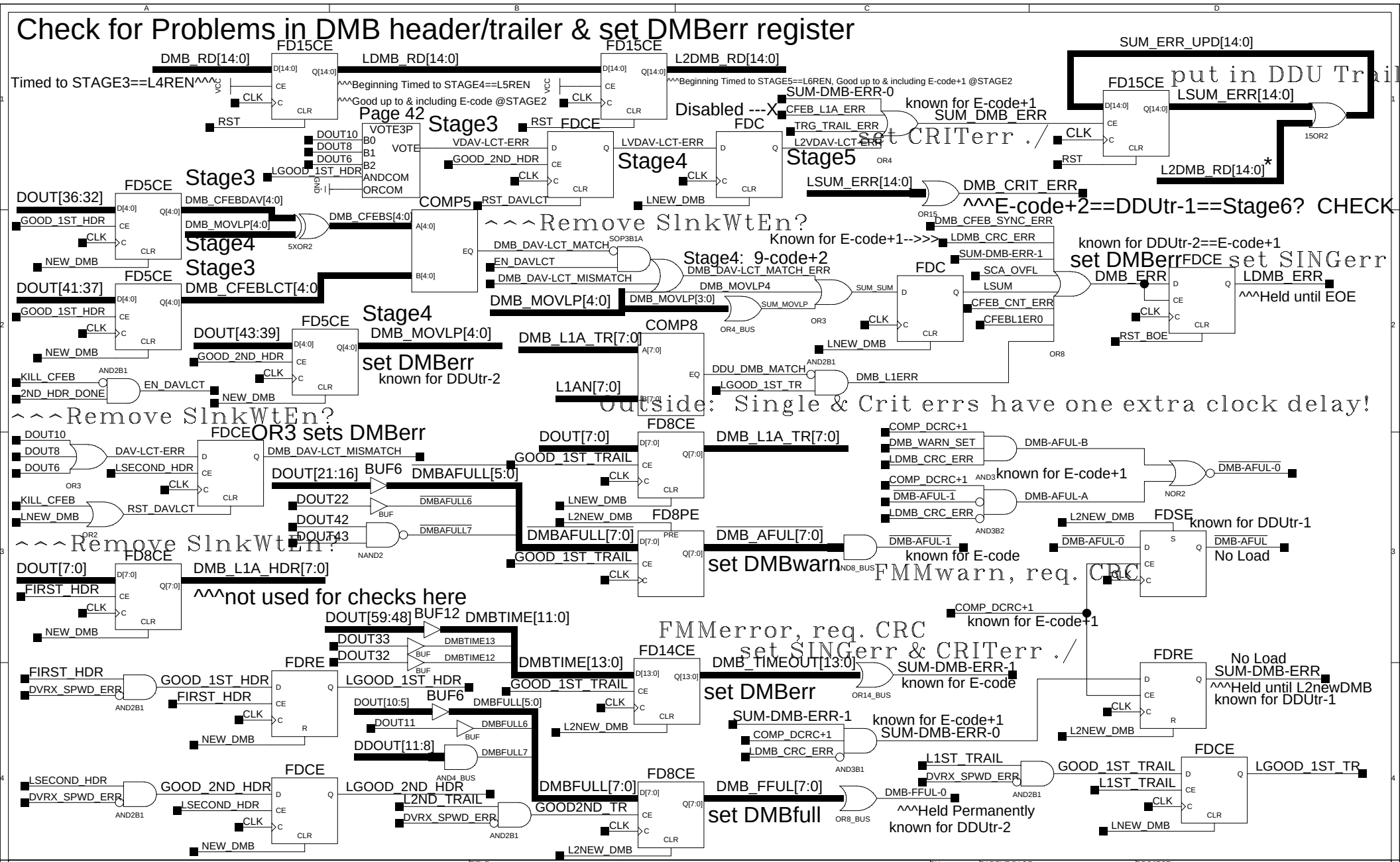


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Status Decode DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 6-29-2005_14:17	PROJECT: D785C FILE: STAGE2 . 4 PAGE: 12C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Count & DMB CRC Check DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C	
		DATE: 9-13-2005_15:30		FILE: STAGE2 . 5	PAGE: 12D

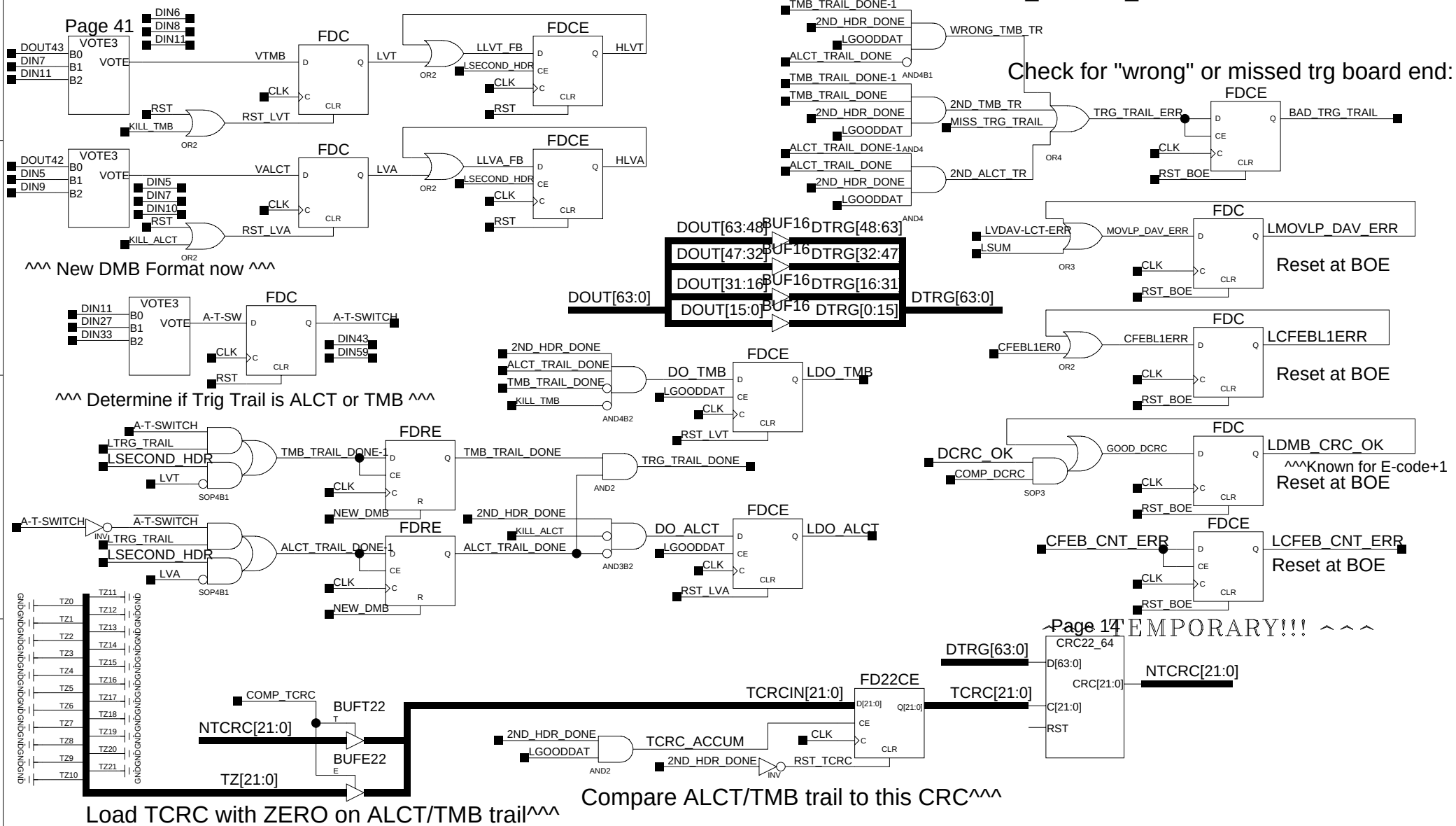
Check for Problems in DMB header/trailer & set DMBerr register



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DMB Status Checks DDU Controller CMS CSC Electronics	BY: JRG DATE: 9-14-2005_13:11	PARENT PAGE: 2 FILE: STAGE2 . 6
		PROJECT: D785C	PAGE: 12E

Trigger CRC Check Control: assume that TMB comes after ALCT!

^^^affects L1A check: DoTMB, 1st_TMB/1st_ALCT

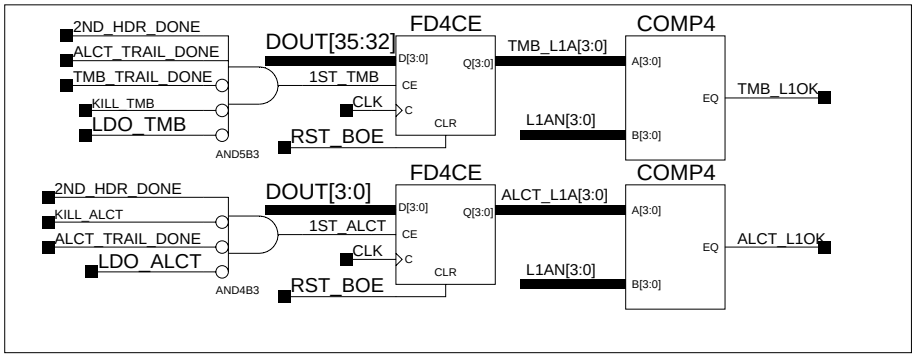


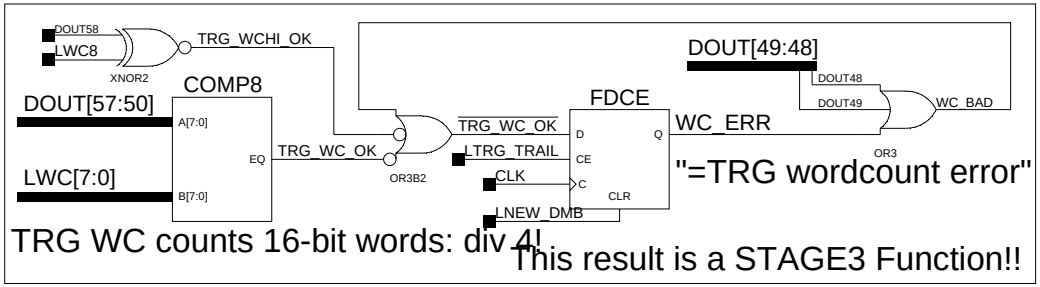
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

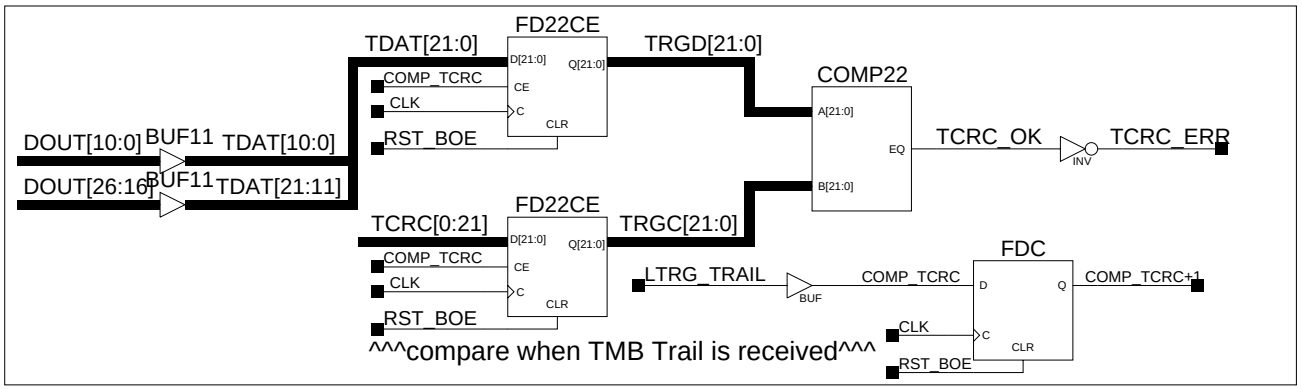
TITLE: Stage 2 Logic: Trigger Board Flags
DDU Controller
CMS CSC Electronics

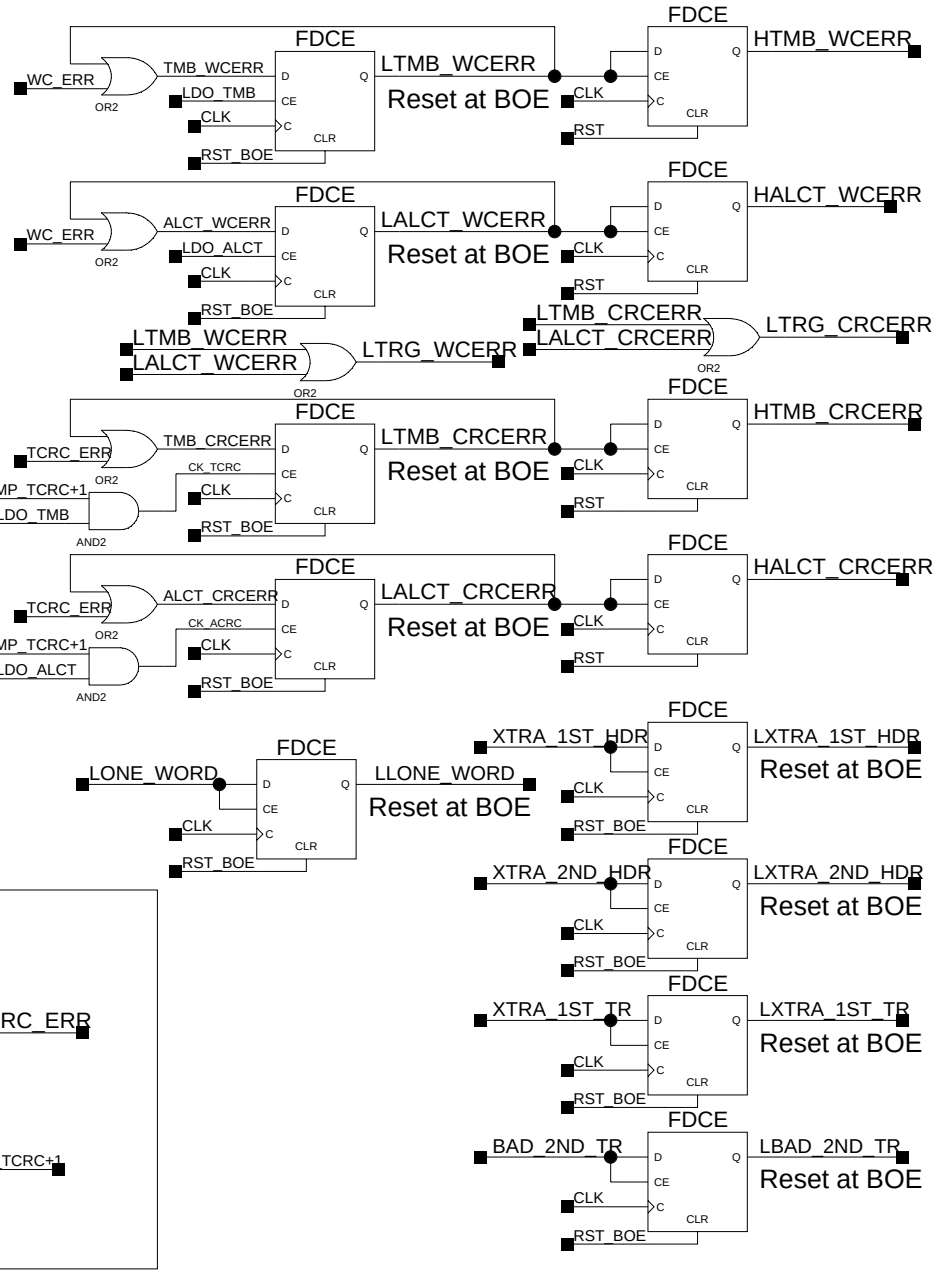
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
9-13-2005_11:56	STAGE2 . 7	12F

Trigger Comparisons and Error Checks

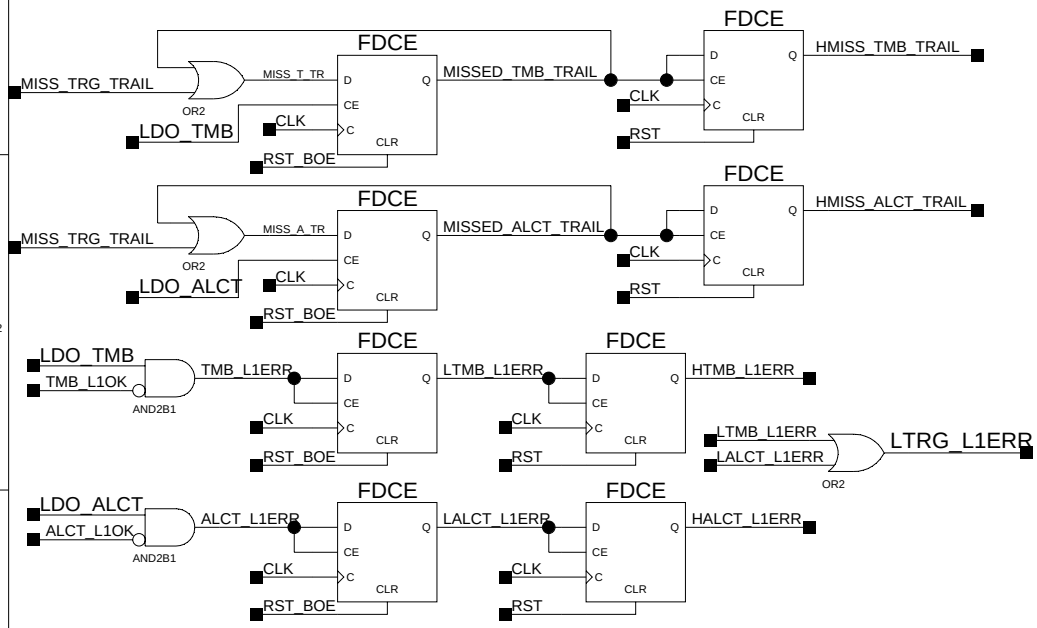


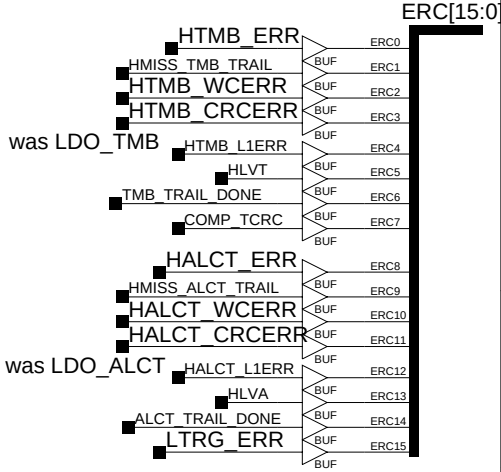






Trigger Error Registers



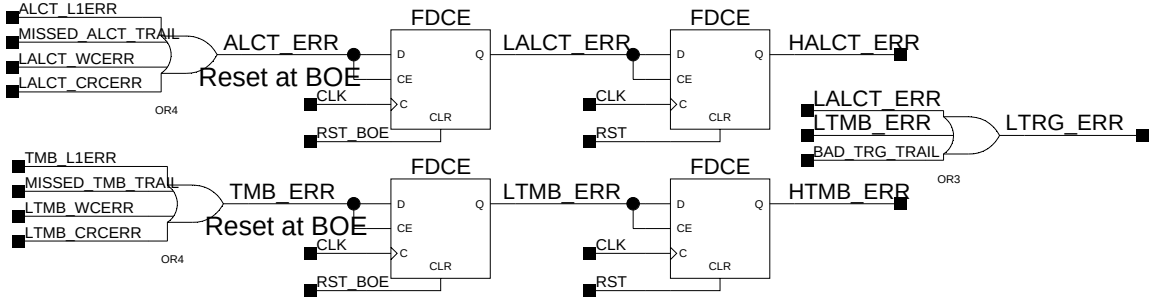


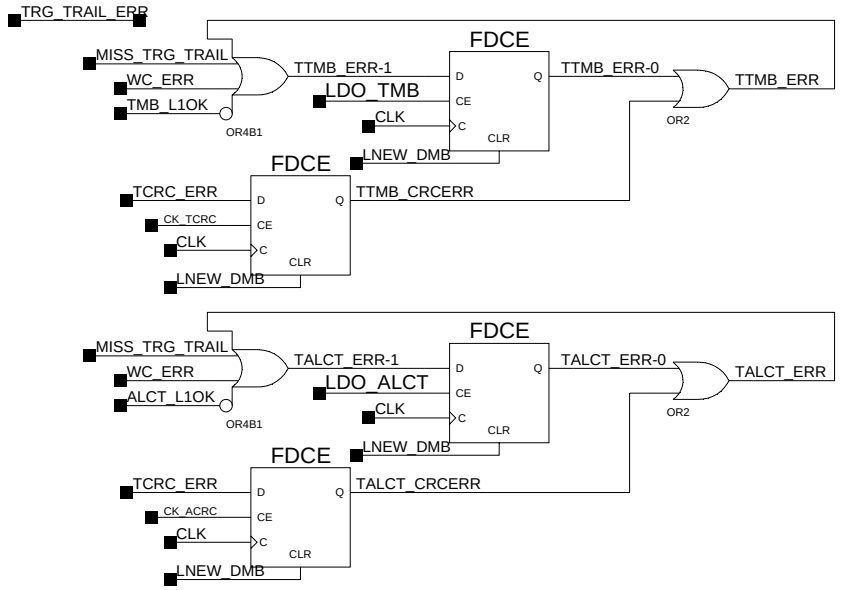
CSC case by LTRG_Trail+1?

TMB/ALCT need Err Reg's for CSC/EVT

CRC: Evt WC: Evt L1err: Evt

TMBerr: CSC&Evt ALCTerr: CSC&Evt

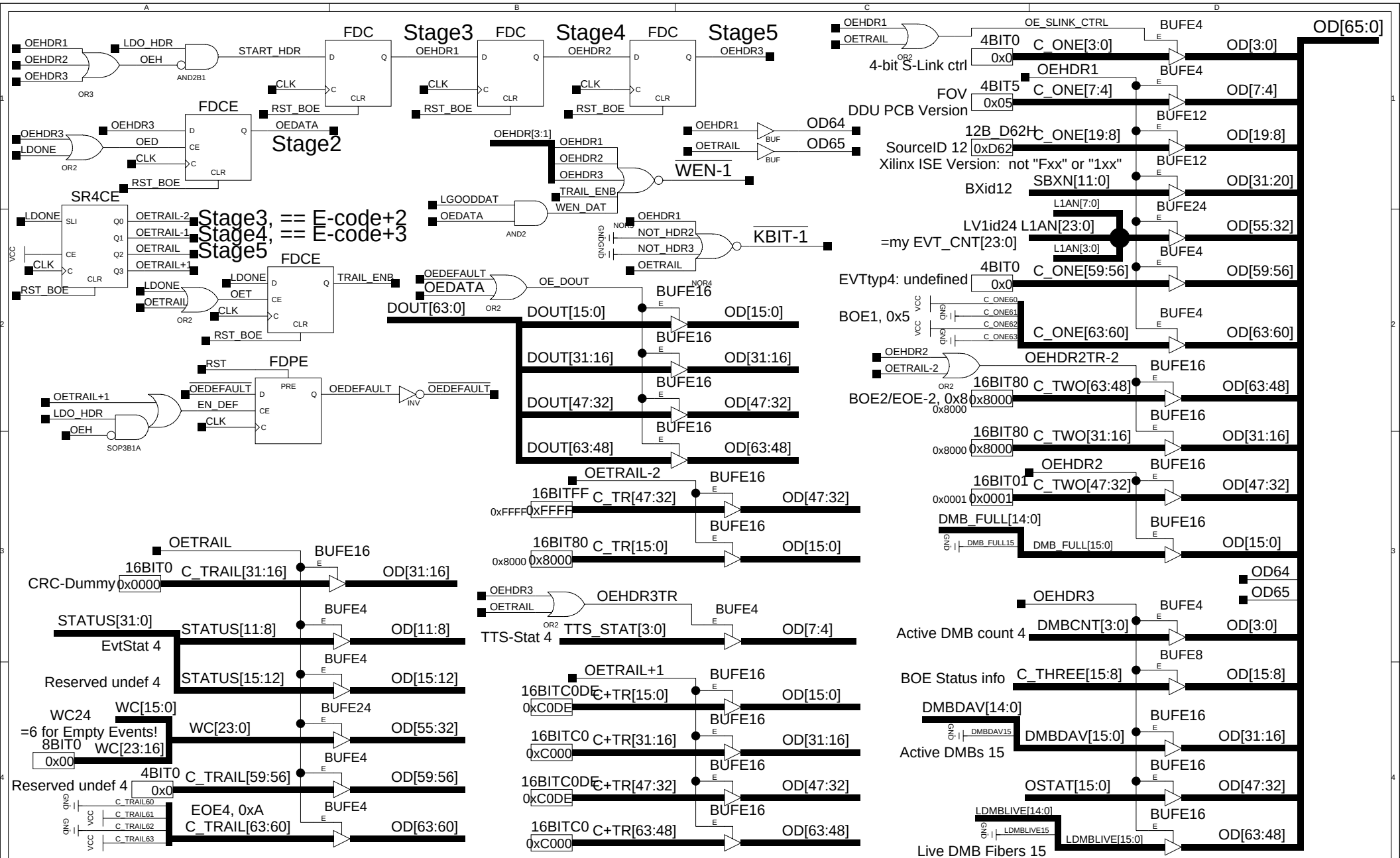




THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Stage 2 Logic: Trigger Error Registers
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
9-13-2005_11:58	STAGE2 . 9	12H



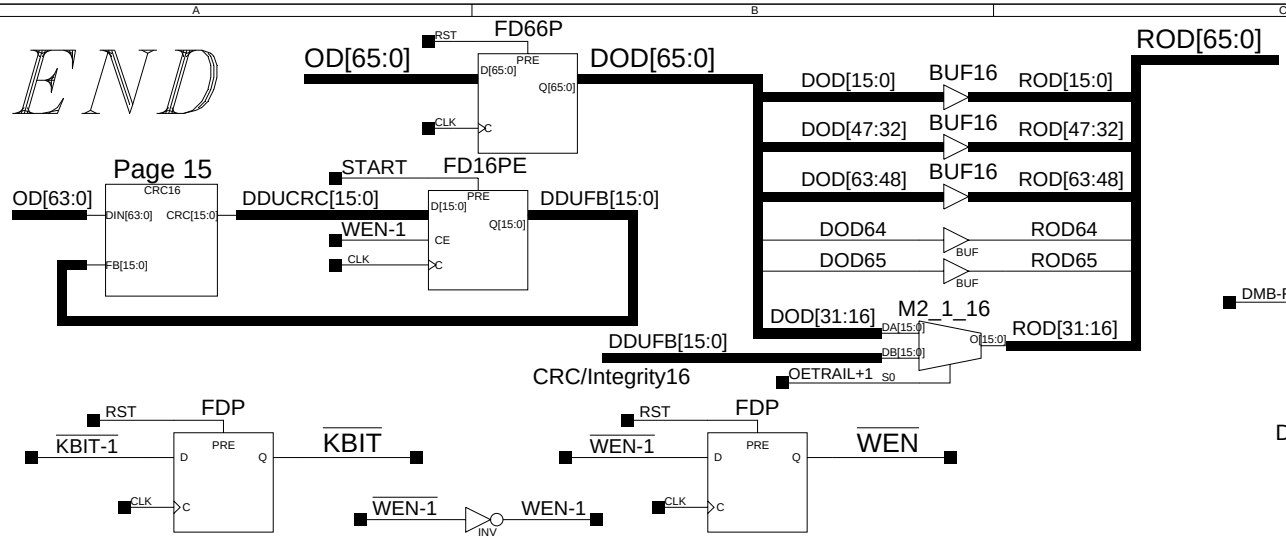
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

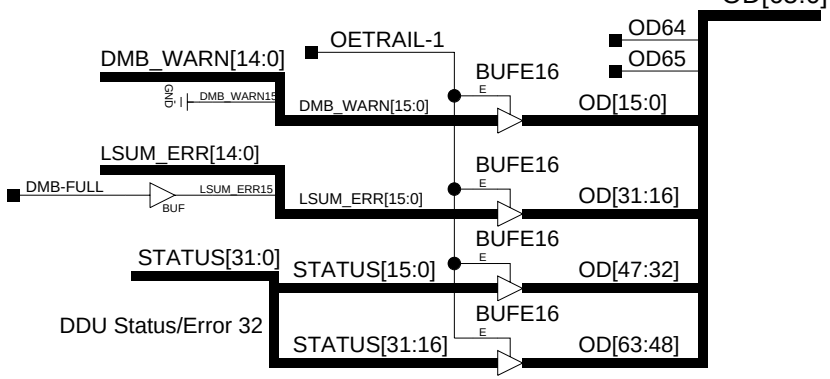
TITLE: Stage 2 Logic: DDU Header/Trailer Control
DDU Controller
CMS CSC Electronics

BY: JRG
PARENT PAGE: 2
DATE: 9-13-2005_11:59
PROJECT: D785C
FILE: STAGE2 . 10
PAGE: 12I

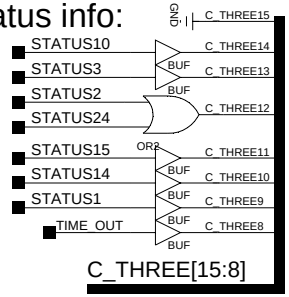
END

Page 15





BOE Status info:



DDU Timing Info

DDUctrl to InFIFO signals: 2" – 4", .3ns – .6ns
IRCLK has 4 loads, may slow signal by 0.1–0.5ns
CKFBout has normal drive, IRCLK has ~1.1ns Faster drive

FPGA I/O Delays (lvcmos33, ns)

IBUF: 0.92
IFD set/hold: 0.92/–0.12 Clk to Q: 0.65

OBUF: 2.33
OFD set/hold: 0.26/0.14 Clk to Q: 2.41
*modifiers for drive/slew settings:
6mA: add 2.60 for Slow, 1.28 for Fast
8mA: add 1.69 for Slow, 0.46 for Fast
12mA: add 1.18 for Slow, 0.26 for Fast
16mA: add 0.52 for Slow, 0.02 for Fast
24mA: +0.44 for Slow, –0.08 for Fast

FPGA CLB Delays (ns)

4–FG: 0.32 5–FG: 0.65
FD set/hold: 0/0.14 Clk to Q: 0.38
Sync. set–rst setup: 0.60
Async. pre–clr to Q: 1.25
SR16 Clk to Q: 3.12
SR32 Clk to Q: 3.49
SI set/hold: 0.34/0.01

TI FIFO I/O Delays (ns)

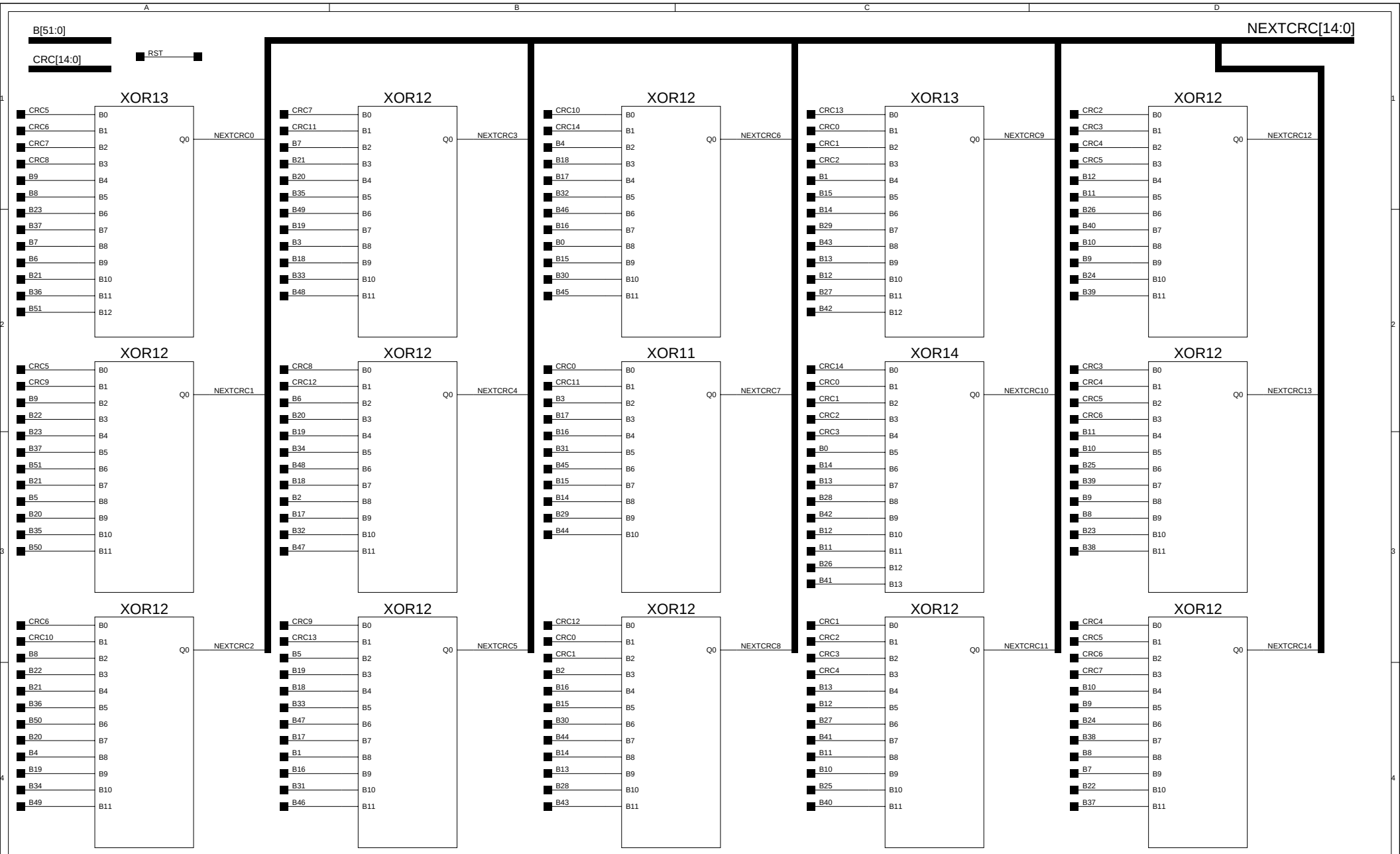
Meas'd on FIFO test board

	Vcc: 3.38V	3.04V
RCLK to Empty (low state) Max: 3.6, Min: 2.5	3.02–3.18	3.20–3.29
to Not Empty (high state)	3.22–3.34	3.23–3.31
RCLK to Q11 False (low state) Max: 4.3, Min: 2.5	3.32–3.62	3.40–3.64
to Q11 True (high state)	3.31–3.87	3.51–4.06
to Q11 (low state)	3.22–3.34	3.2

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU CRC Logic for SLINK/C.D.F. Compatibility
DDU Controller
CMS CSC Electronics

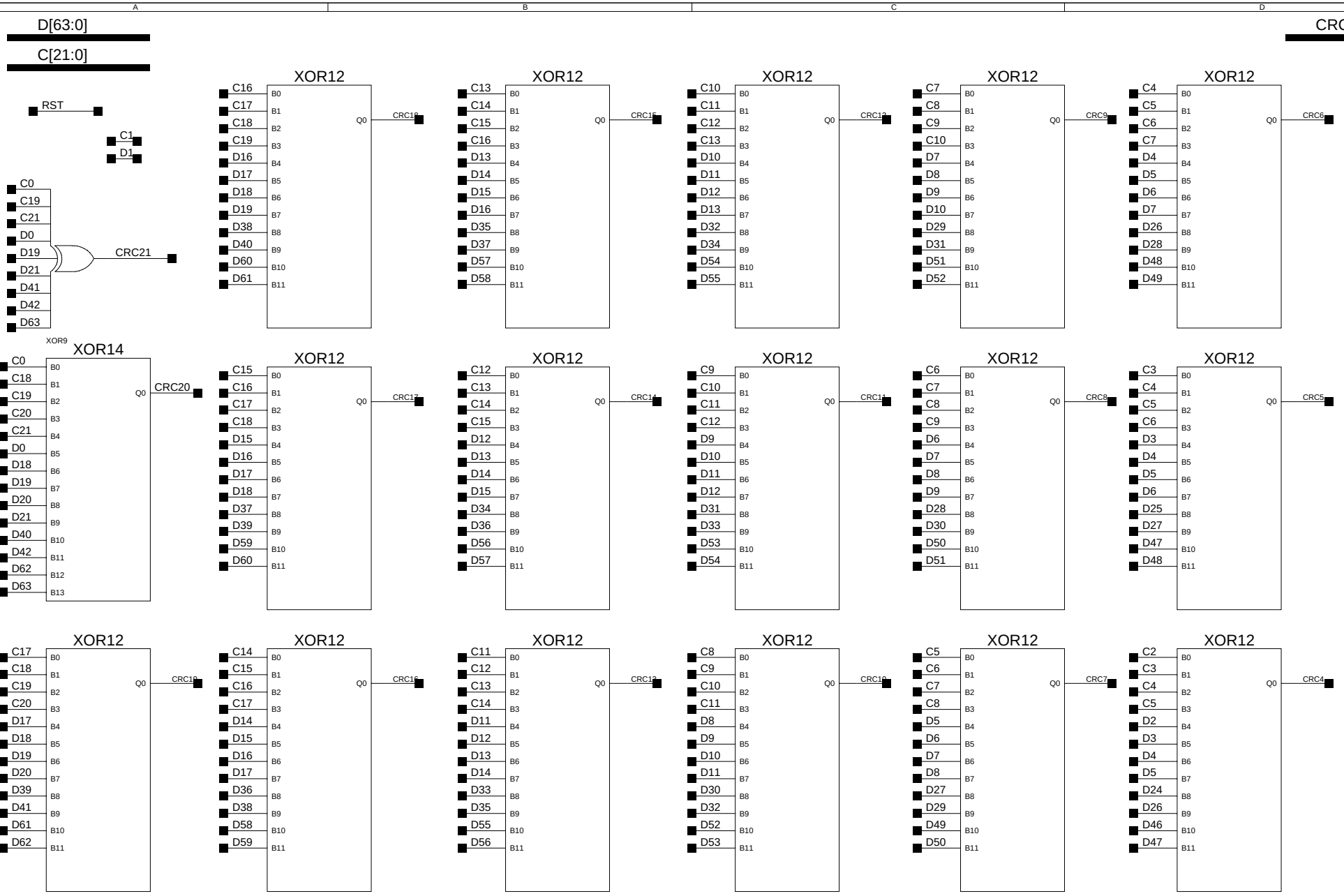
BY: JRG PARENT PAGE: 2 PROJECT: D785C
DATE: 8-16-2005_9:55 FILE: STAGE2 . 11 PAGE: 12J



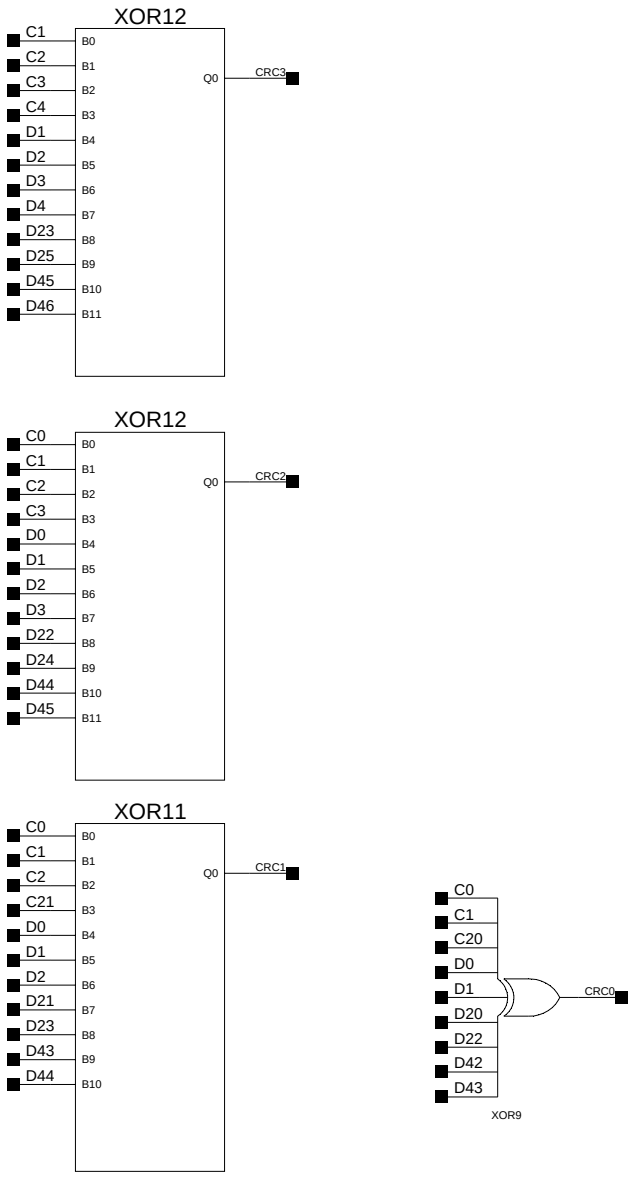
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: CRC15, 52-bit wide data equations
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	12B	D785C
DATE	FILE	PAGE
1-26-2005_11:33	CRC15_52 . 1	13

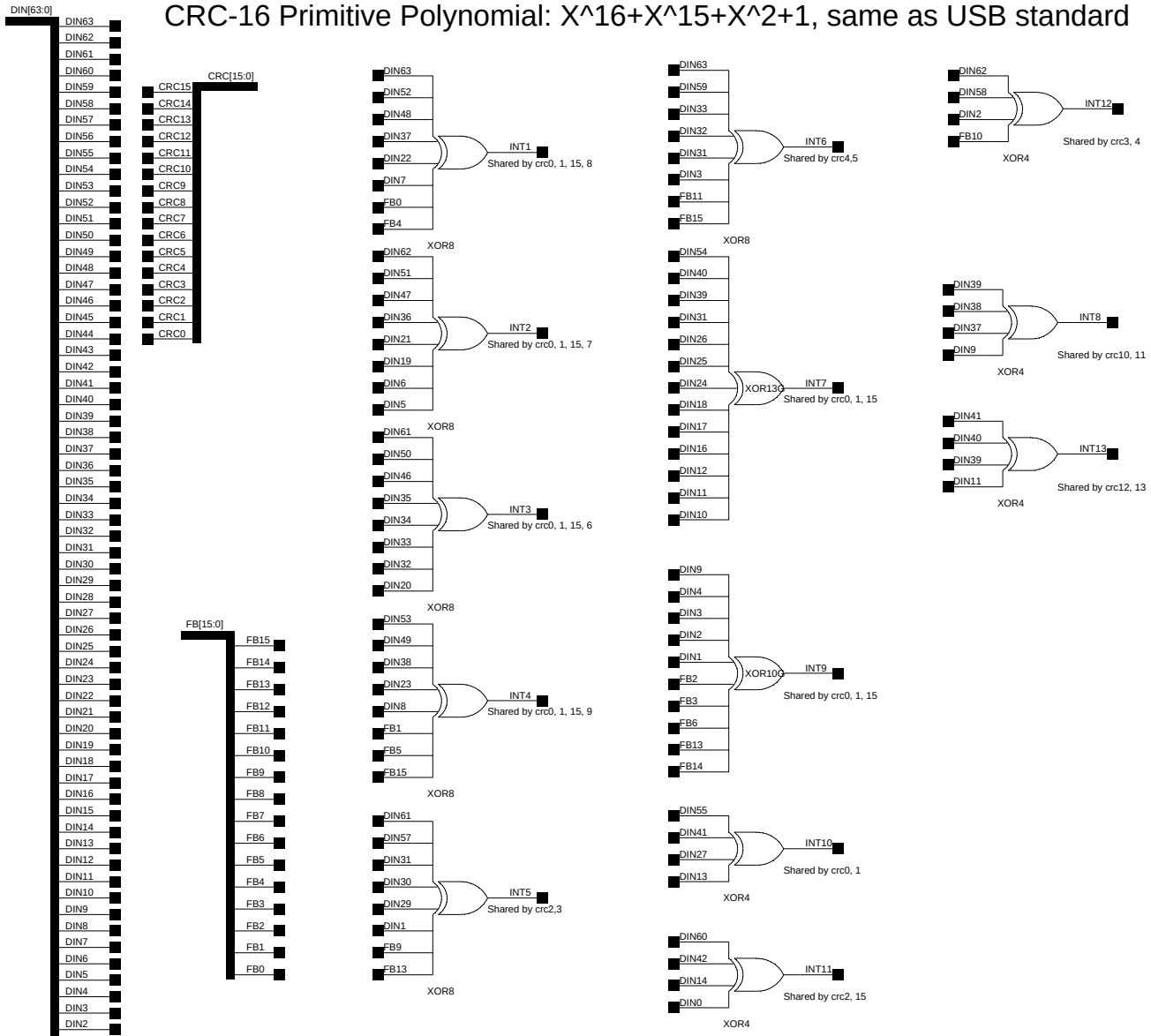


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:33	PARENT PAGE: 12C FILE: CRC22_64 . 1	PROJECT: D785C PAGE: 14

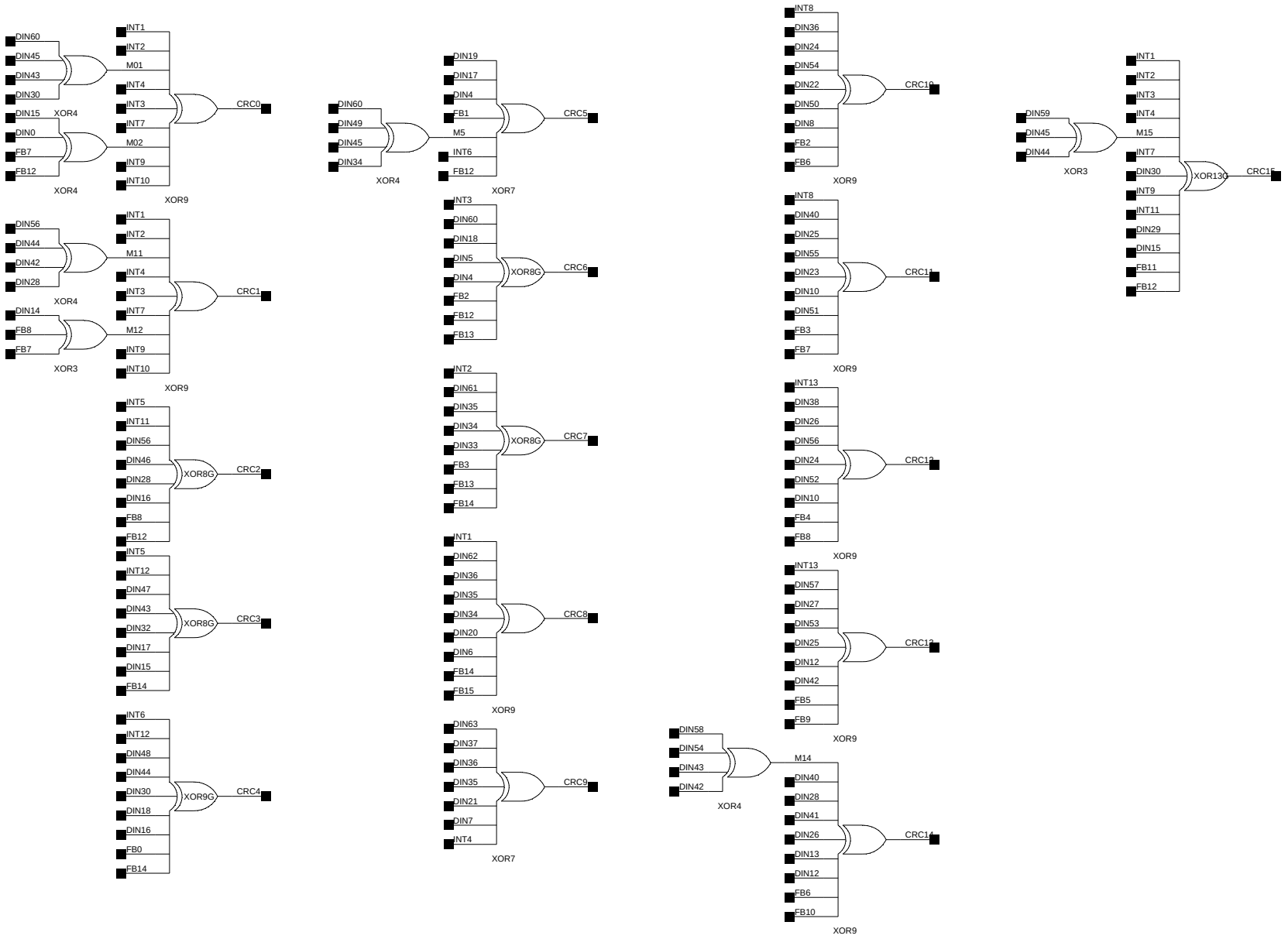


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:34	PARENT PAGE: 12C	PROJECT: D785C FILE: CRC22_64 . 2 PAGE: 14A

CRC-16 Primitive Polynomial: X^16+X^15+X^2+1, same as USB standard



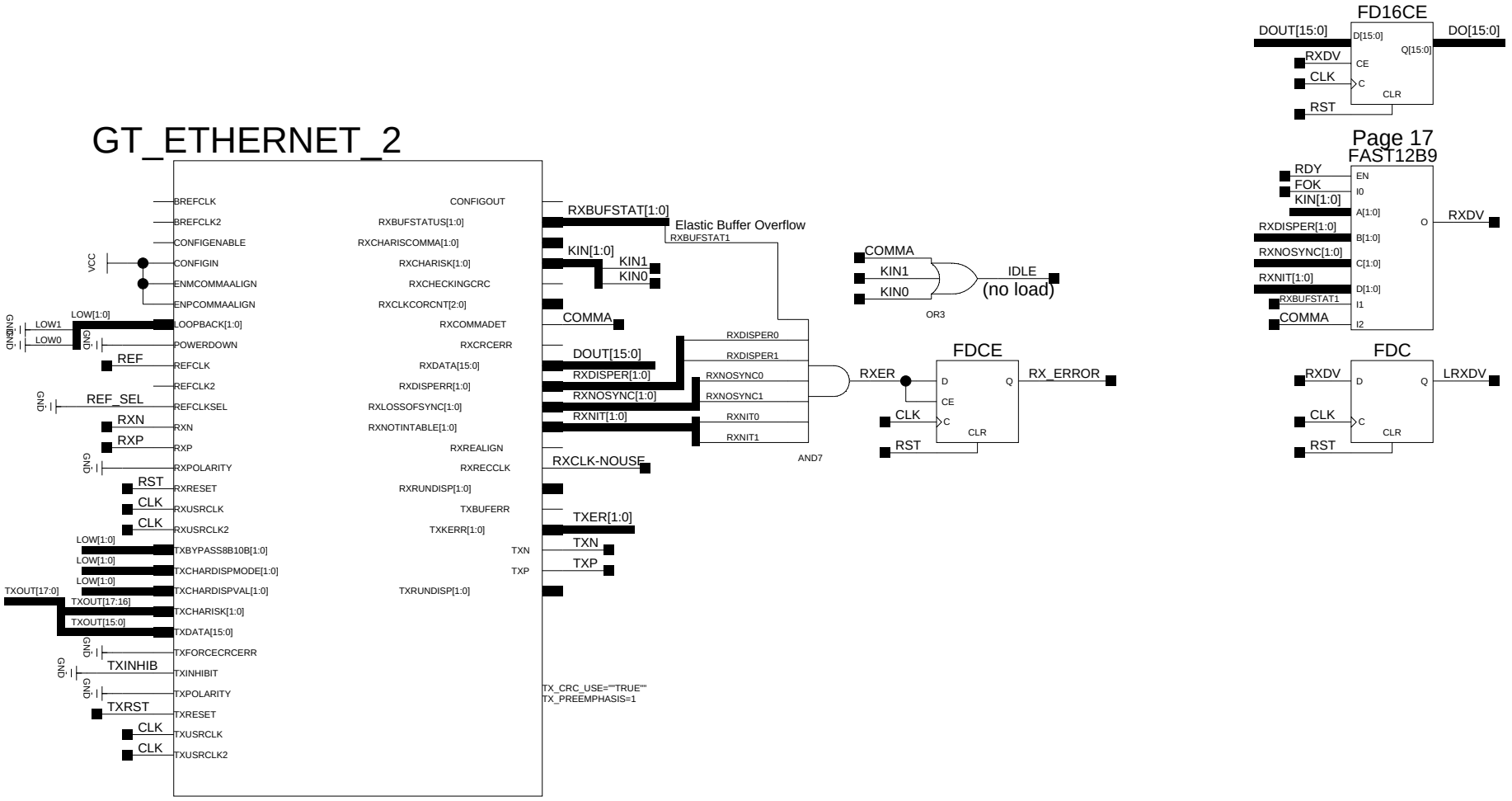
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	SLINK CRC16 Calculation, common components DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
			DATE 2-7-2005_17:50	FILE CRC16 . 1	PAGE 15



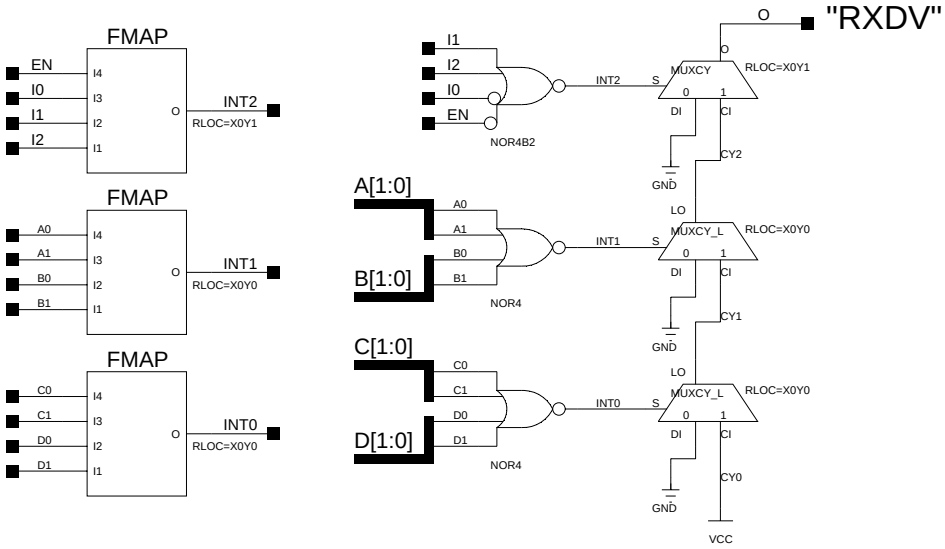
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: SLINK CRC16 Calculation DDU Slink Interface FPGA CMS CSC Electronics	BY: GU	PARENT PAGE: 12F	PROJECT: D785C
		DATE: 2-7-2005_17:50	FILE: CRC16 . 2	PAGE: 15A

Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.

---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.

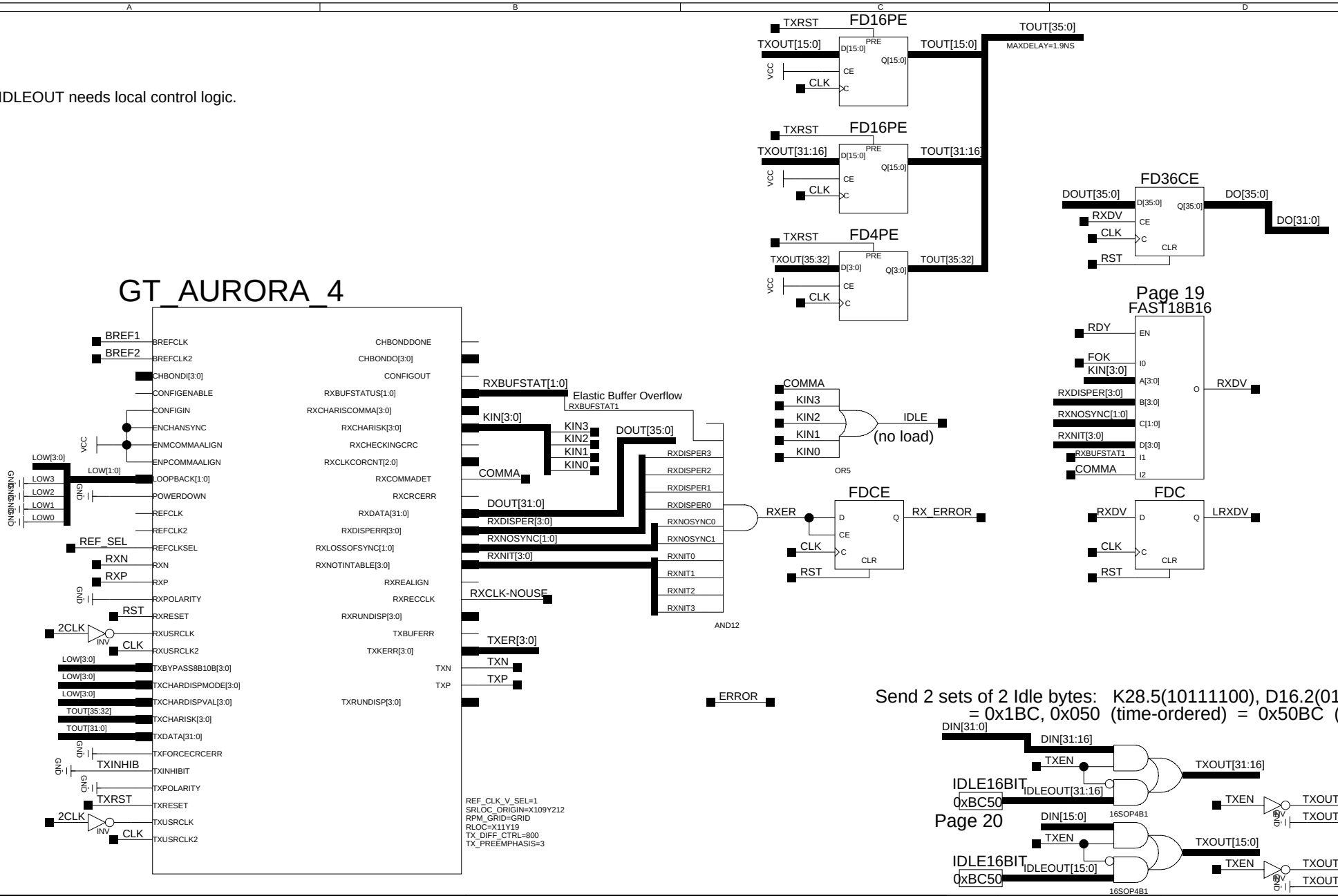


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Gigabit Ethernet Tranceiver DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:14	PARENT PAGE: 2E FILE: OUT_GBE . 1	PROJECT: D785C PAGE: 16

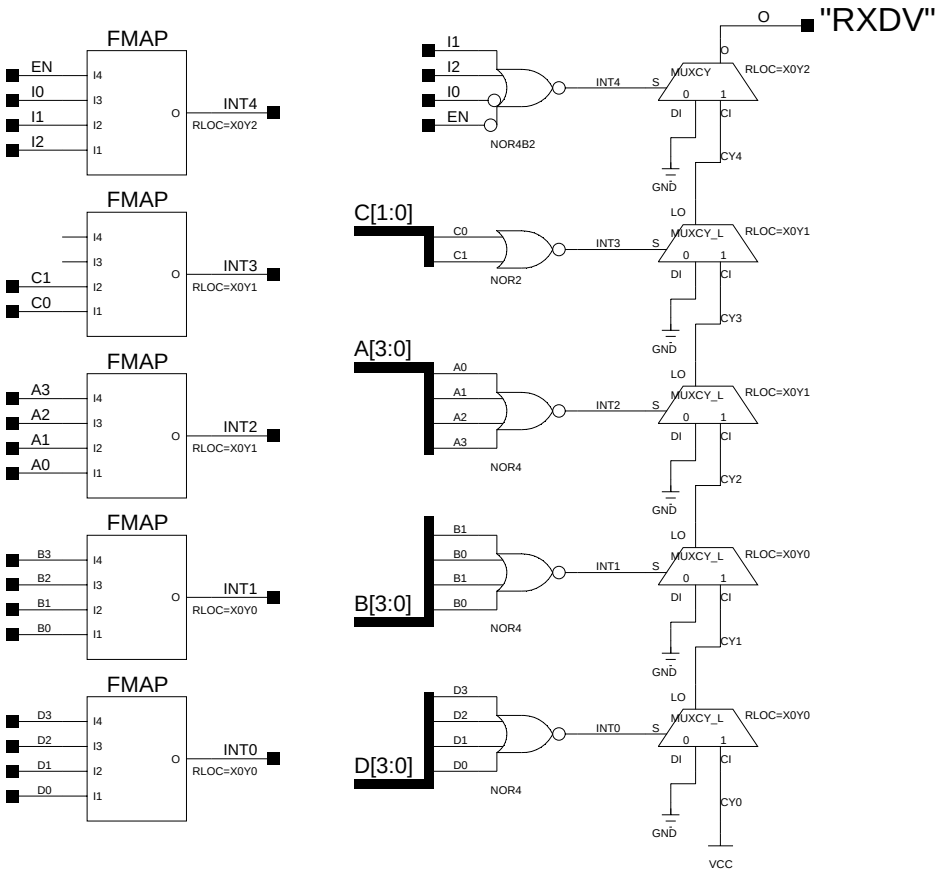


XILINX			JRG
Title:	FAST12B9		
Comments:	Custom Logic for DDU similar to: AND12B9		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

IDLEOUT needs local control logic.



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Multi Gigabit Tranceiver DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2E
		DATE 7-18-2005_16:15	PROJECT D785C
		FILE OUT_UNIT . 1	PAGE 18



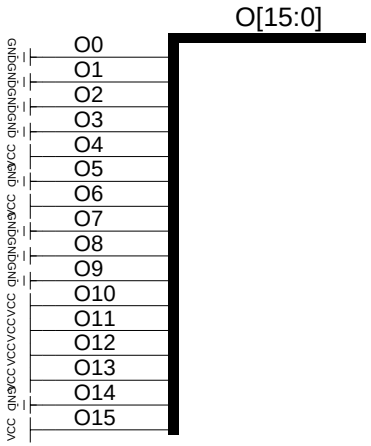
XILINX			JRG
Title:	FAST13B10		
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)

= 0x1BC + 0x050 (time-ordered)

= 0xBC50 (in parallel)

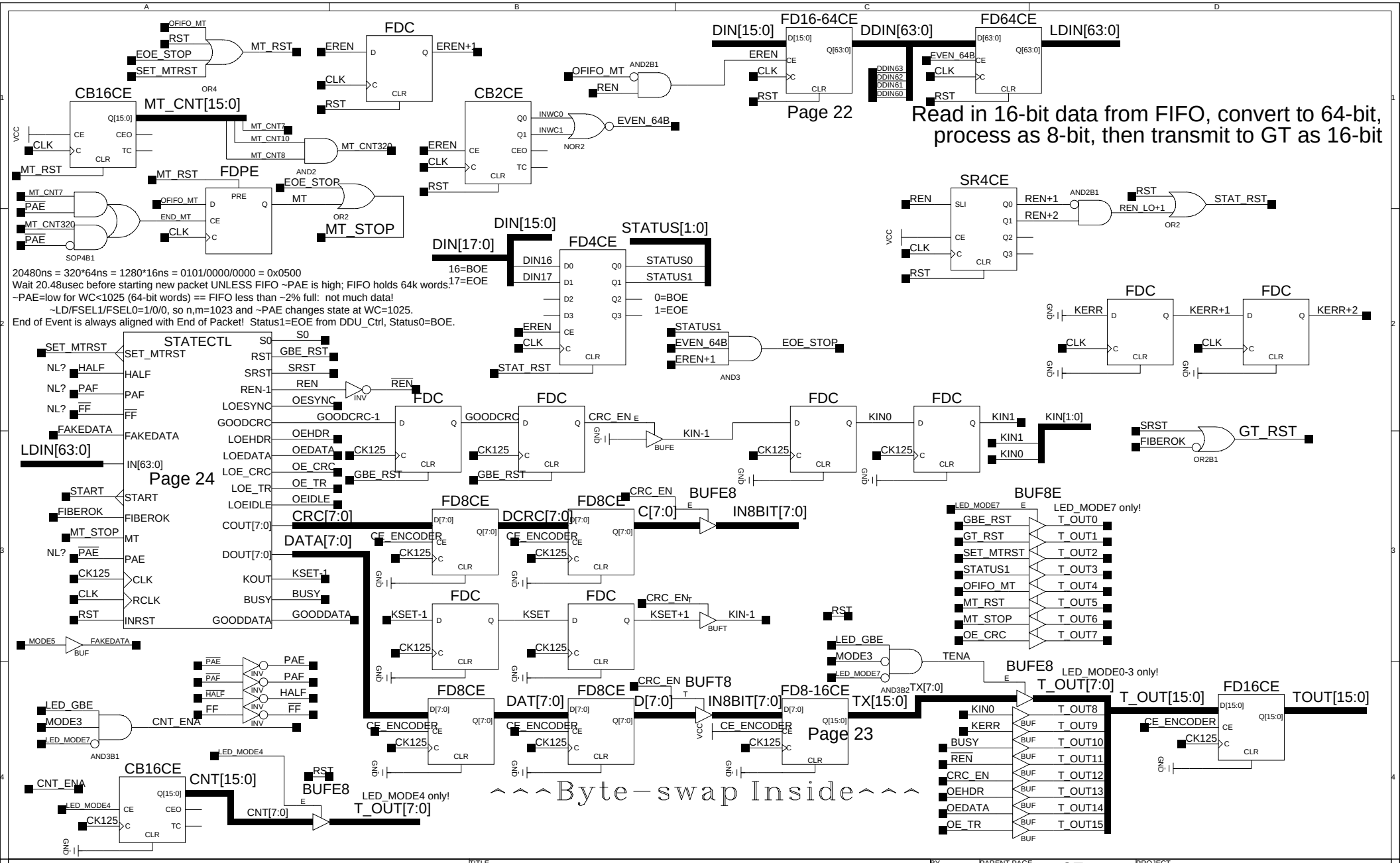


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

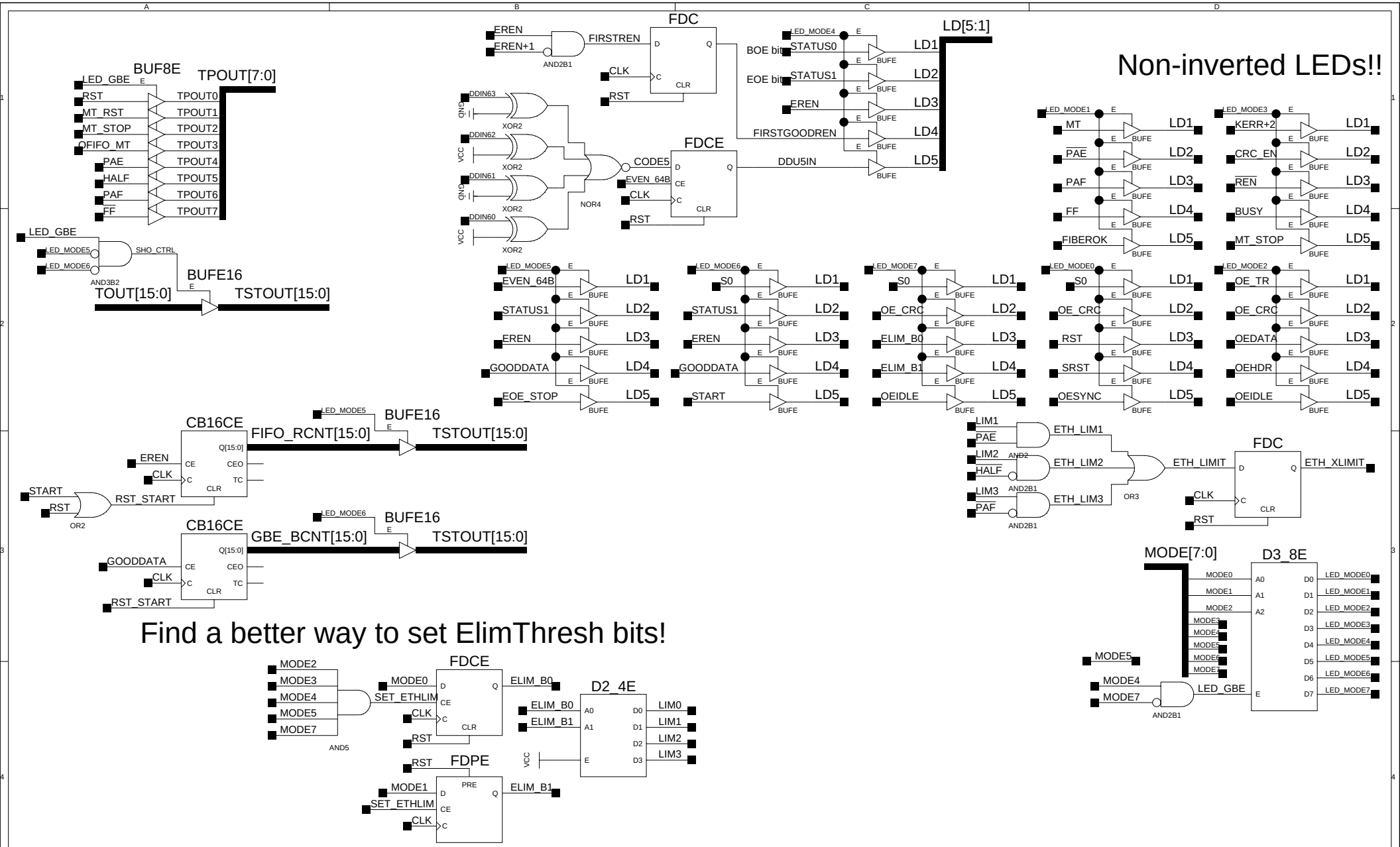
TITLE: Gigabit "Idle" Code
Constant Bus Settings
CMS CSC Electronics

BY: JRG | PARENT PAGE: 18 | PROJECT: D785C

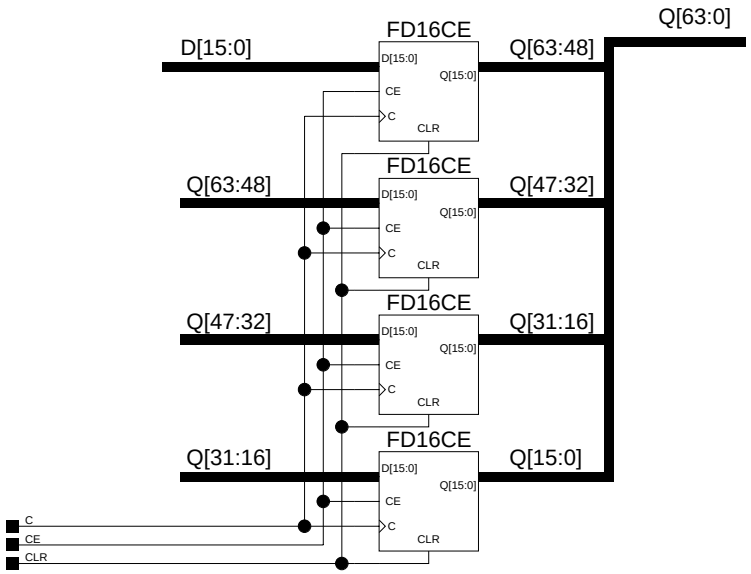
DATE: 1-26-2005_11:43 | FILE: IDLE16BIT . 1 | PAGE: 20



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2F	PROJECT D785C	
		DATE 8-1-2005_12:56		FILE ETHCNTRL . 1	PAGE 21



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-22-2005_16:55	PARENT PAGE: 2F FILE: ETHCNTRL . 2
		PROJECT: D785C	PAGE: 21A



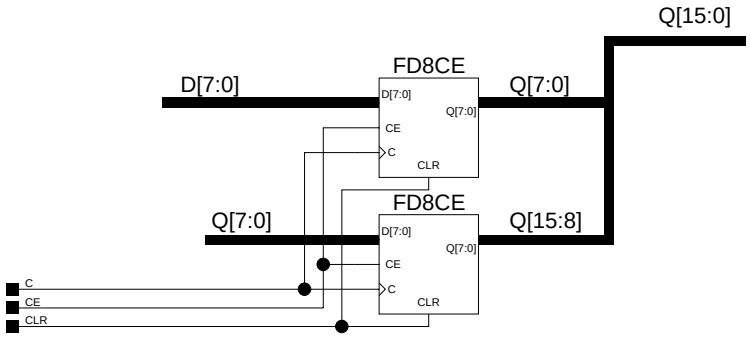
XILINX

JRG

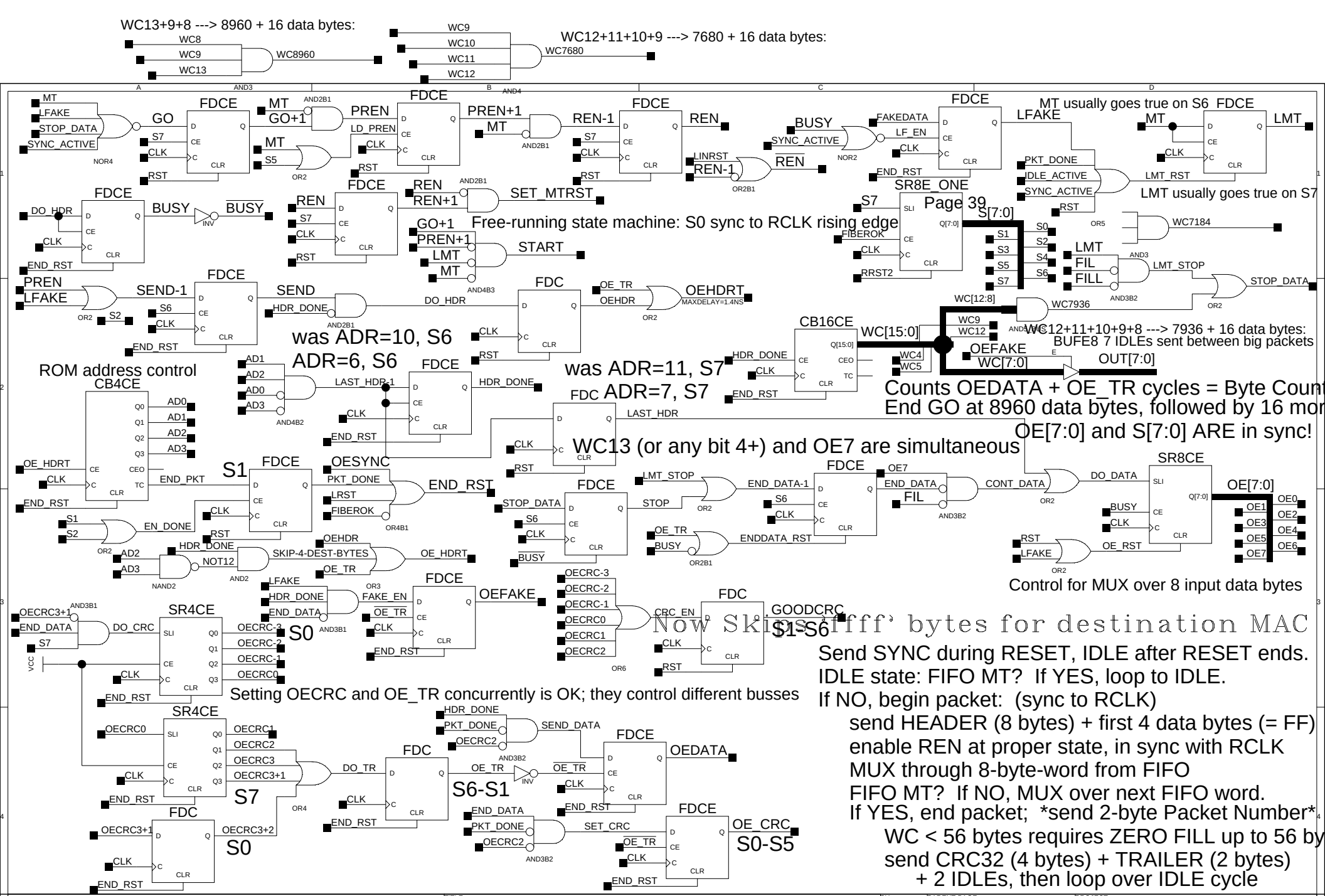
Title: VIRTEX Family FD16-64CE Macro

16-bit Bus Matching Register with Asynchronus Clear and Chip Enable

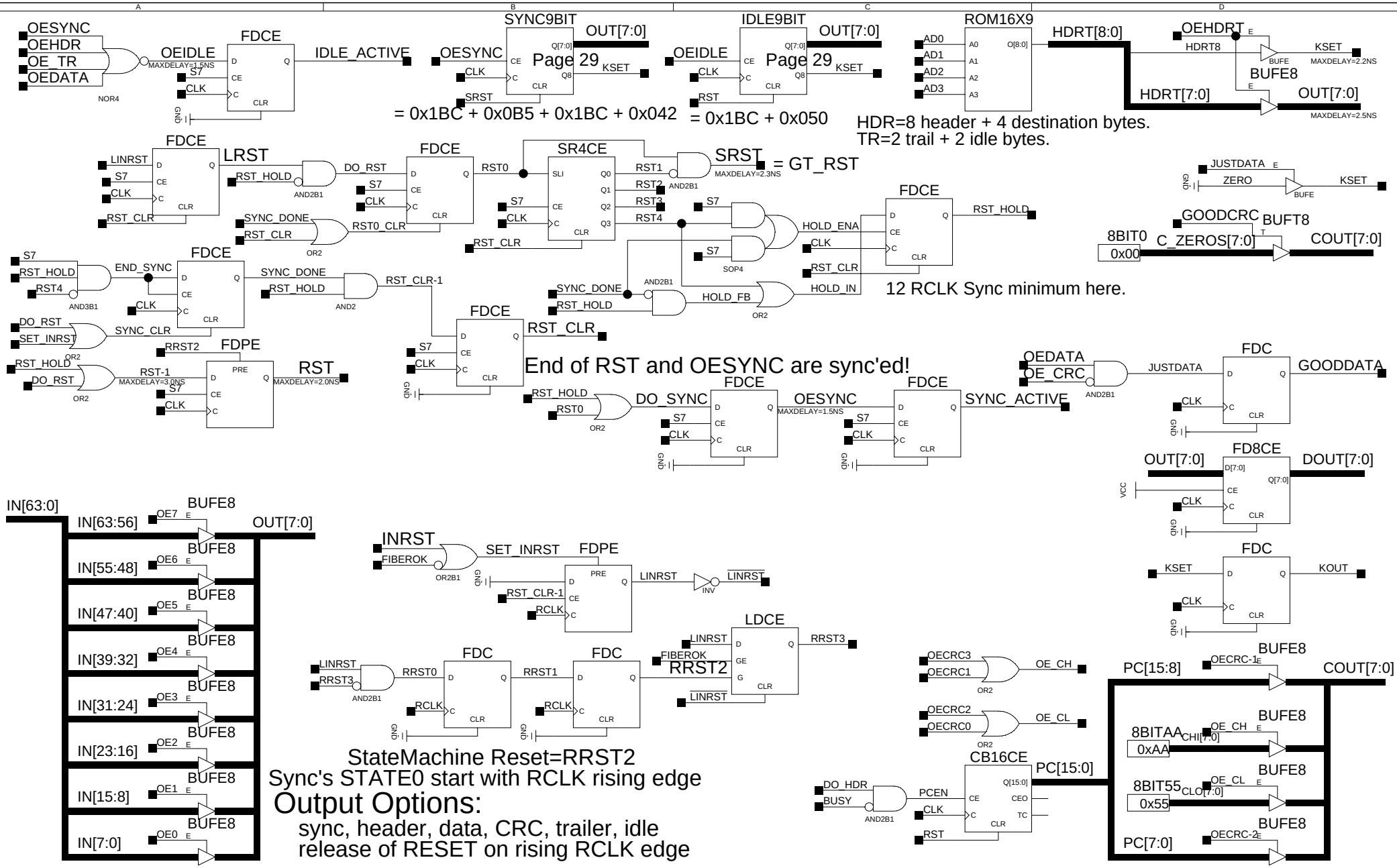
Date:	2nd February 2004	Ver:	1
Sheet Size: B		Rev:	A



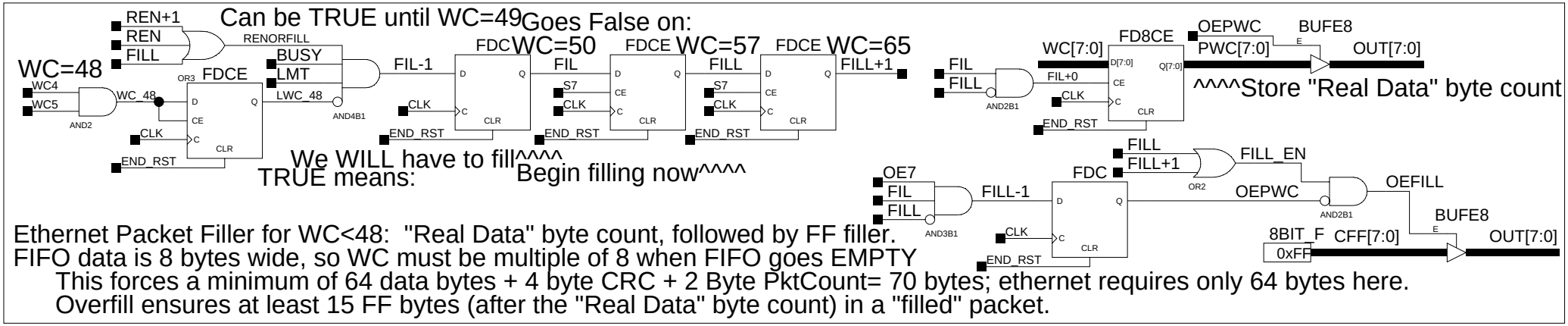
XILINX		JRG	
Title:	VIRTEX Family FD8-16CE Macro		
Comments:	8-16-Bit Bus Matching Register with Asynchronus Clear and Chip Enable		
Date:	4th February 2004	Ver:	1
Sheet Size: B		Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-29-2005_13:26	PARENT PAGE: 21A FILE: STATECTL . 1
		PROJECT: D785C	PAGE: 24



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:19	PARENT PAGE: 21A FILE: STATECTL . 2
		PROJECT: D785C	PAGE: 24A



Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.

THE OHIO STATE UNIVERSITY
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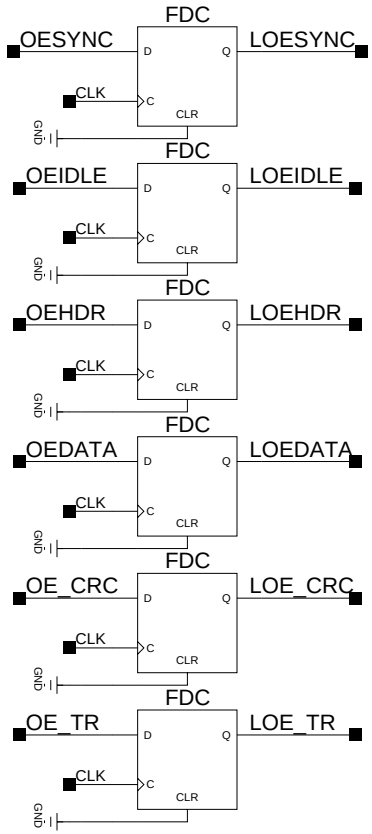
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: State Machine Control
DDU Ethernet Logic
CMS CSC Electronics

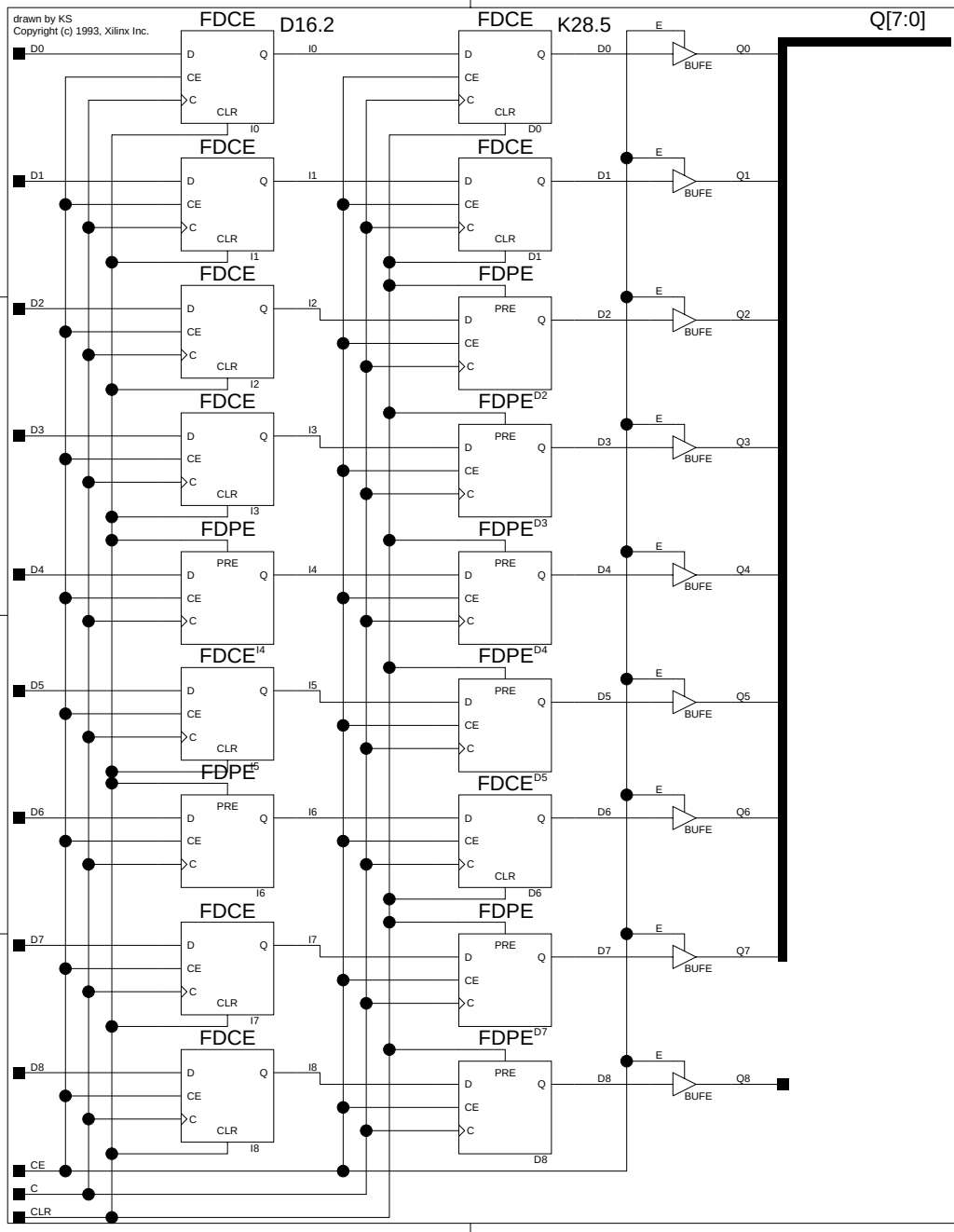
BY: JRG | PARENT PAGE: 21A | PROJECT: D785C
DATE: 1-26-2005_11:50 | FILE: STATECTL . 3 | PAGE: 24B



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: JTAG Control Signals
DDU Ethernet Logic
CMS CSC Electronics

BY: JRG
PARENT PAGE: 21A
DATE: 5-25-2005_15:01
PROJECT: D785C
FILE: STATECTL . 4
PAGE: 24C

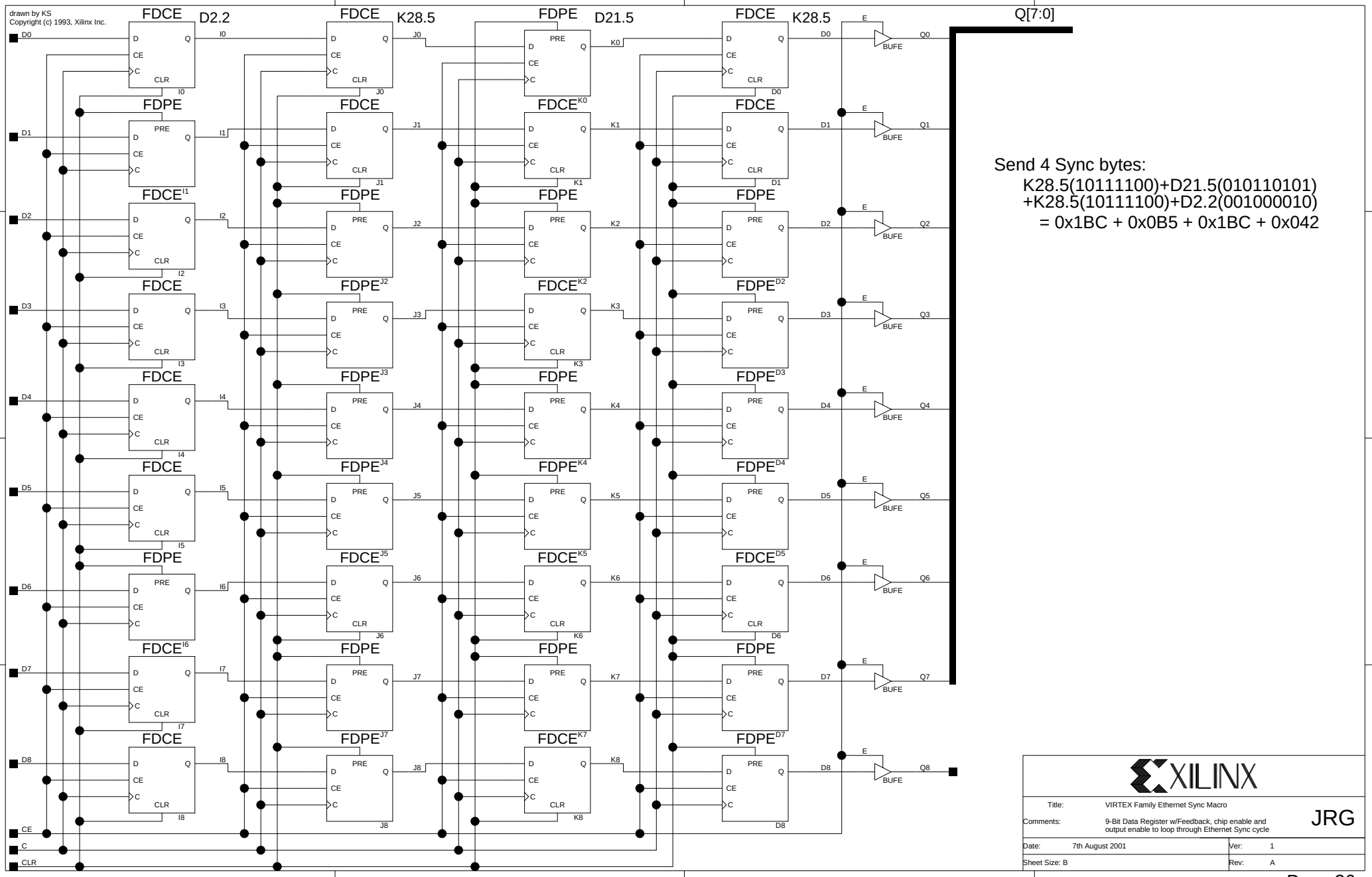


Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050

XILINX

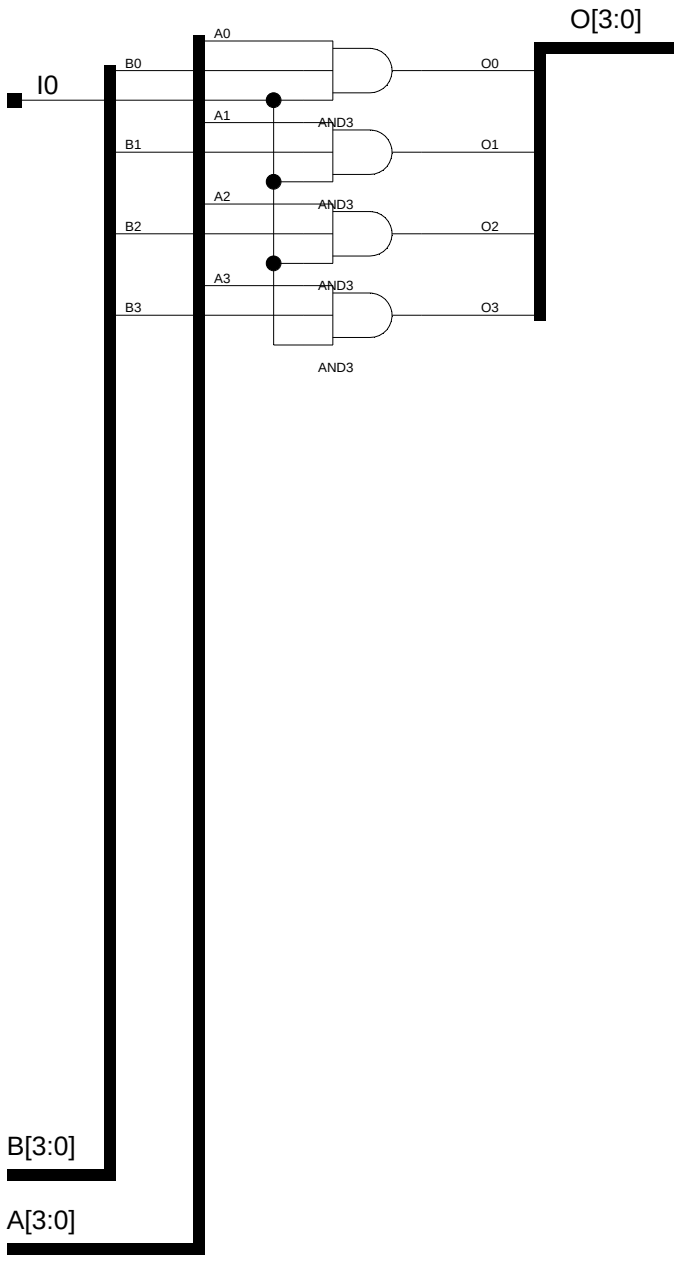
Title:	VIRTEX Family Ethernet Idle Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



Send 4 Sync bytes:

K28.5(10111100)+D21.5(010110101)
+K28.5(10111100)+D2.2(001000010)
= 0x1BC + 0x0B5 + 0x1BC + 0x042

Title:	VIRTEX Family Ethernet Sync Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Sync cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



XILINX

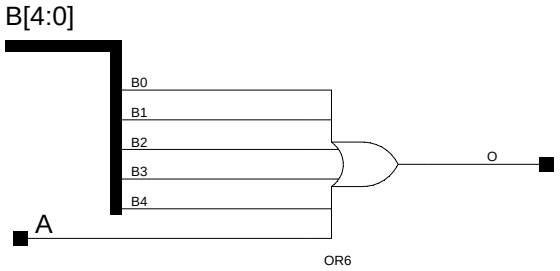
Title:VIRTEX Family 4-AND3COM1 Macro

Comments: 4-AND3 Bus Gate plus 1 common bit

JRG

Date:	1st October 2003	Ver:	1
Sheet Size: A		Rev:	A

drawn by KS



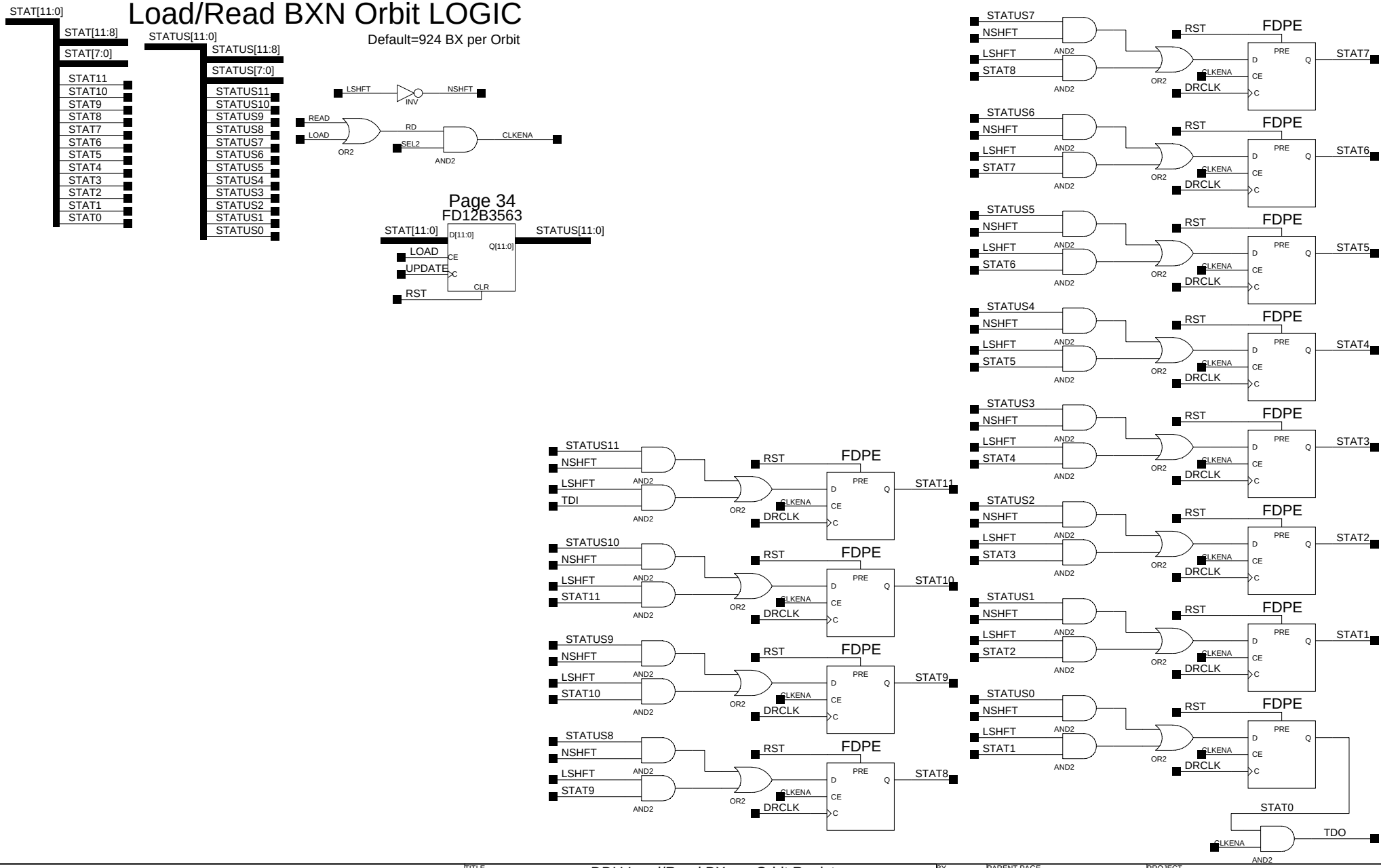
drawn by KS

XILINX

Title:	VIRTEX Family OR5+1 Macro		
Comments:	OR5 Bus Gate w/Common		JRG
Date:	27th December 2001	Ver:	1
Sheet Size: A		Rev:	A

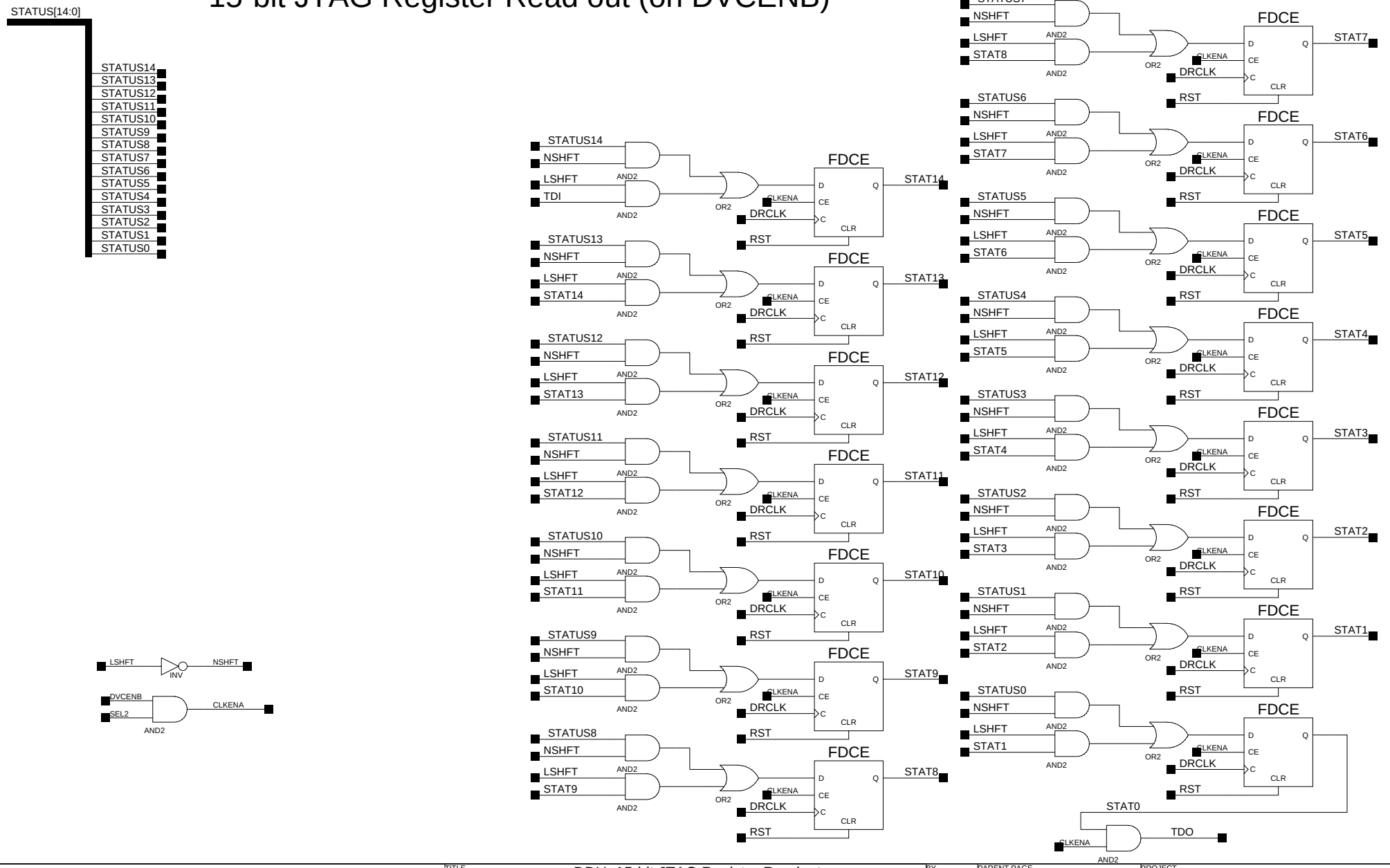
Load/Read BXN Orbit LOGIC

Default=924 BX per Orbit



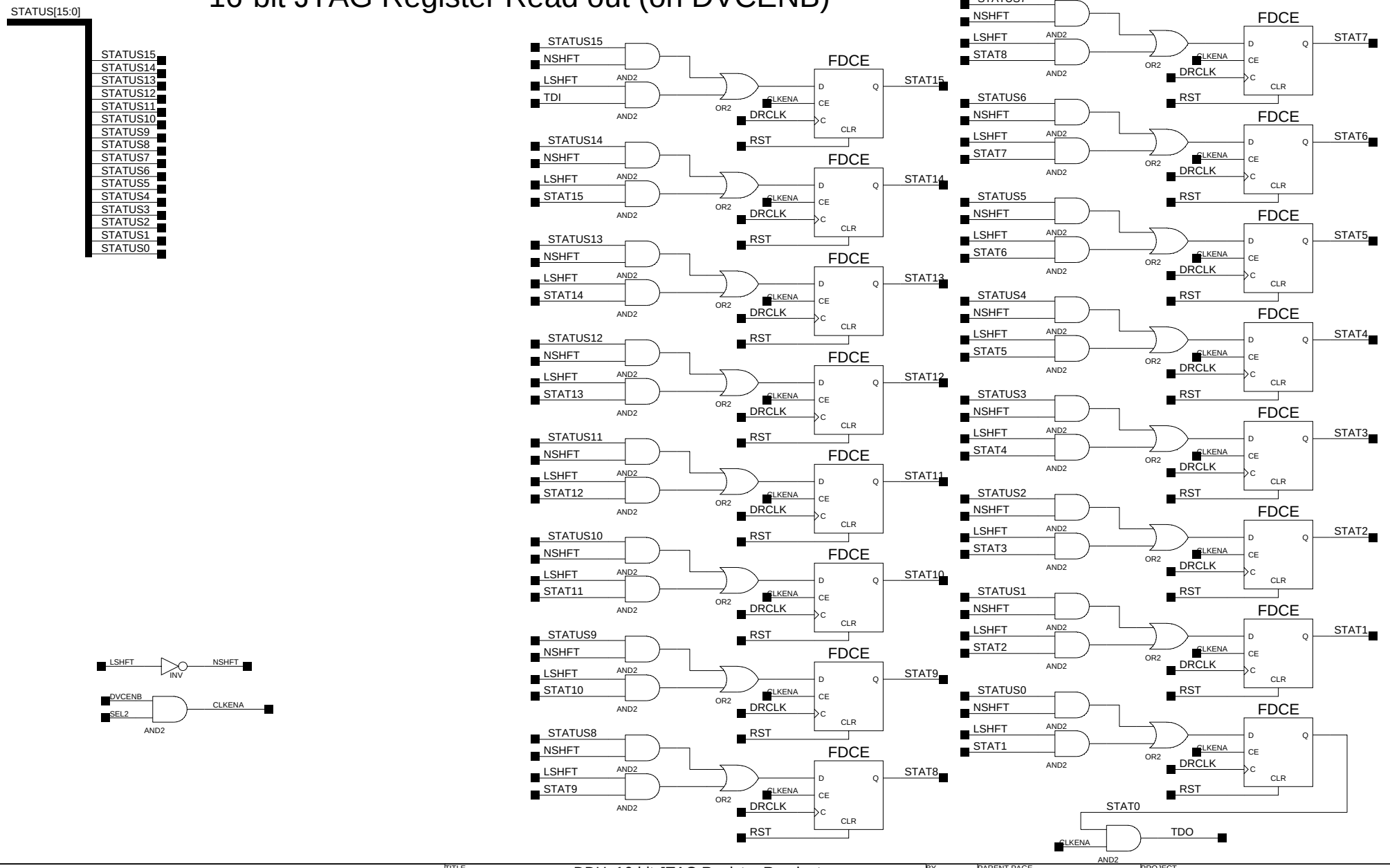
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Load/Read BX per Orbit Register DDU Controller CMS CSC Electronics	BY JRG DATE 9-19-2005_9:55	PARENT PAGE 3F FILE BXN_REG . 1	PROJECT D785C PAGE 29

15-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 15-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_15 . 1	PAGE: 31

16-bit JTAG Register Read out (on DVCENB)

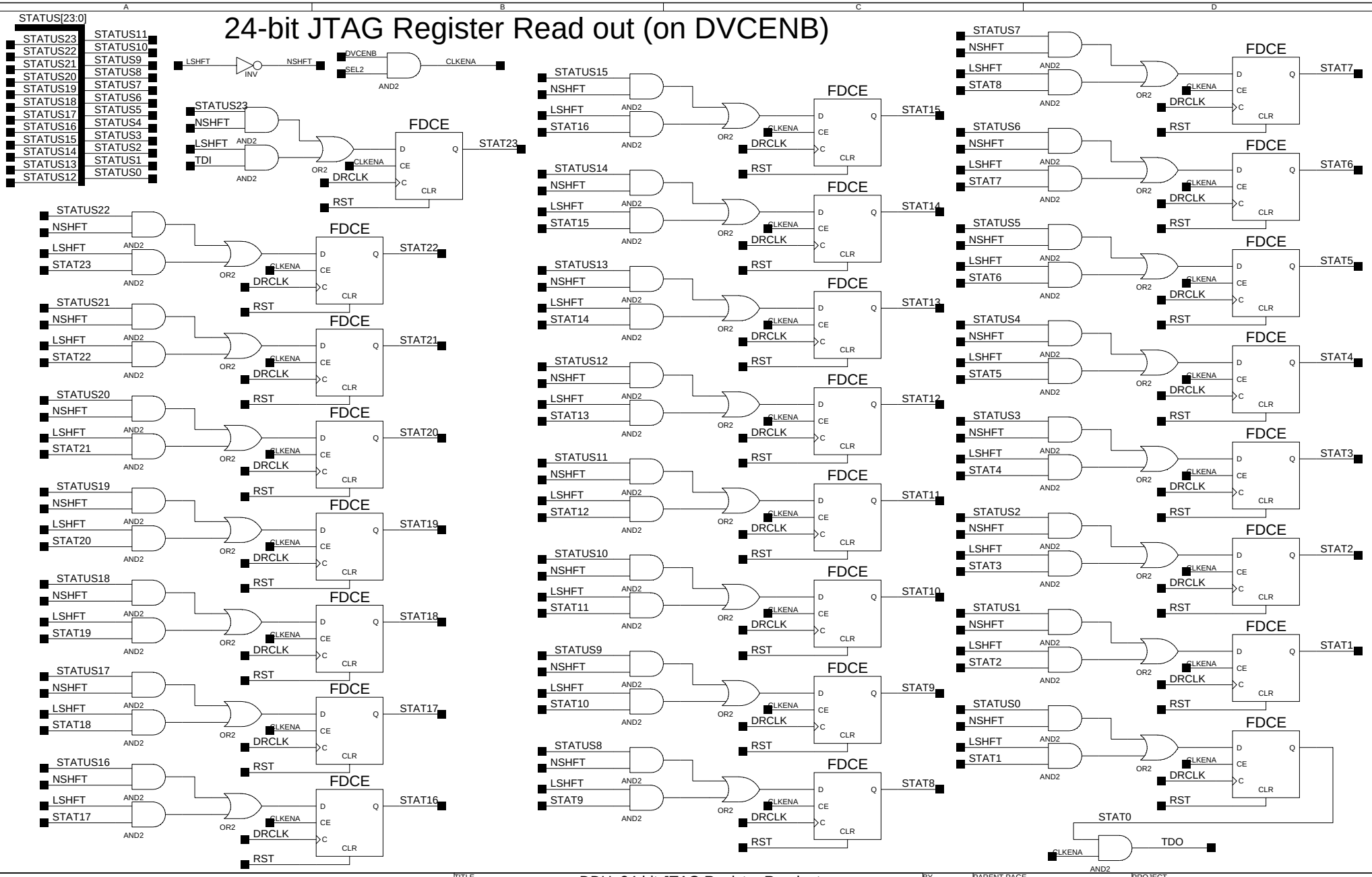


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU 16-bit JTAG Register Readout
DDU Controller
CMS CSC Electronics

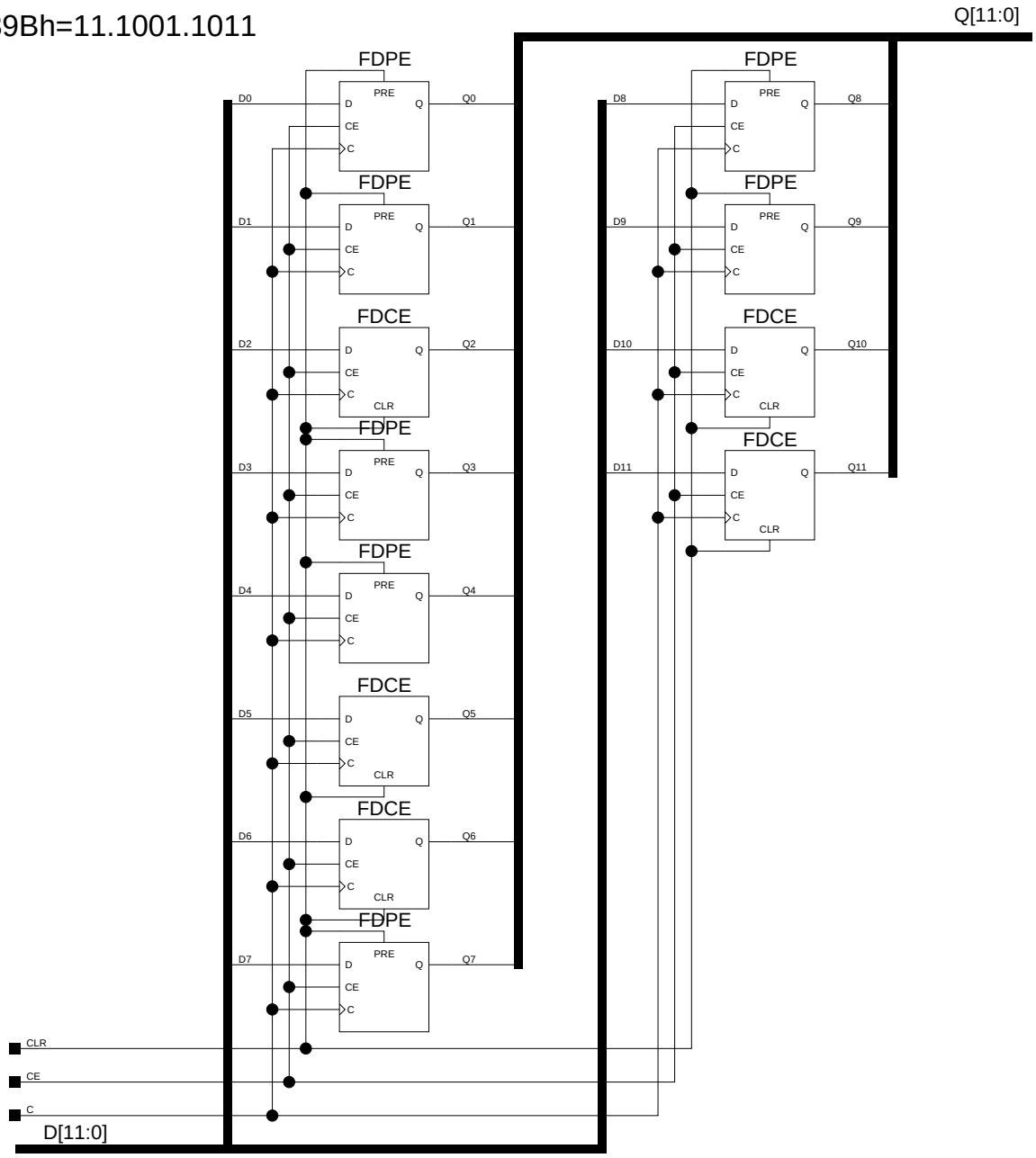
BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE	FILE	PAGE
1-26-2005_12:16	CHECK_16 . 1	32

24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:17	FILE: CHECK_24 . 1	PAGE: 33

def=923=39Bh=11.1001.1011



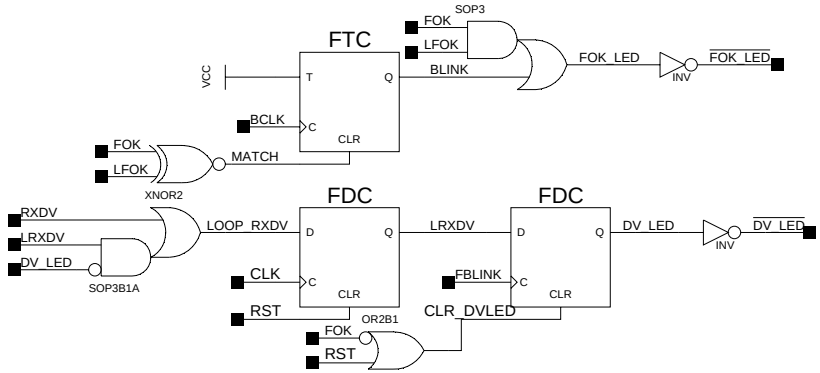
Title:	VIRTEX Family FD12b923 Macro		
Comments:	12-Bit D Flip-Flop with Preset to 923d and Enable	JRG	
Date:	8th May 2003	Ver:	1
Sheet Size: B		Rev:	A

FOK LED

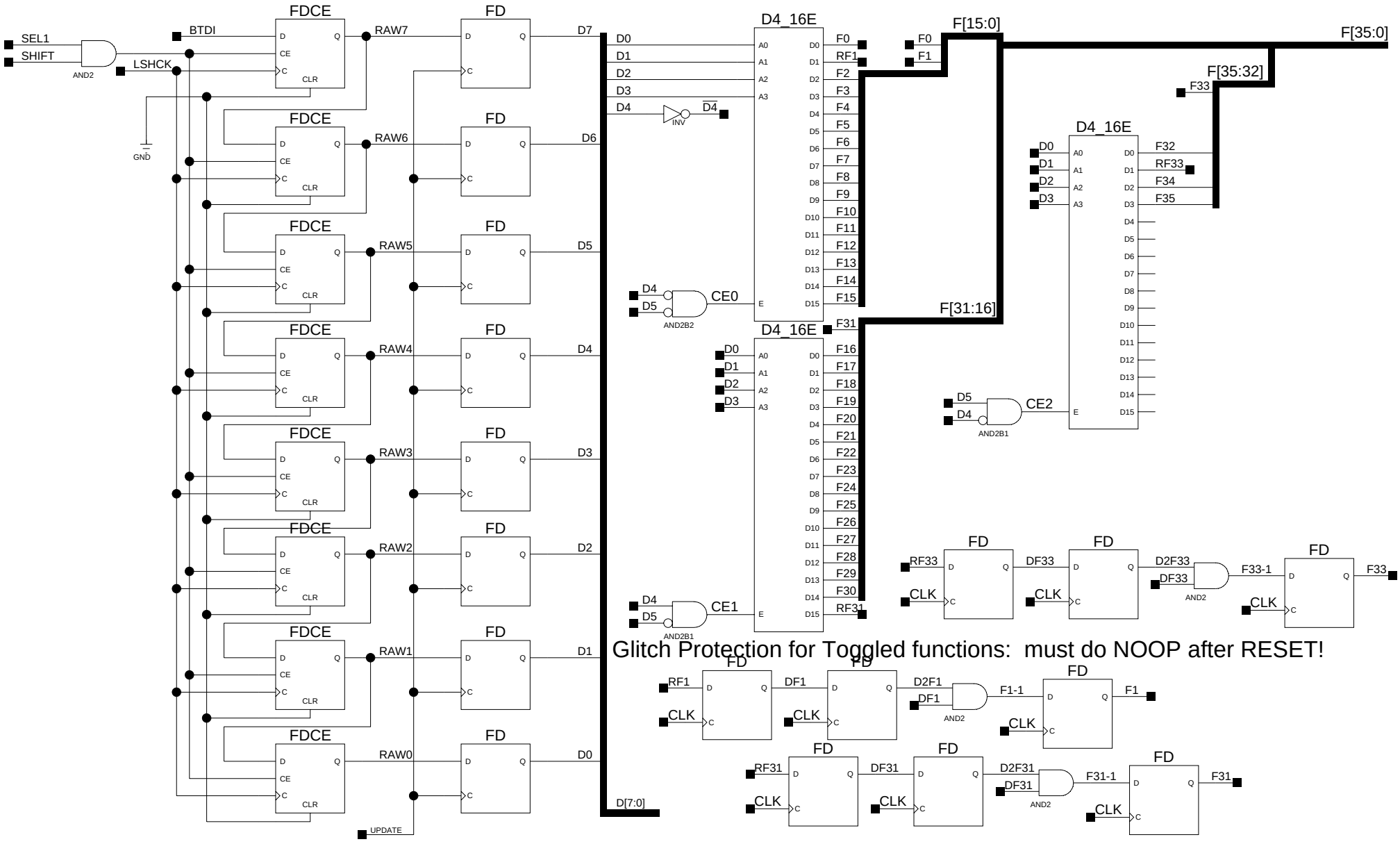
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED

--LIT == Active Data Xmit
--OFF == No data to Xmit

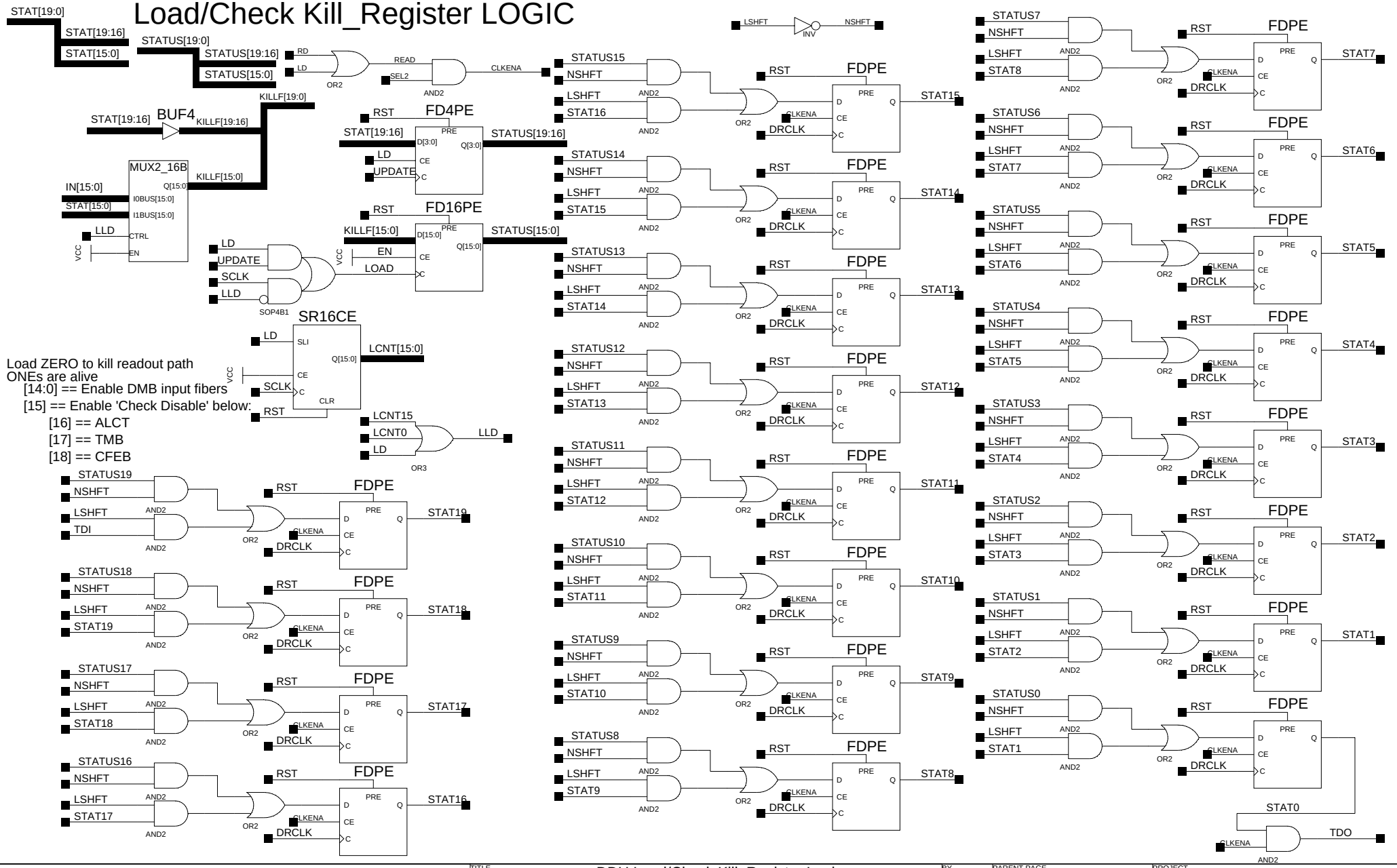


XILINX			JRG
Title:	FIBERLED		
Comments:	Custom LED Slow-Blink Control for Fiber Inputs		
Date:	27th January 2004	Ver:	1
Sheet Size: B		Rev:	A

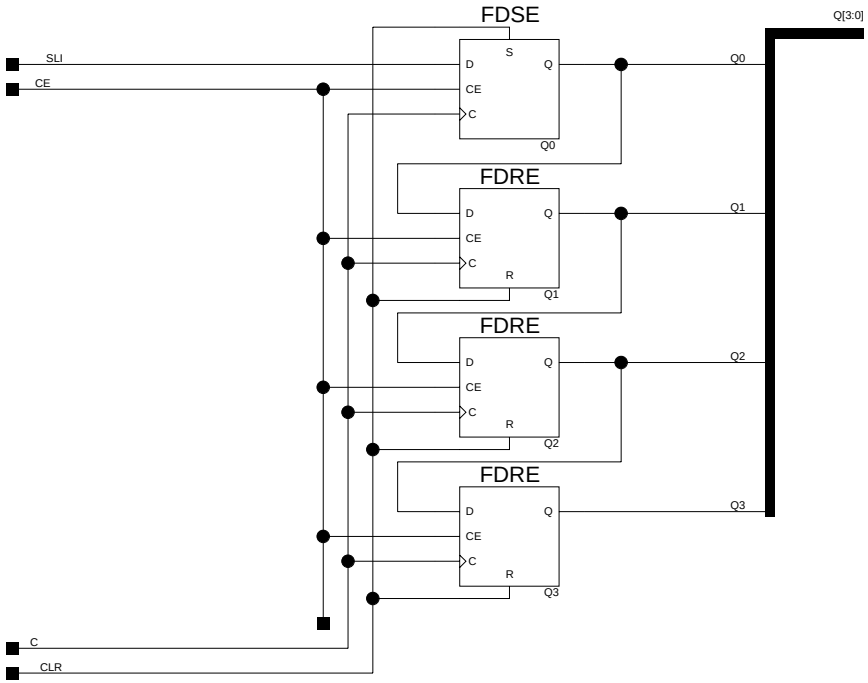


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Instruction Decode DDU Controller CMS CSC ELECTRONICS	BY: JRG PARENT PAGE: 3D DATE: 1-26-2005_12:19	PROJECT: D785C FILE: INSTRGDC . 1 PAGE: 36

Load/Check Kill_Register LOGIC



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	DDU Load/Check Kill_Register Logic DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3D	PROJECT D785C
			DATE 8-17-2005_14:06	FILE KILL_REG . 1	PAGE 37



drawn by KS

XILINX

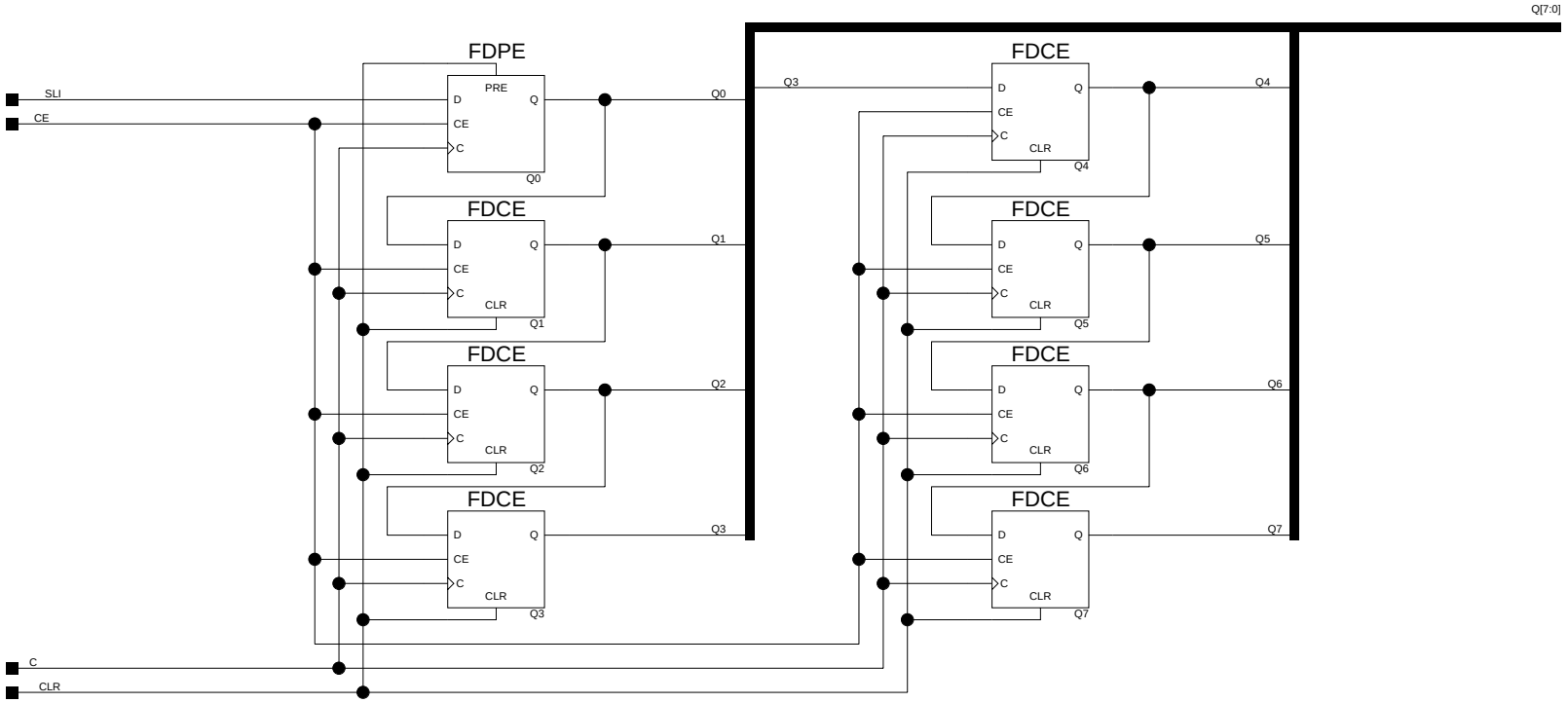
Title: VIRTEX Family SR4CE Macro

Comments: 4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset

JRG

Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A



drawn by KS

XILINX

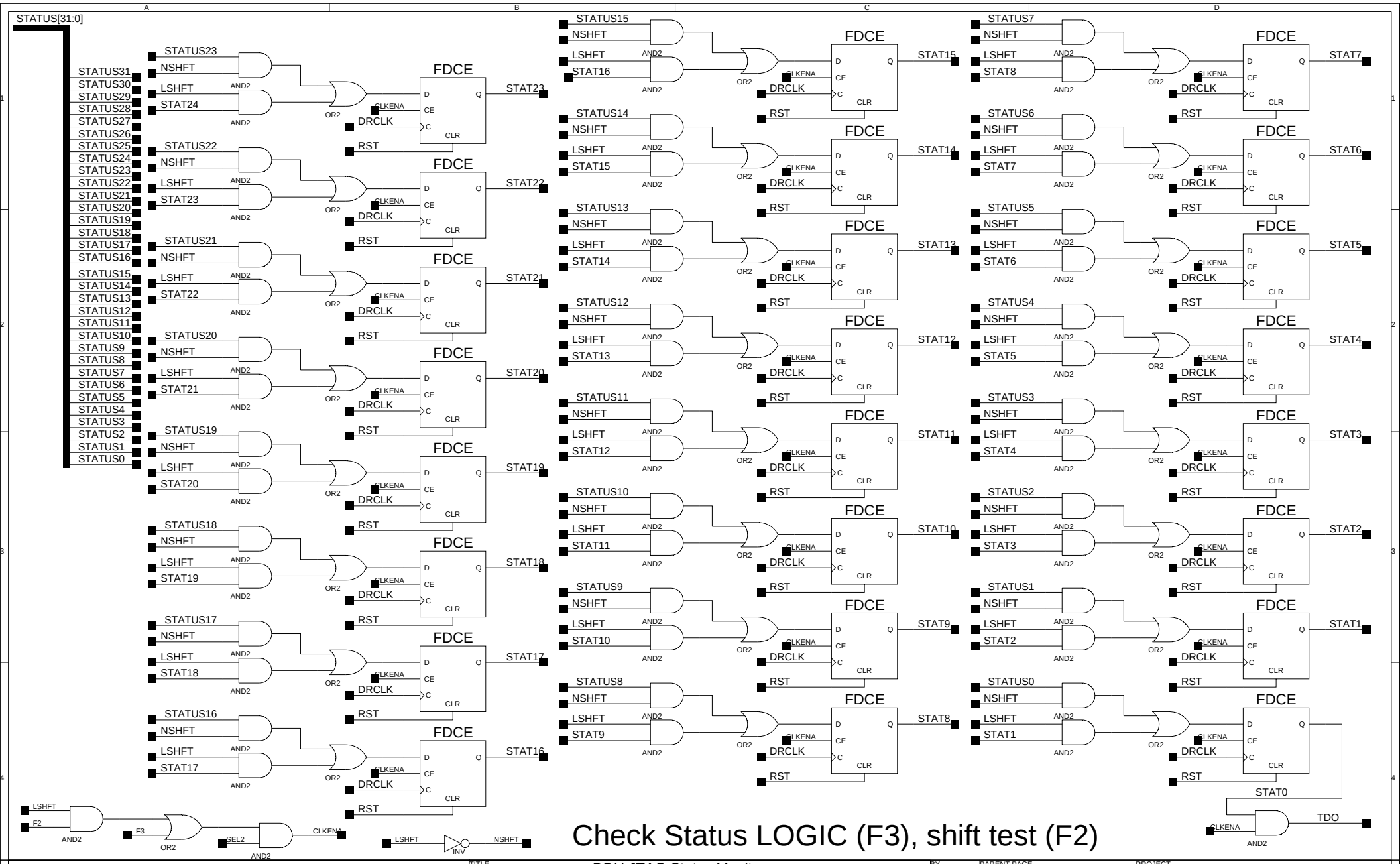
Title: VIRTEX Family SR8CE Macro

Comments: 8-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single one on Async Clr

JRG

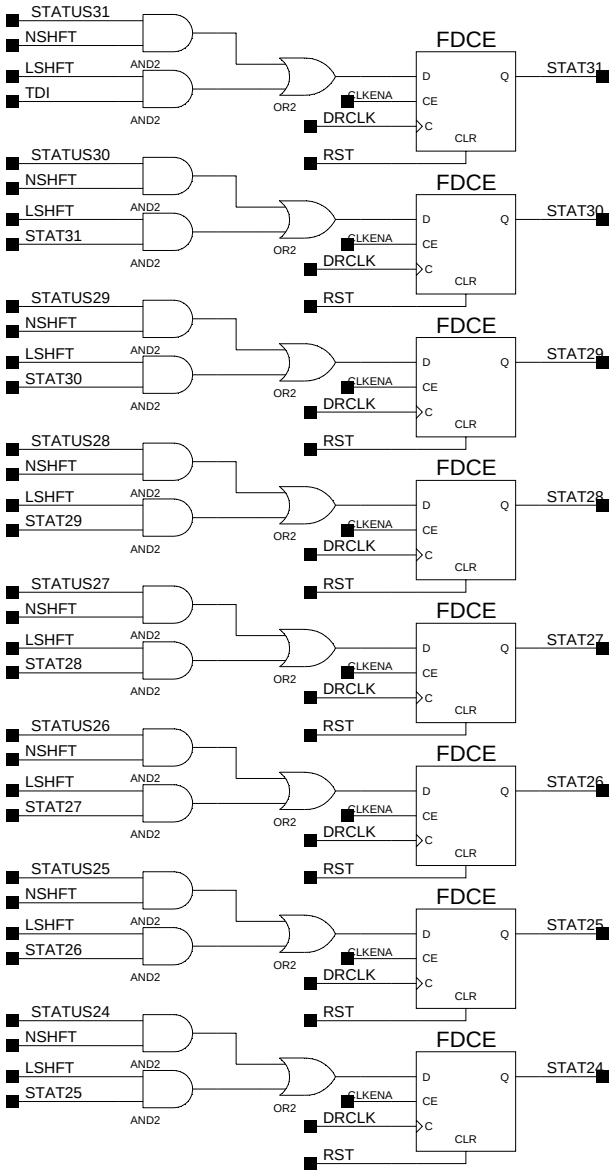
Date: 7th August 2001 | Ver: 1

Sheet Size: B | Rev: A



Check Status LOGIC (F3), shift test (F2)

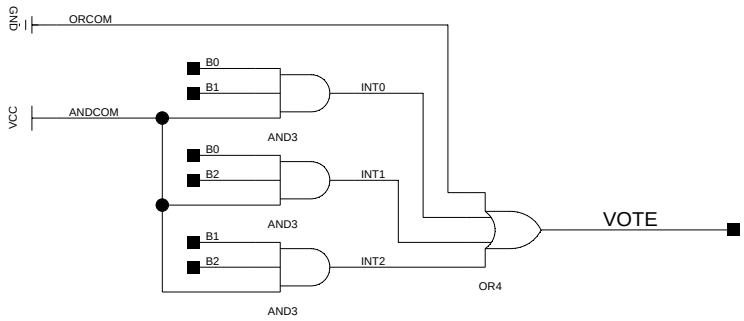
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D
		DATE: 1-26-2005_12:27	PROJECT: D785C
		FILE: STAT_MON . 1	PAGE: 40



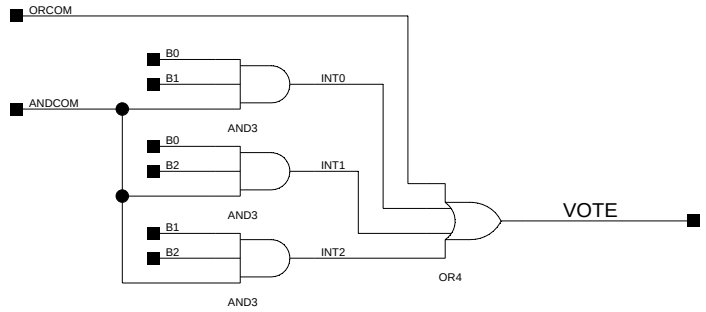
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 3D | PROJECT: D785C
DATE: 1-26-2005_12:27 | FILE: STAT_MON . 2 | PAGE: 40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Vote 2 out of 3 DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 12C	PROJECT D785C
		DATE 1-26-2005_12:28	FILE VOTE3 . 1	PAGE 41



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: ? DATE: 7-18-2005_16:56	PROJECT: D785C FILE: VOTE3P . 1 PAGE: 42