DDU5CTRL (file 0dductrl)

10-3-2006_15:37
CF038A02 Version 38

CMS CSC DDU5, Central Control FPGA

v33: change SourceID=760=2F8h for TF-DDU
v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!**
v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic
r2, removed redundant RdyIn2 requirement for SEN bits
r3-4, OSyncRst on ~Clk40, tune OFIFO Mon, req. VMEctrv17+ & InCtrlv22r3+
v36: non-TF DDUs have SrcID==BrdID, NoLiveFibers will now readout on L1A
v36-r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFDMB
v37: diagnostic changes....Tune DMBL1err(notALCTerr), BadCtrl(notMissTrg), LIE(addMissTrg), DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to on Era15, XtraTrgTrails on Erc5+13,DDUfmm 3-bits held Reset until SystemRdy
v37r2-3: tune CfebL1aErr/SyncErr &DMBcritErr logic, MultL1err logic, InSingWarn=Era10,ValidDMBfull=Erb0,DMBtimeout=Era15
v38: DMBcritErr=Erc7, improve Htmb/alct timing,C-codeErr goes to InMxmitReg, InTimeout goes to EndTimeBusyReg
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFOb15, LDMB_CRCok held at least 4 cycles

DDUCNTRL

Set All I/O to 3.3V

PART=XC2VP7-6-FF672

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5ctrl\DDU5ctrl\ddu5ctrl
C038DD99
C138DD99

PromID: 05026093h
FPGAid: 2124A093h

PROGRAM takes < 55 ms (31ms this FPGA)

1: Mode Bit 0 LED0 on top, pins on away-side from LEDs
2: Mode Bit 1 RST_1=Asynchronus Reset for FPGA1 and ALL FIFOs
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GbE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/CMD if SW8 is off
8: FPGA version on LEDs

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DDU Format Since DDUctrl v15:

BOE1 type L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK

49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH

LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000

DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP

EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

mojo

DDU5CTRL -- Project History

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits
Last w/DDU_FOV=4 --->> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Klll option
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VMEctrl
v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV=5
v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 bytes
v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--->rev2: SLOW8
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_Stat
v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDDR
Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisable,
Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/1
v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critical)
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB
v27: tune CFEB_L1er, 8/16 sample flag, WarnMon & BX offset
v28: add Big debug reg. on F21, Timeout reg. on F28, uses LnextFIFO, replace
LLLREN w/LFOE for TimeoutReg, make ERA-St/End-TO perm.
v29: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L1A
v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logic
v31: tune CFEB-DAV check (OR DAVs from DMB Hdr1 & Hdr2),
add SP/TF compatibility & diagnostic logic
v32: change CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4),
modified ERR13 for Permanent DDU_DLL_err, add DDU CSC-Board occupancy monitor-F34?
-r2: add zeroing logic at RST for Occ.Mon. -r3: fix LRST logic

Default Startup Order:

Release DLL (no wait)
4) DONE
5) En. Outputs
6) Release WE

CSC_L1Err <--Bring to VME-JTAG Reg?

TST	Clock	BUFGMUX	
0P	drck1	5P *4P	-TR
2P	2clk	5S *1S	
3S	clk	7S *7S	
0S	clk625	2S- *2S	
7P	ck125	1P *0S	-BL
5P	clk40	0S *3P	
4S-	clk156	4S- *4S	
1S	drck2	3P *5S	
6S-	sclk	6S- *6S	

* denotes LOCed position

New Ideas: Store & check DMB source IDs from each fiber?
Feed SLINK status into FMM logic (for UF).
Set DMB CRC OK flag for DDU Empty Events? no...
In case of StuckData send PRST? How to distinguish SEU? Later event still gets LostHdr or Timeout, could self-correct. Add "PRSTed" VME register to track occurrence.
In case of L1Amismatch, let it run and see if it is better a few~10 evts later. Possible to self-correct as above...? Can only work if DMB really lost event data.

To Do:
- COMPARE BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Determine correct values to store in Flash Mem
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case
- No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL
- Make Verilog module to get Fiber/DMB_RD in one CLK?
- Multiple TRG_L1err ought to request a Sync Reset?
  * Same for consecutive events with a TRG_L1err?

Check Phase of CMD to CLK40
* pg. 2G & 3I
- CFEB-DMB sync check pg. 12C
- CFEB-L1A check disabled, pg. 12D: not! Found a fix...
- options for Monitoring on pg. 3H, 12E?
- Does CFEB-Check-Disable cause TF/SP mimic?

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DDU Format Since DDUctrl v15:

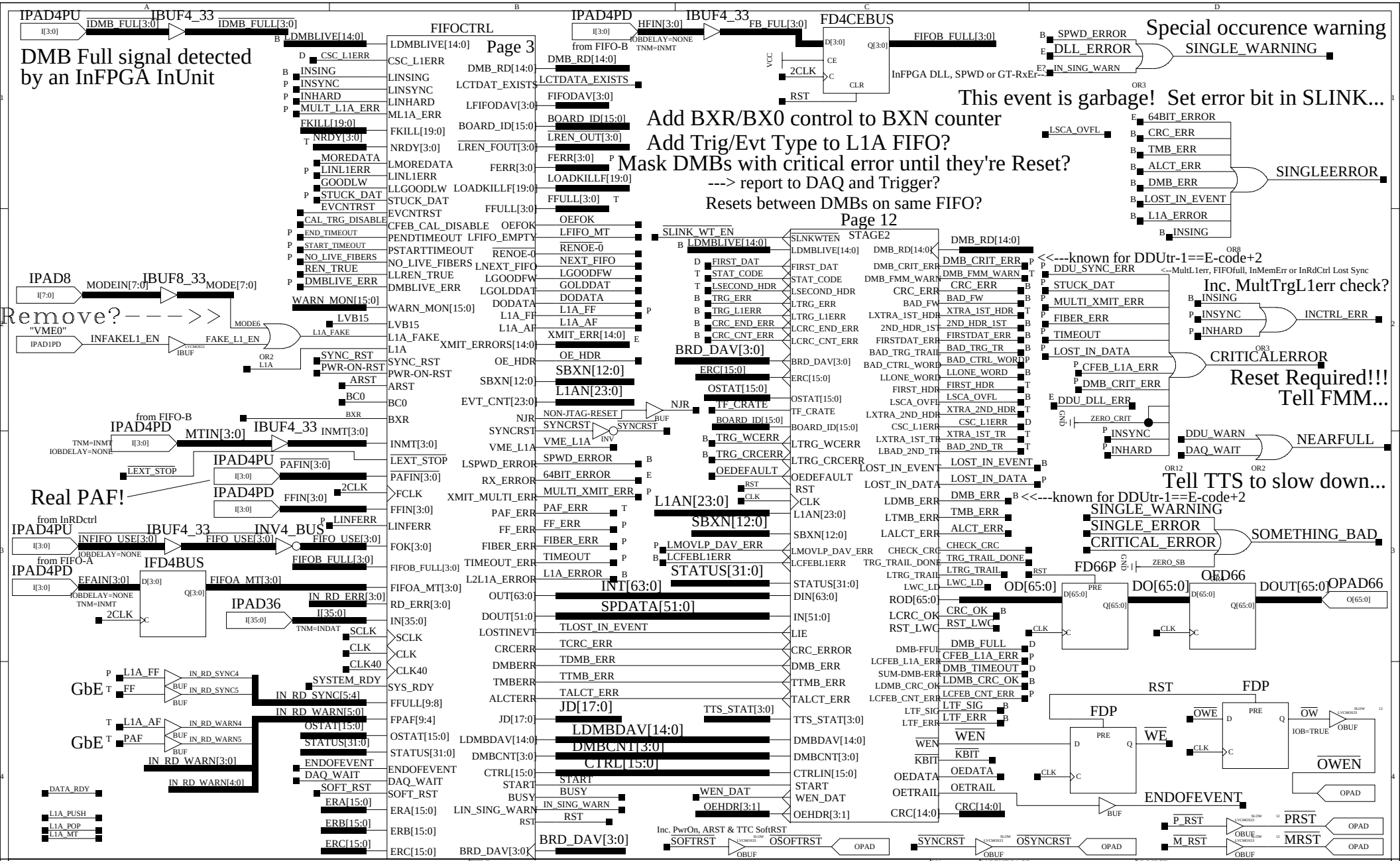
H1: 0x/5T/NN.NNNN/XXX/I.II/VK (BOE1 type, L1A Number, BXN, ID, FOV, K-Status)
H2: 0x/8000/0001/8000/HHHH (49-bit ~unique constant, DMBfull(15))
H3: 0x/LLLL/oooo/ZZZZ/GGMY (LiveDMB(15), Ostat, DMB-DAV(15), BOEstat, DMBcnt)

T-2: 0x/8000/FFFF/8000/8000 (64-bit unique constant)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP (DDU EOF Status, DMBerr, DMBwarn(15))
TR: 0x/A/?/WW.WWWW/RRRR/UUMK (EOE, WordCount, CRCword, EOEstat, K-Status)

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes

mojo


DMB Full signal detected by an InFPGA InUnit
Special occurence warning
This event is garbage! Set error bit in SLINK...
Add BXR/BX0 control to BXN counter
Add Trig/Evt Type to L1A FIFO?
Mask DMBs with critical error until they're Reset?
---> report to DAQ and Trigger?
Resets between DMBs on same FIFO?
Page 3
Page 12
FIFOCTRL
FD4CEBUS
STAGE2
Inc. MultTrgL1err check?
Reset Required!!! Tell FMM...
Tell TTS to slow down...
Real PAF!
Remove?
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DDU Controller Logic
CMS CSC Electronics
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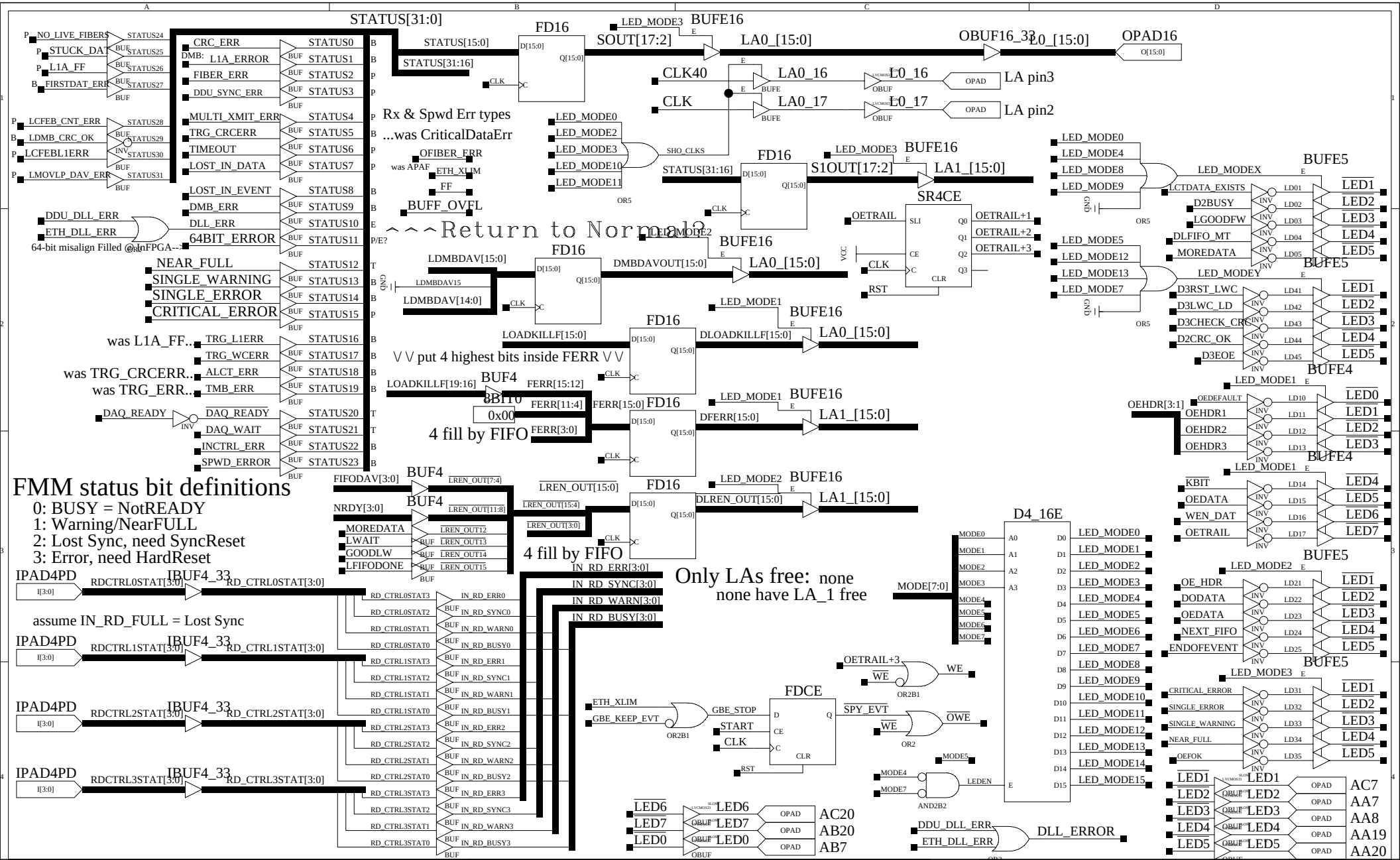
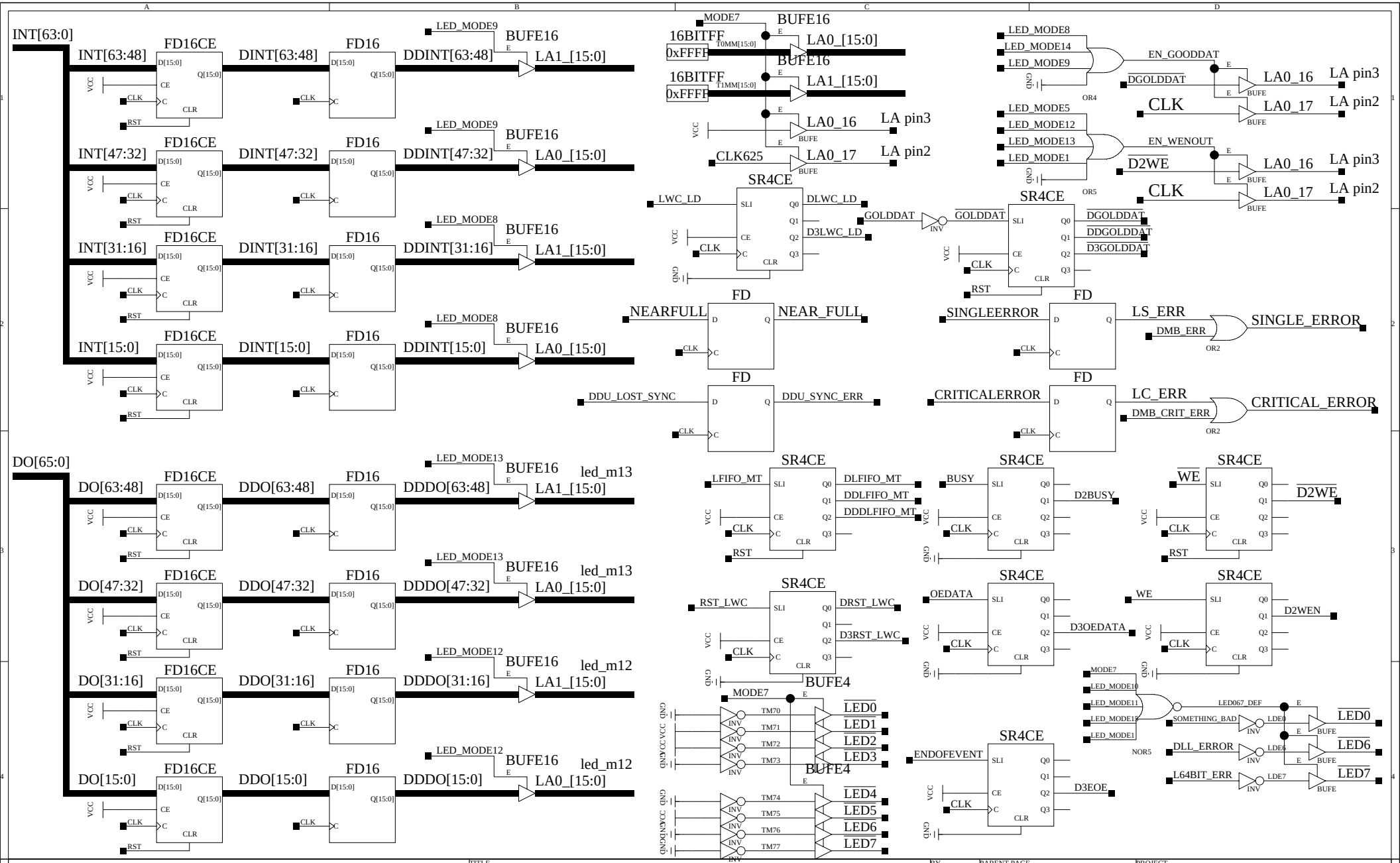
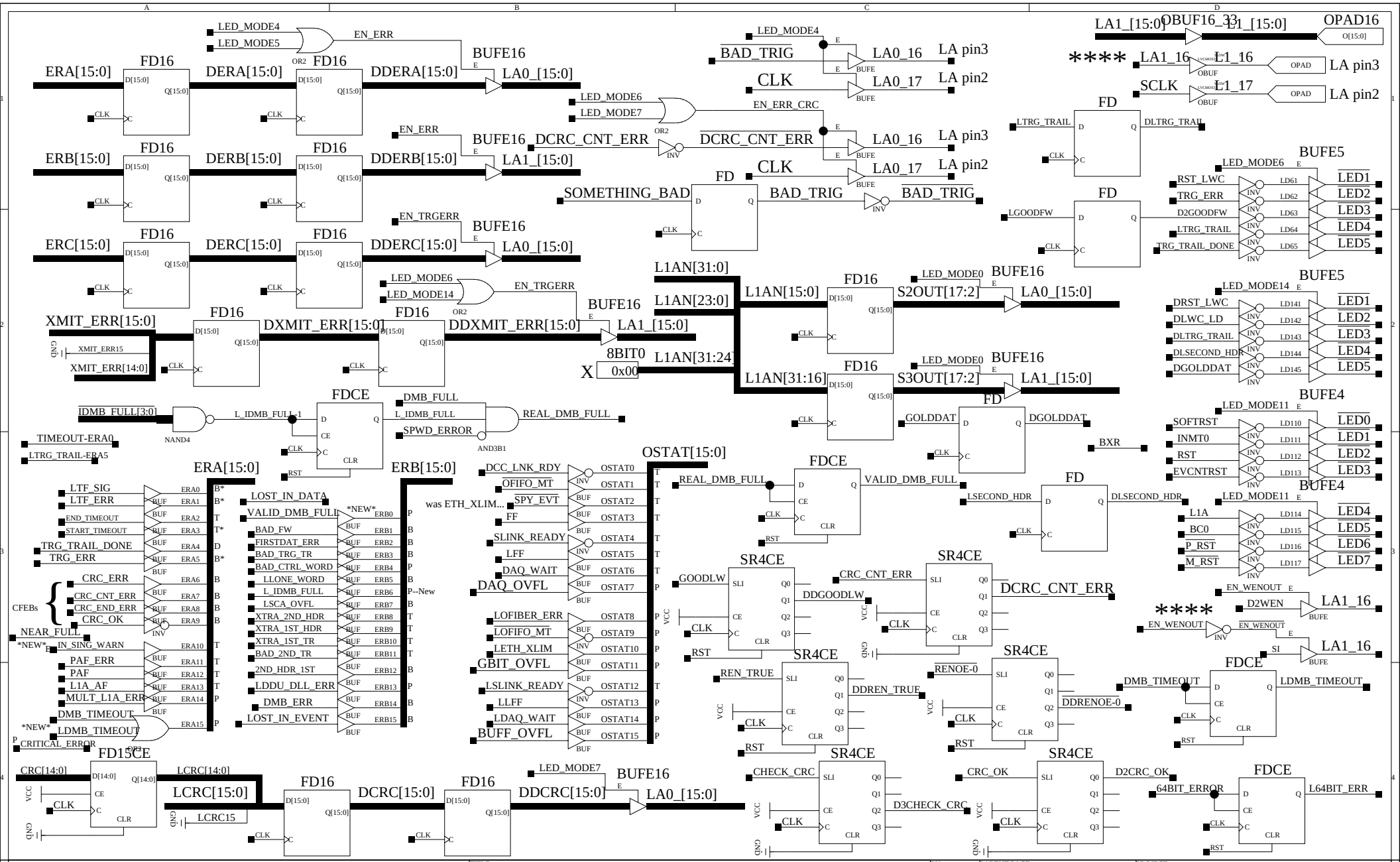
10-3-2006_11:28
D785C
DDUCNTRL . 1
2



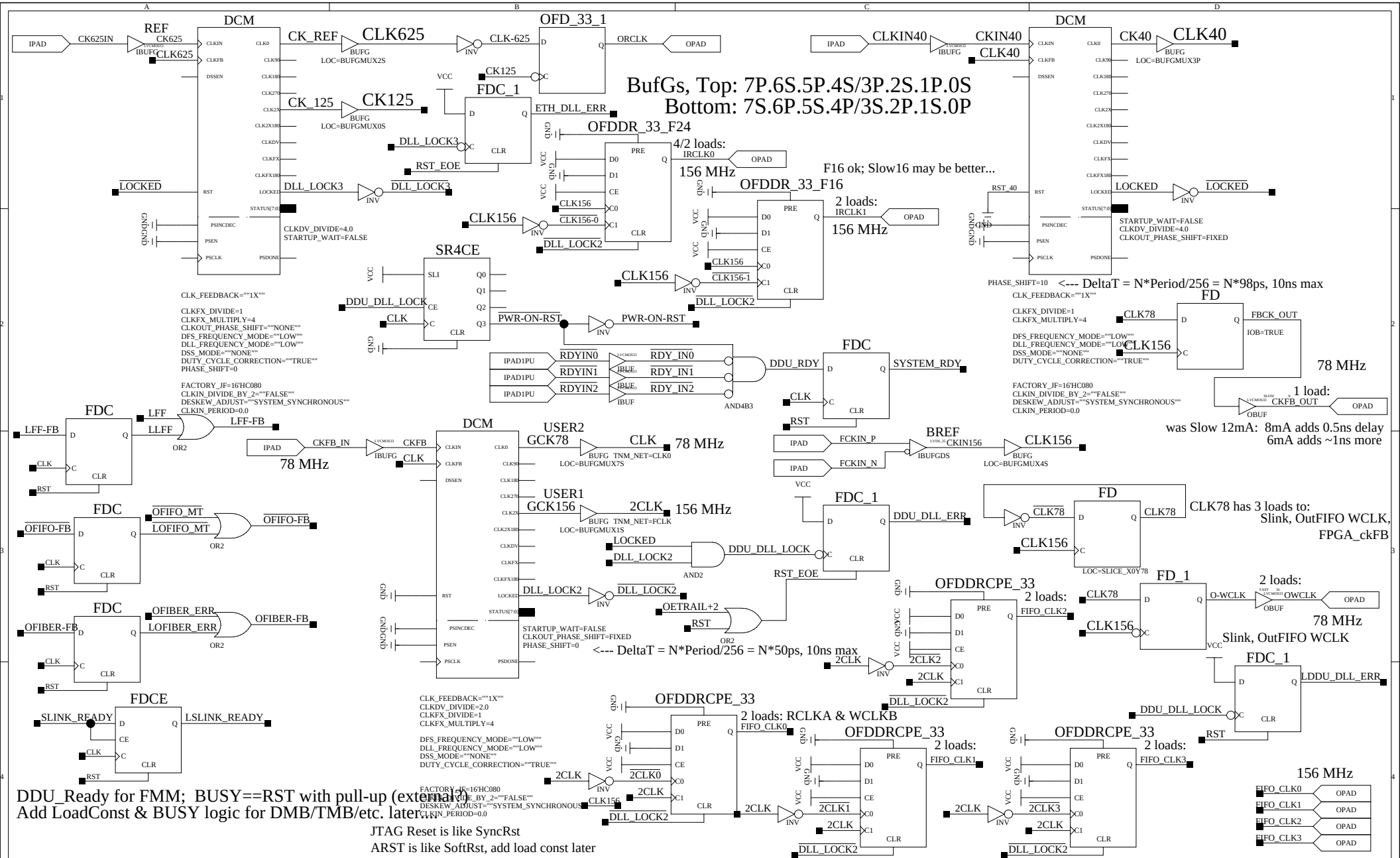
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 10-2-2006_13:46	PARENT PAGE: 1 FILE: DDUCNTRL . 2
		PROJECT: D785C	PAGE: 2A



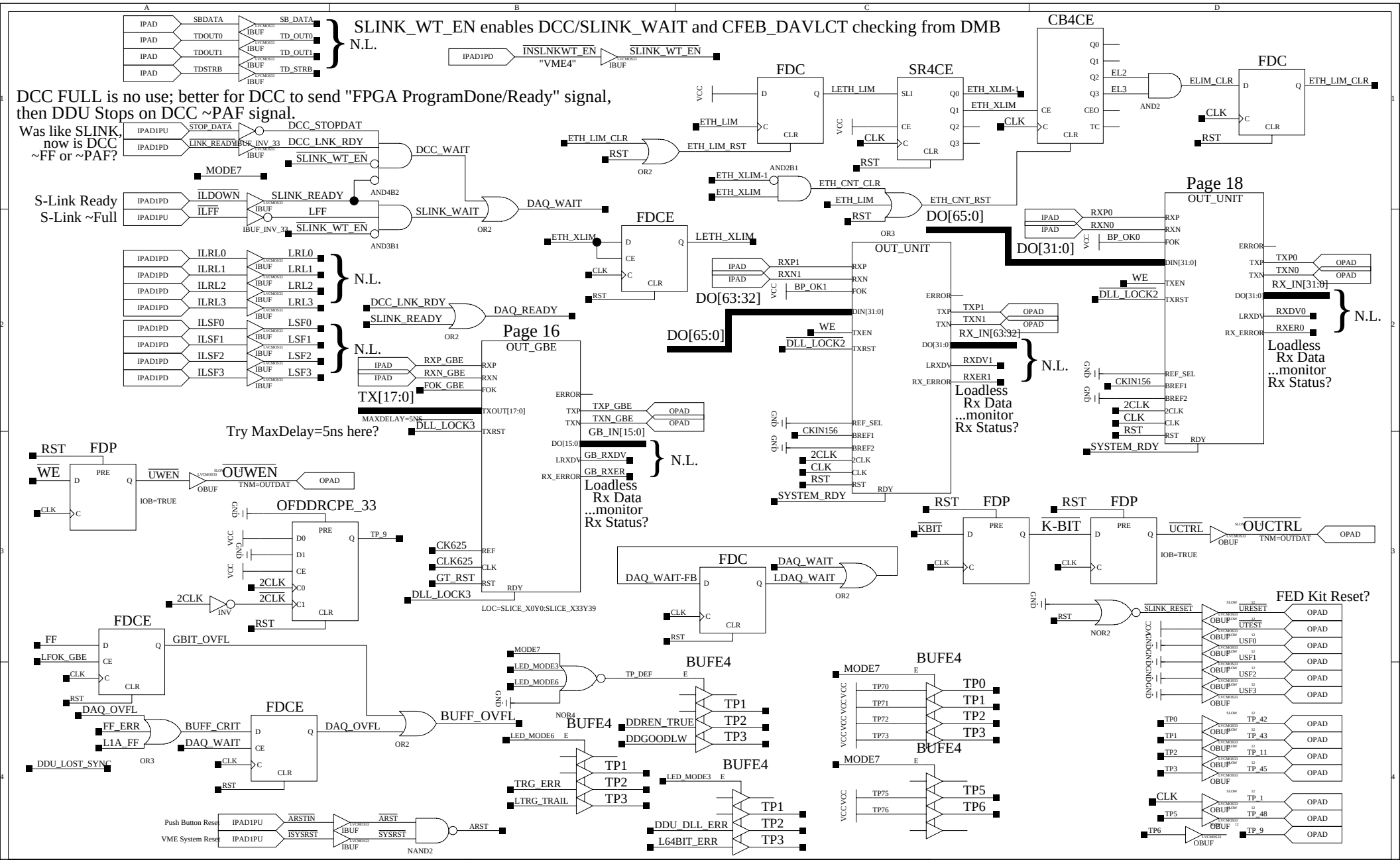
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785C
		DATE: 9-29-2006_14:51	FILE: DDUCNTRL . 3	PAGE: 2B



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 10-3-2006_10:27	PARENT PAGE: 1 FILE: DDUCNTRL . 4
		PROJECT: D785C	PAGE: 2C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785C	
		DATE: 6-1-2006_16:55	FILE: DDUCNTRL . 5	PAGE: 2D	


SLINK_WT_EN enables DCC/SLINK_WAIT and CFEB_DAVLCT checking from DMB
N.L.
DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal,
then DDU Stops on DCC ~PAF signal.
Was like SLINK,
now is DCC
~FF or ~PAF?
S-Link Ready
S-Link ~Full
Try MaxDelay=5ns here?
Page 16
Page 18
Loadless
Rx Data
...monitor
Rx Status?
FED Kit Reset?
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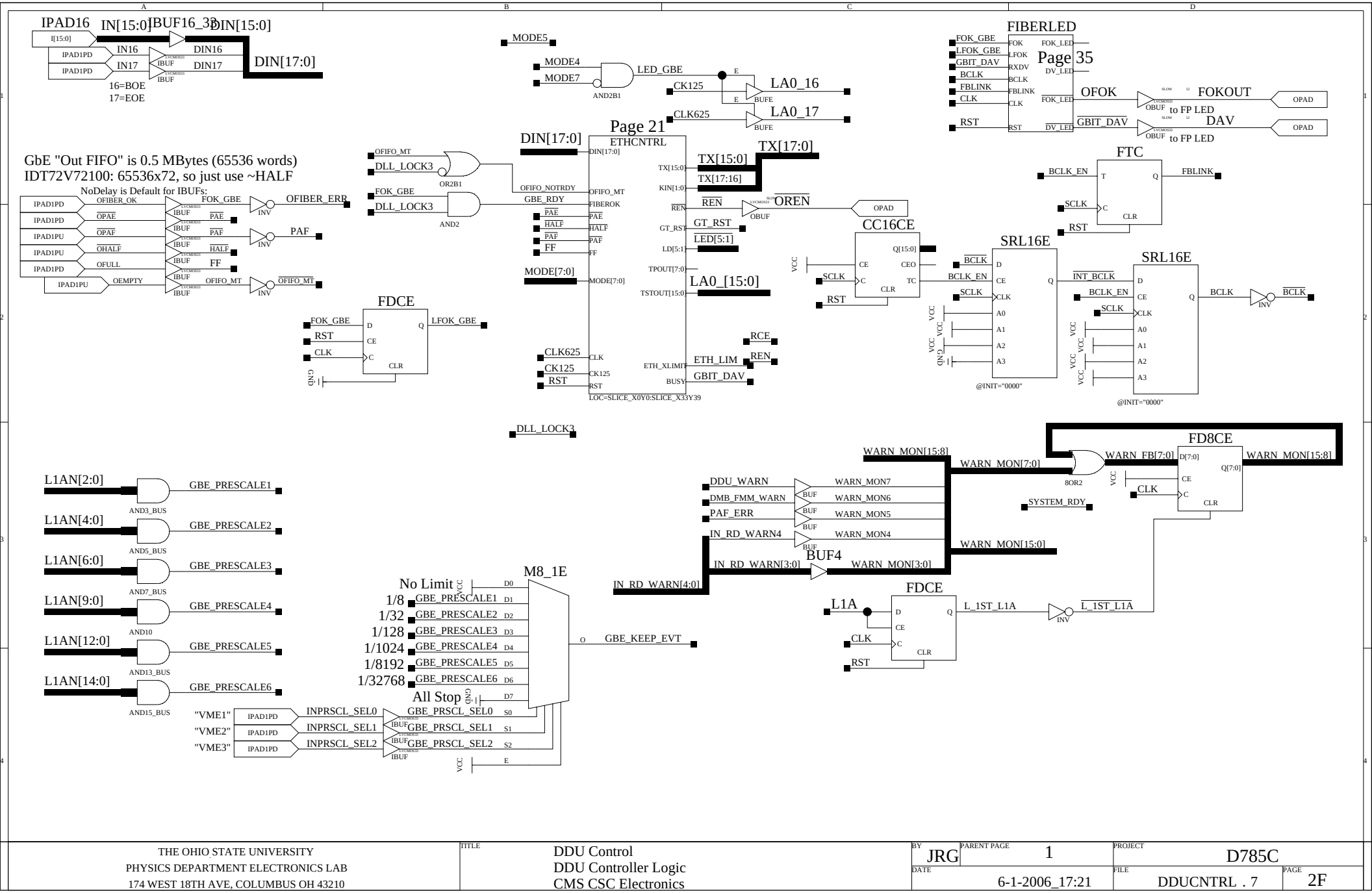
DDU Controller Logic
CMS CSC Electronics
JRG
1
D785C
9-29-2006_14:51
DDUCNTRL . 6
2E



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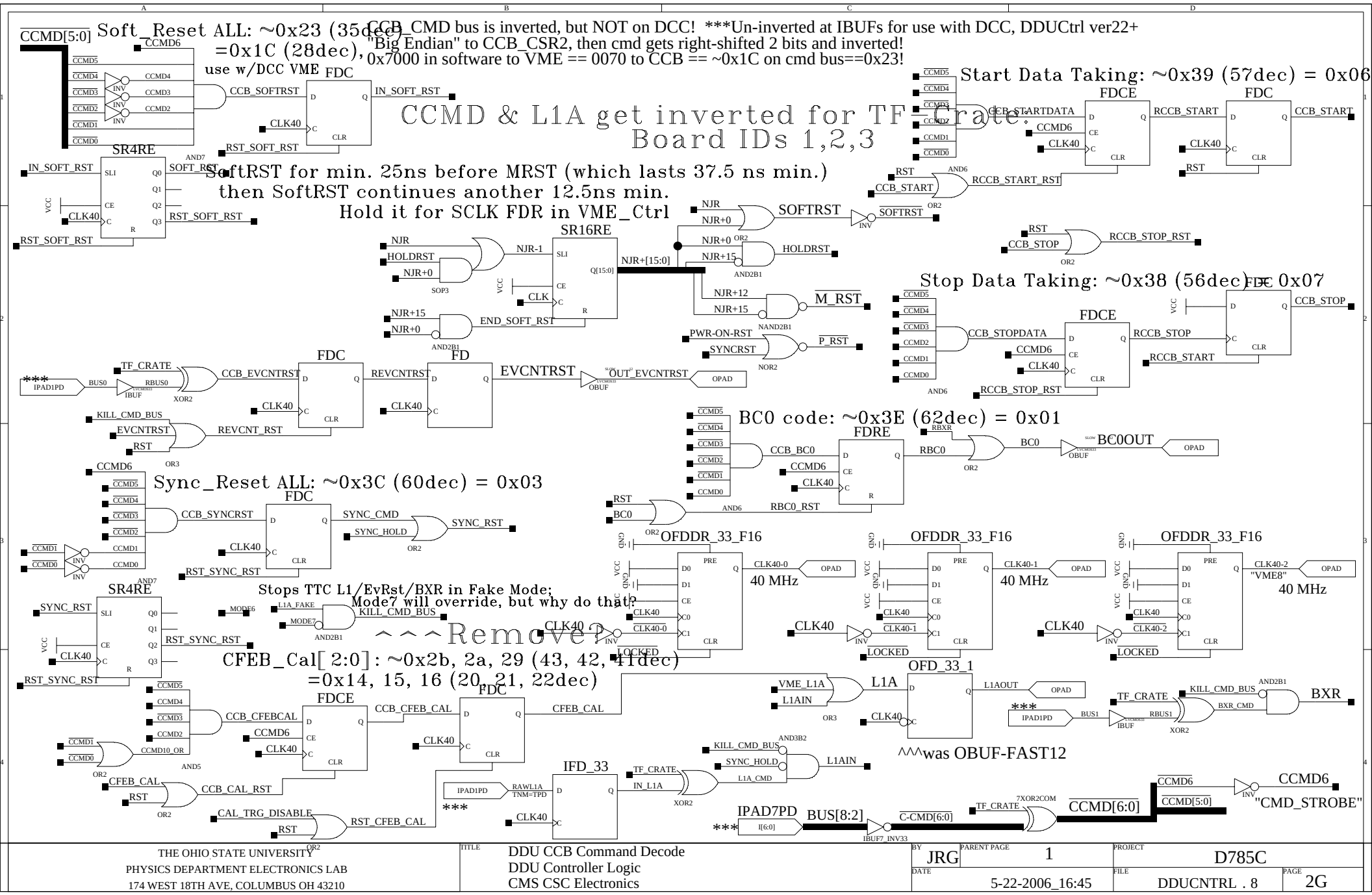
		DATE: 6-1-2006_17:21	FILE: DDUCNTRL . 7	PAGE: 2F


CCMD[5:0]
Soft_Reset ALL: ~0x23 (35dec) =0x1C (28dec), use w/DCC VME
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
"Big Endian" to CCB_CSR2, then cmd gets right-shifted 2 bits and inverted!
0x7000 in software to VME == 0070 to CCB == ~0x1C on cmd bus==0x23!
CCMD & L1A get inverted for TF Crate.
Board IDs 1,2,3
Start Data Taking: ~0x39 (57dec) = 0x06
SoftRST for min. 25ns before MRST (which lasts 37.5 ns min.)
then SoftRST continues another 12.5ns min.
Hold it for SCLK FDR in VME_Ctrl
Stop Data Taking: ~0x38 (56dec) = 0x07
BC0 code: ~0x3E (62dec) = 0x01
Sync_Reset ALL: ~0x3C (60dec) = 0x03
Stops TTC L1/EvRst/BXR in Fake Mode;
Mode7 will override, but why do that?
^^^Remove?
CFEB_Cal[2:0]: ~0x2b, 2a, 29 (43, 42, 41dec) =0x14, 15, 16 (20, 21, 22dec)
^^^was OBUF-FAST12
40 MHz
"VME8"
"CMD_STROBE"
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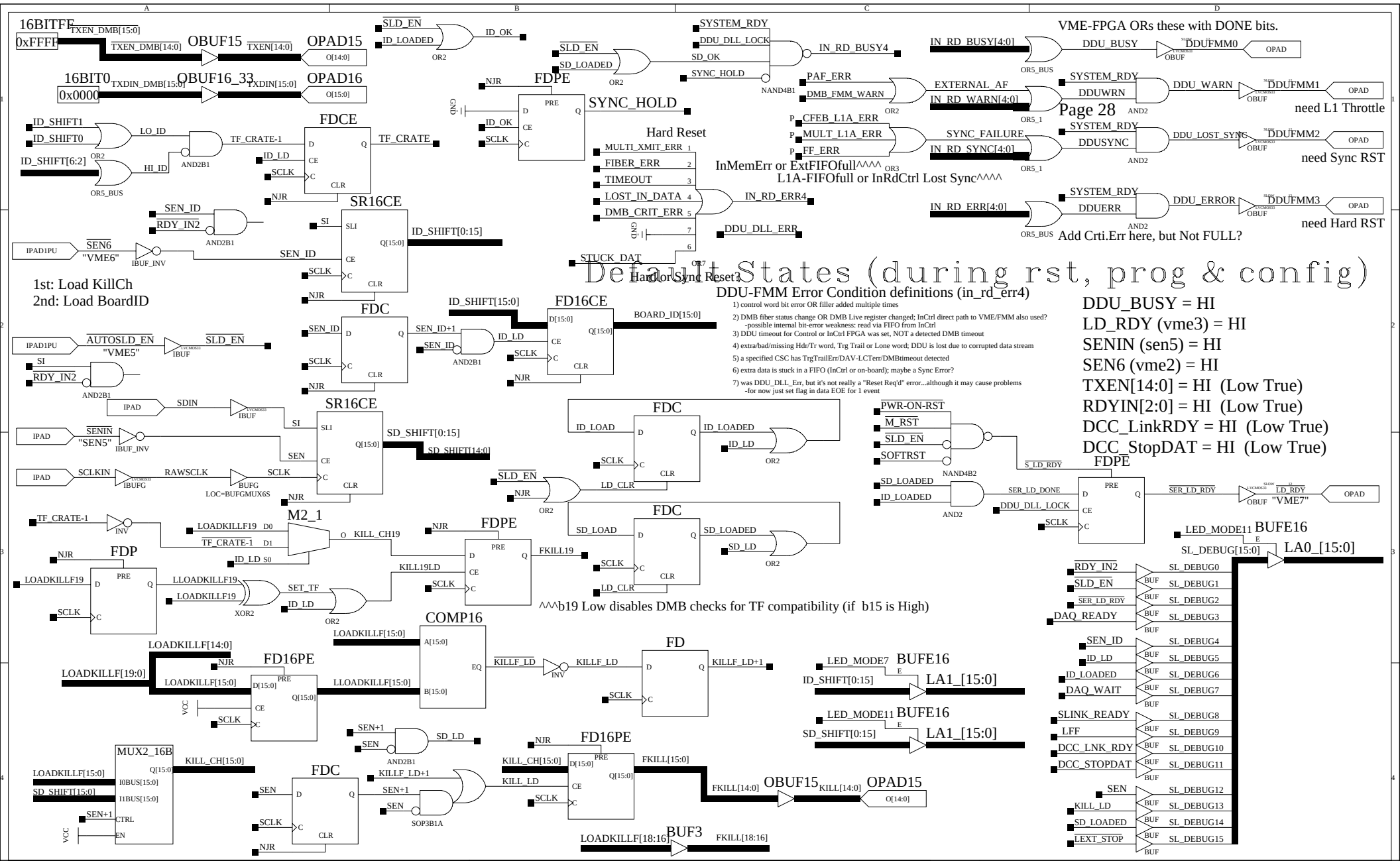
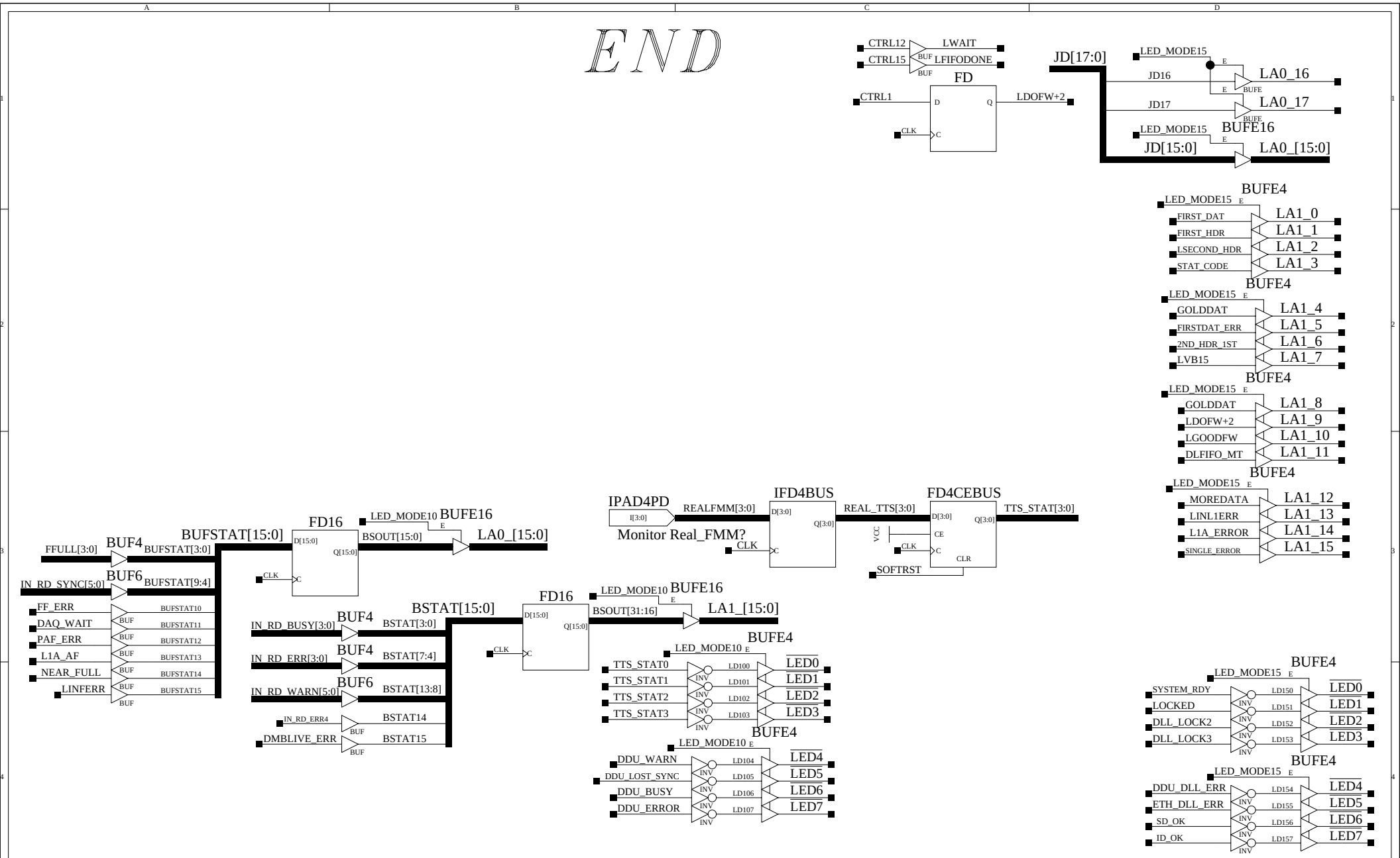
TITLE
DDU CCB Command Decode
DDU Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 1
PROJECT D785C
DATE 5-22-2006_16:45
FILE DDUCNTRL . 8
PAGE 2G



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Control DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 1	PROJECT D785C
		DATE 9-13-2006_17:20	FILE DDUCNTRL . 9	PAGE 2H



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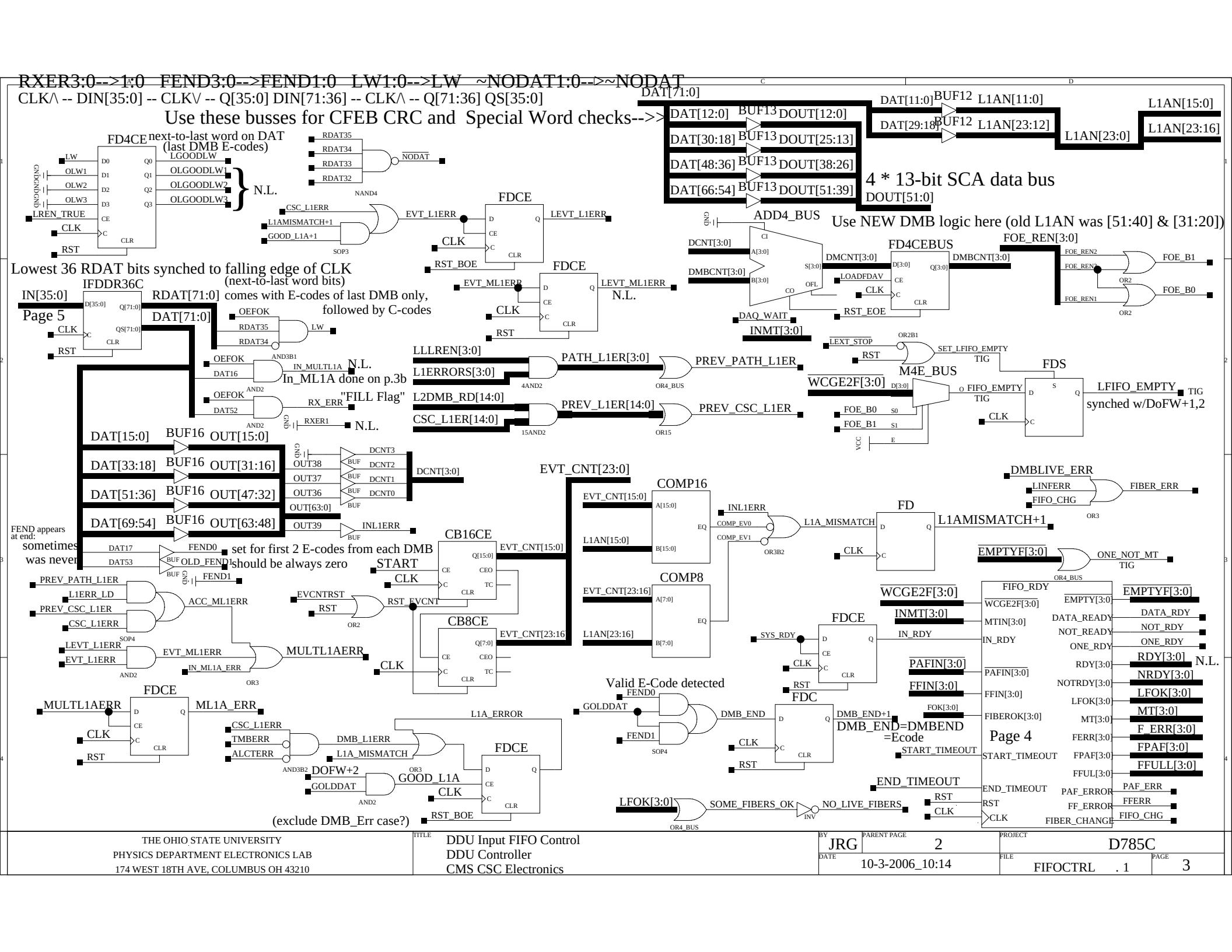
		DATE: 5-23-2006_16:04	FILE: DDUCNTRL . 10	PAGE: 2I

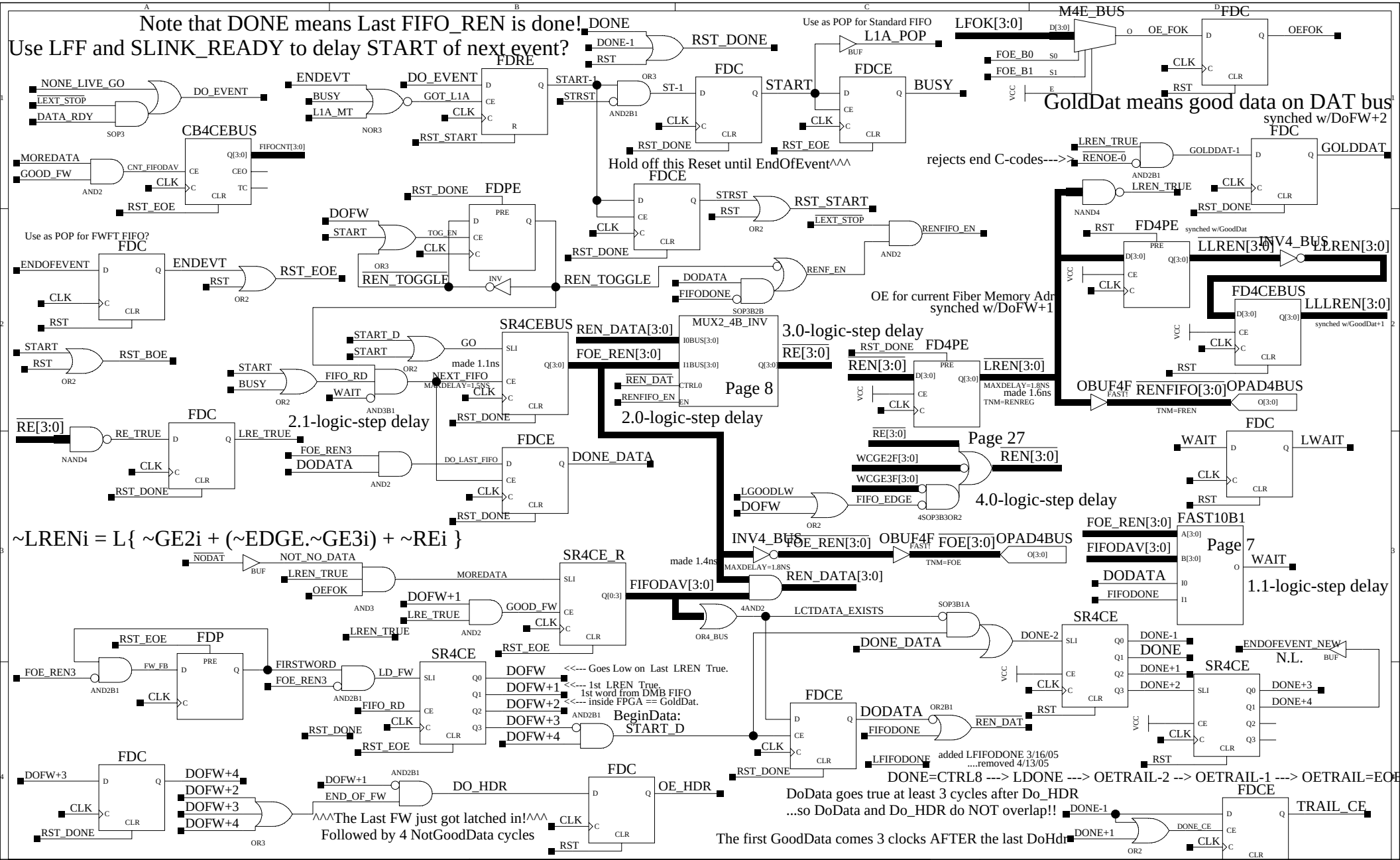
RXER3:0-->1:0 FEND3:0-->FEND1:0 LW1:0-->LW ~NODAT1:0-->~NODAT

CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

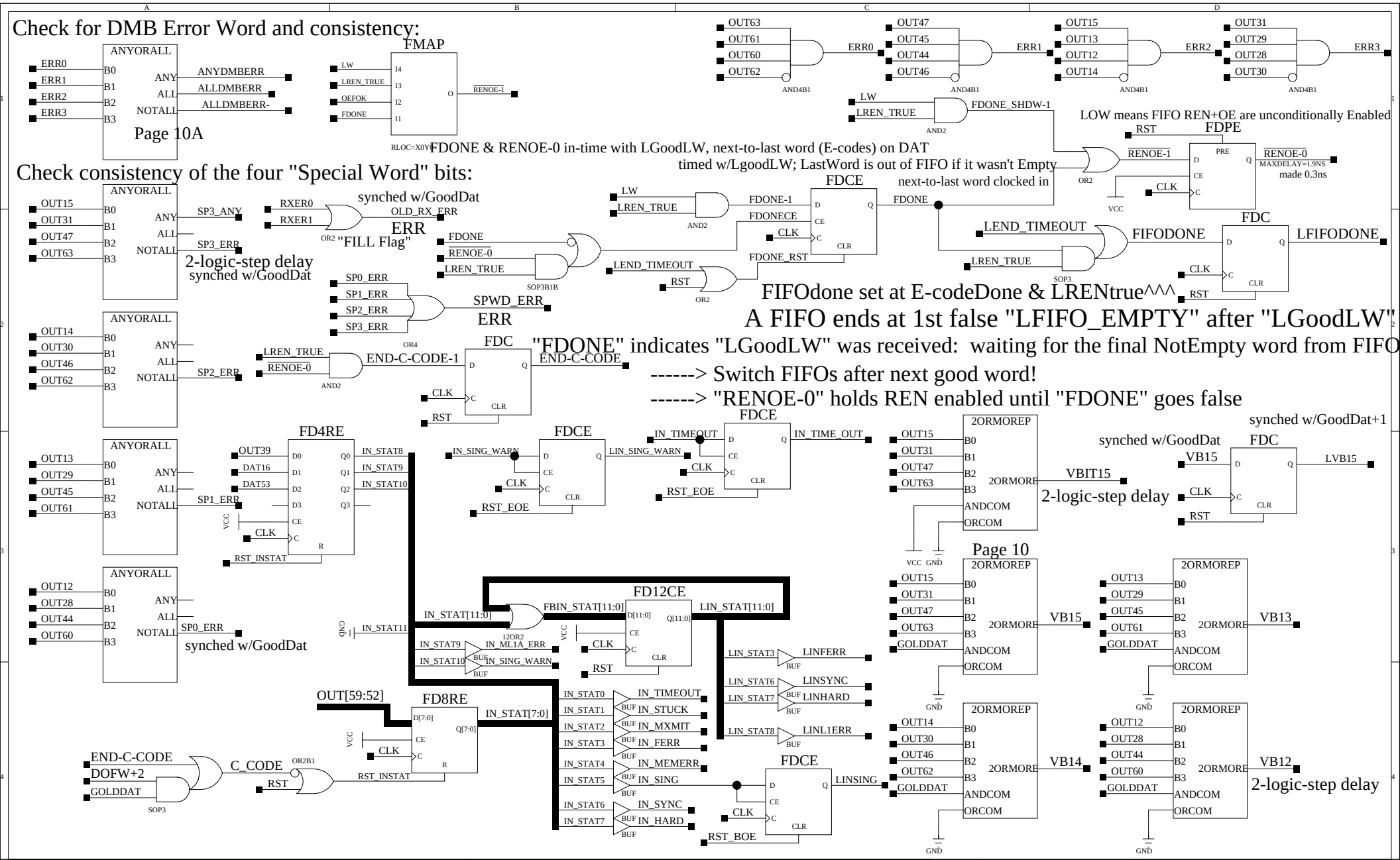
Use these busses for CFEB CRC and Special Word checks-->>



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2006_10:14	FILE: FIFOCTRL . 1	PAGE: 3



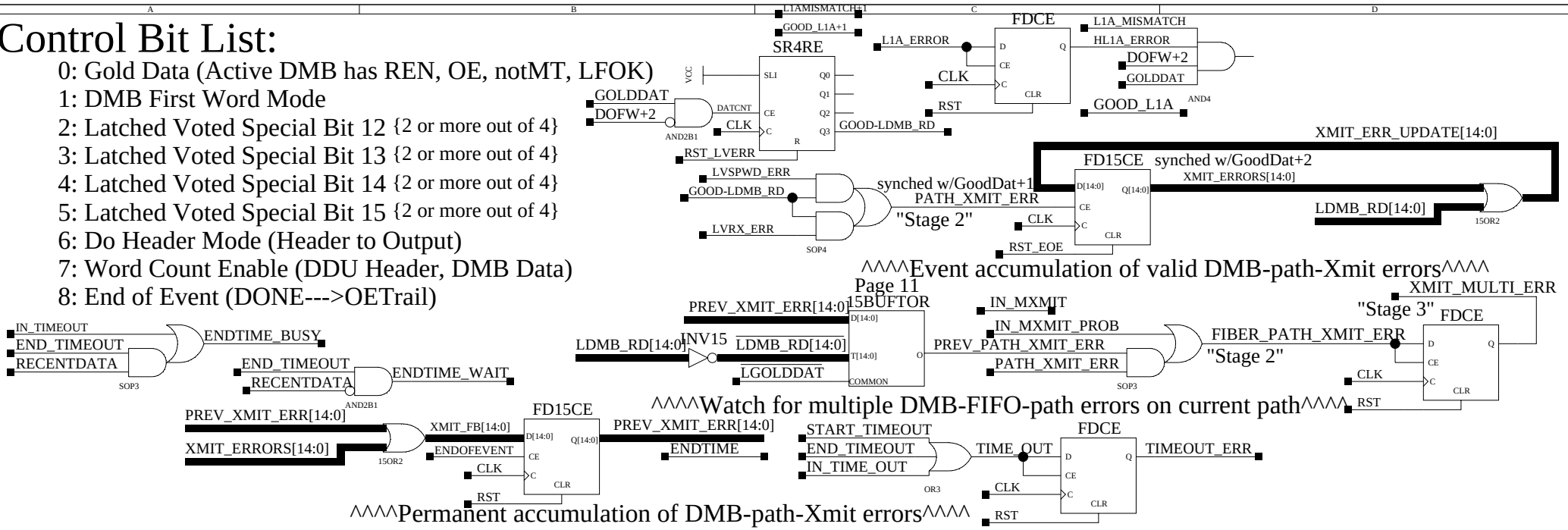
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 6-27-2006_11:14	PARENT PAGE: 2 FILE: FIFOCTRL . 2
		PROJECT: D785C	PAGE: 3A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-14-2006_14:42	FILE: FIFOCTRL . 3	PAGE: 3B

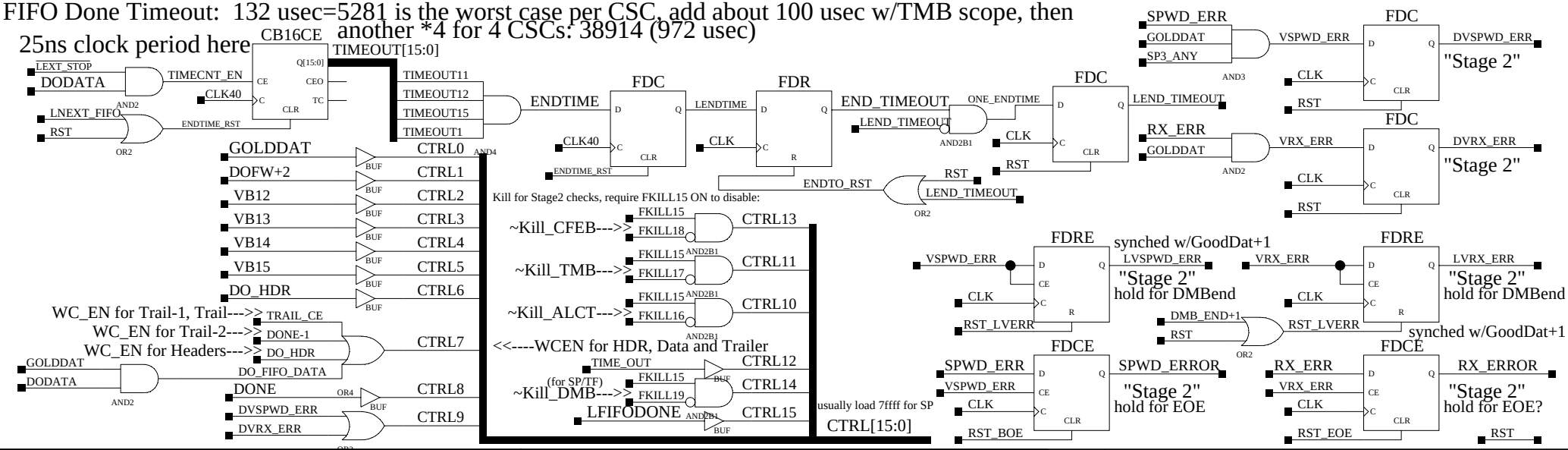
Control Bit List:

0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE--->OETrail)



FIFO Done Timeout: 132 usec=5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another *4 for 4 CSCs: 38914 (972 usec)

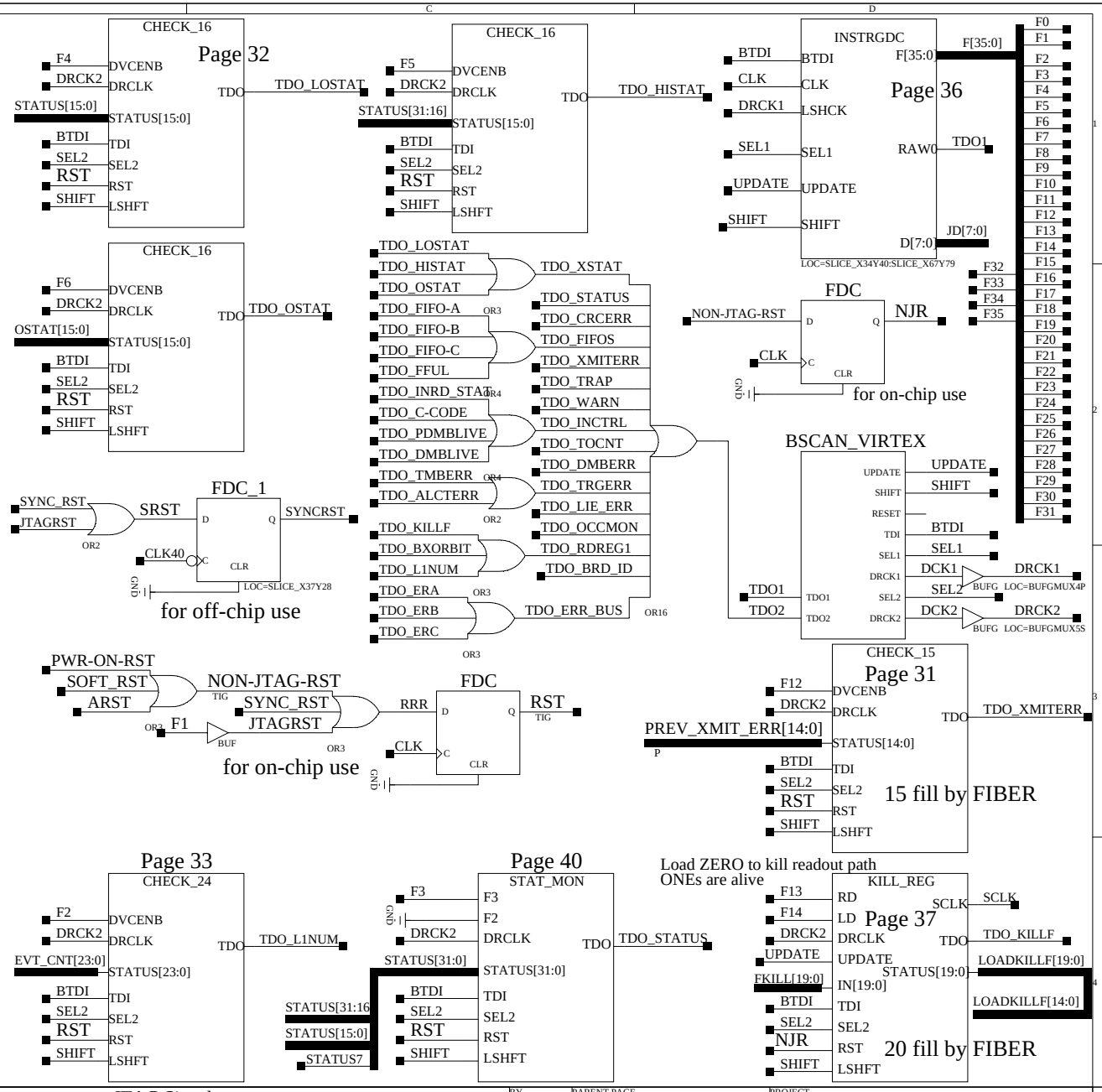
25ns clock period here



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-29-2006_15:00	FILE: FIFOCTRL . 4	PAGE: 3C

JTAG Instruction Decode

OpCode	Function [OpName]	
0	No Operation [NOOP]	
1	FPGA Reset [toggle]	
2	Read Current DDU L1A Number (24-bit scaler)	
3	Check status (capture and shift) [32 bits]	
4	Check status, low-word [16 bits]	
5	Check status, high-word [16 bits]	
6	Output Path Status [16-bits]	
7a	Check FOK (active input FIFOs) [lowest 4 bits]	
7b	L1A Mismatch (FIFO headers) [4-bits]	check FIFO-A
7c	Check FIFO Err (active FIFO change) [4 bits]	
7d	Stuck Data Errors (input FIFOs) [highest 4-bits]	
8a	Almost Full FIFOs [lowest 10-bits]	check FIFO-B
8b	FIFO Empty/GE2 Status [highest 6-bits]	
9a	Full FIFOs [lowest 10-bits]	FIFO Full/MT (raw)
* 9b	Raw FIFO Empty [highest 6-bits]	
10	CRC Errors [15-bits]	
11a	Lost In Data [lowest 4-bits]	check FIFO-C
11b	Timeout: start [4-bits]	
11c	Timeout: end-wait [4-bits]	
11d	Timeout: end-active [highest 4-bits]	
12	Data Xmit Errors [15-bits]	
13	Check KILL_Register [20 bits]	
14	Load KILL_Register [20 bits]	
15	DMB Errors [15-bits]	
16	TMB Errors [15-bits]	
17	ALCT Errors [15-bits]	
18	Lost In Event [15-bits]	
* 19	InRD Status [16-bits]	
* 20	InRD C-code & MxmitErr History [16-bits]	
* 21	Critical Error Trap Reg. [192 bits]	
22	Error Register A [16-bits]	
23	Error Register B [16-bits]	
24	Error Register C [16-bits]	
25	Read DMB_LIVE [15-bits]	
26	Read P_DMB_LIVE [15-bits]	
27	Read WARN_MON [16-bits]	
* 28	Max Timeout Count [16-bits]	
29	Set BX per Orbit [12-bits]	
30	Read BX per Orbit [12-bits]	
31	Toggle CFEB_Cal Auto_L1 [default enable]	
32	Read DDU Board ID [16-bits]	
33	DDU-only VME_L1A	
* 34	Read CSC Board Occupancy scalers (loops for 60 words, 32-bit)	



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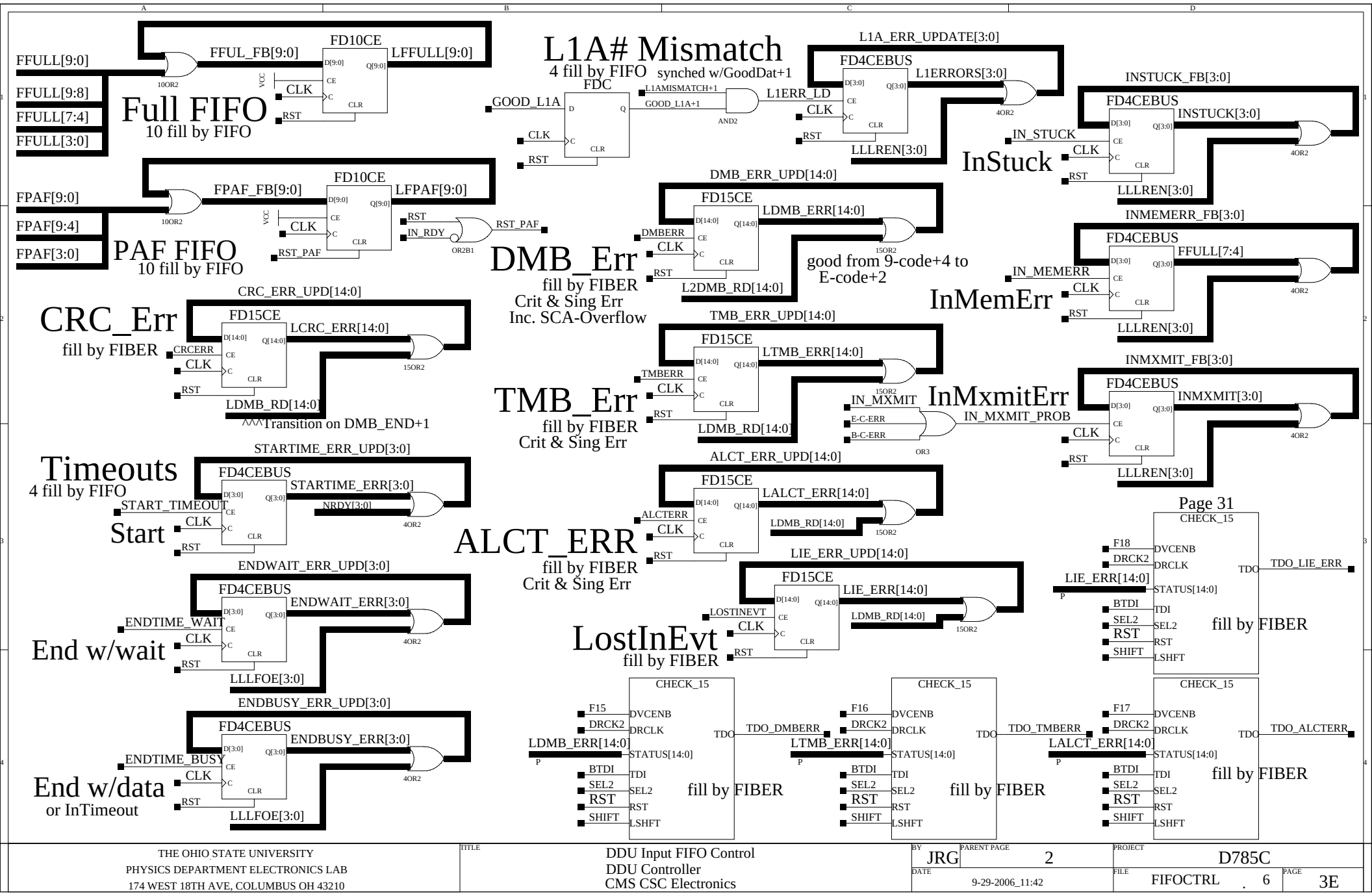
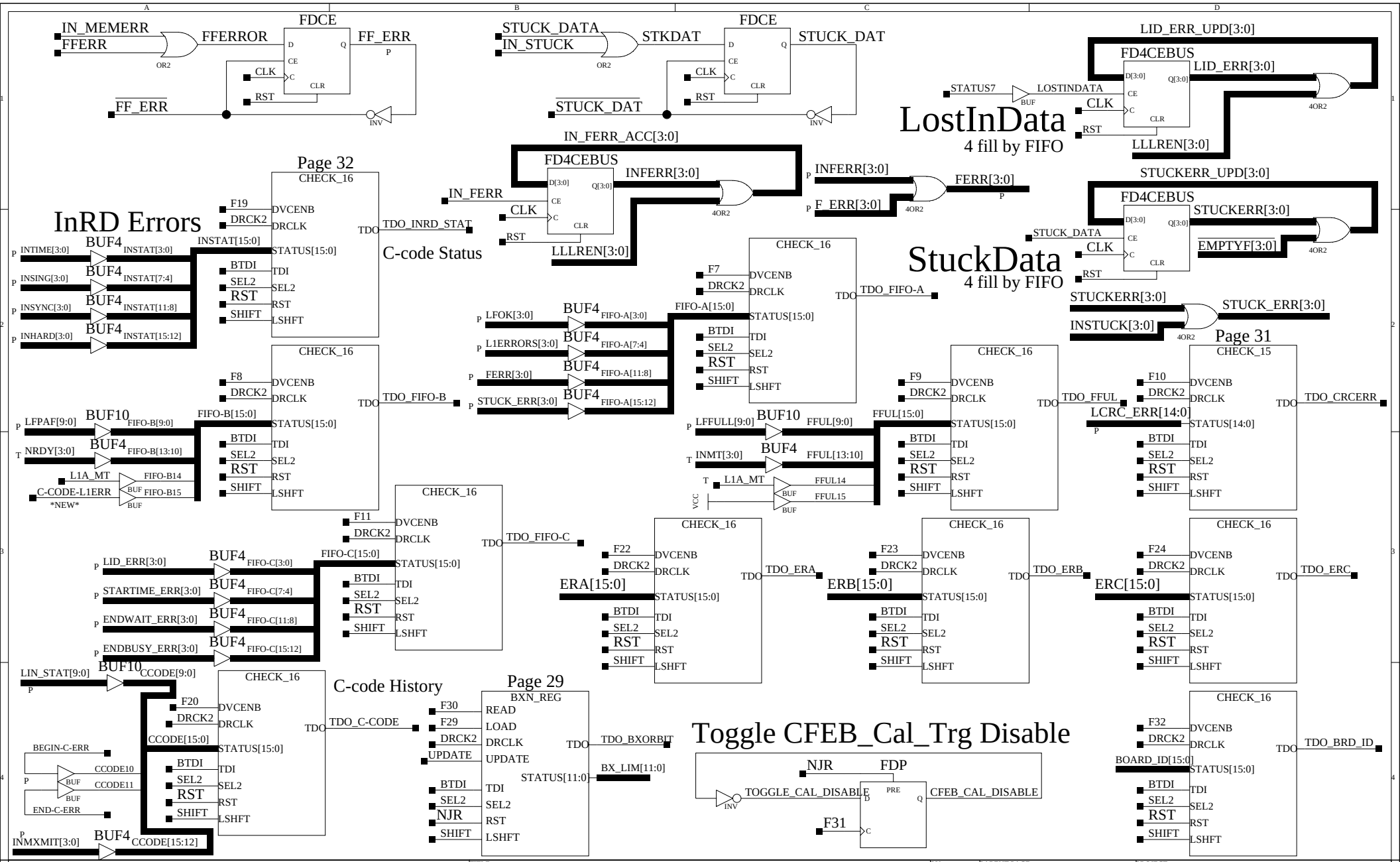
TITLE: JTAG Signals
DDU Controller
CMS CSC Electronics

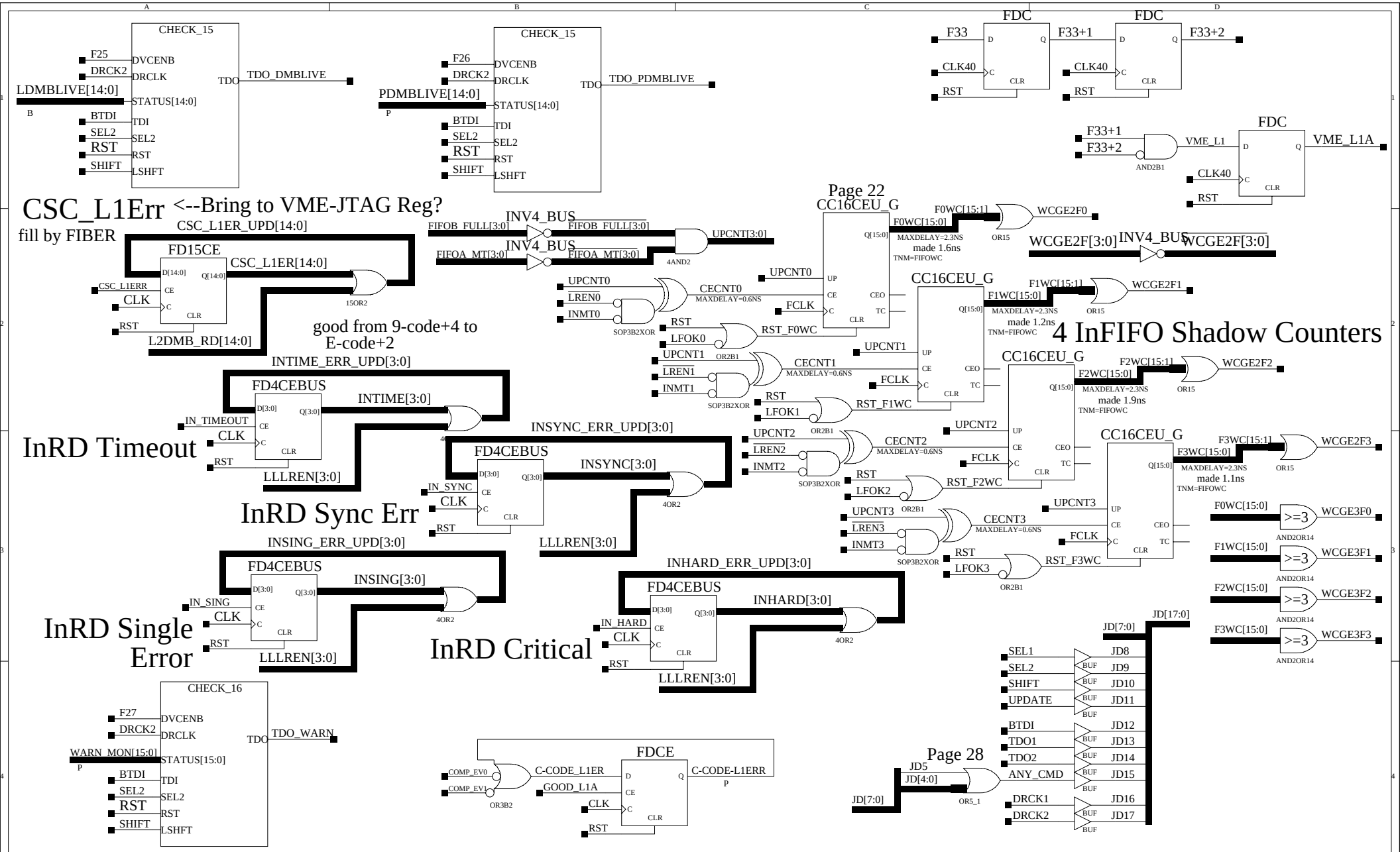
BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 6-1-2006_17:23 | FILE: FIFOCTRL . 5 | PAGE: 3D



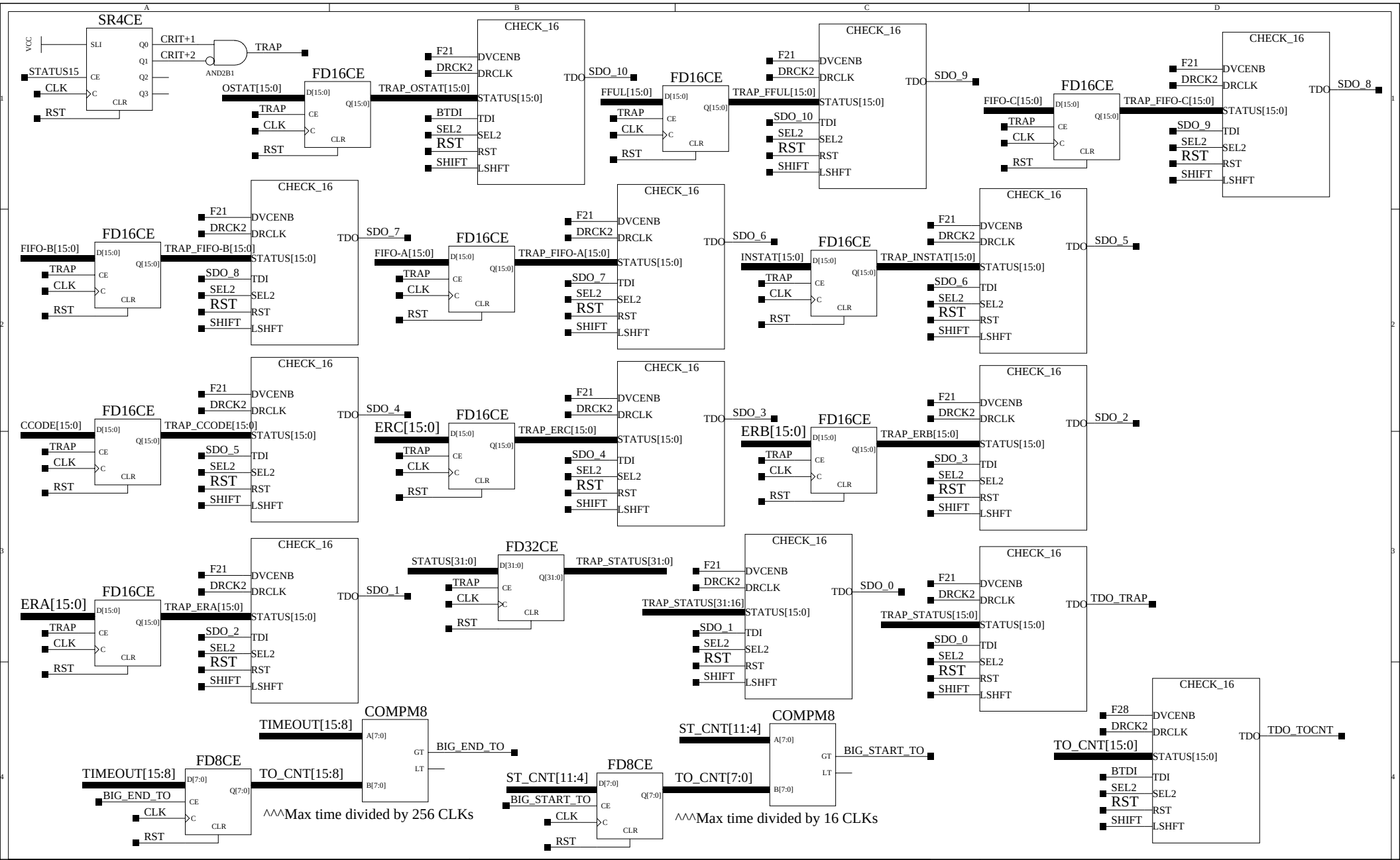
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-29-2006_11:42	FILE: FIFOCTRL . 6	PAGE: 3E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2006_10:28	FILE: FIFOCTRL . 7	PAGE: 3F

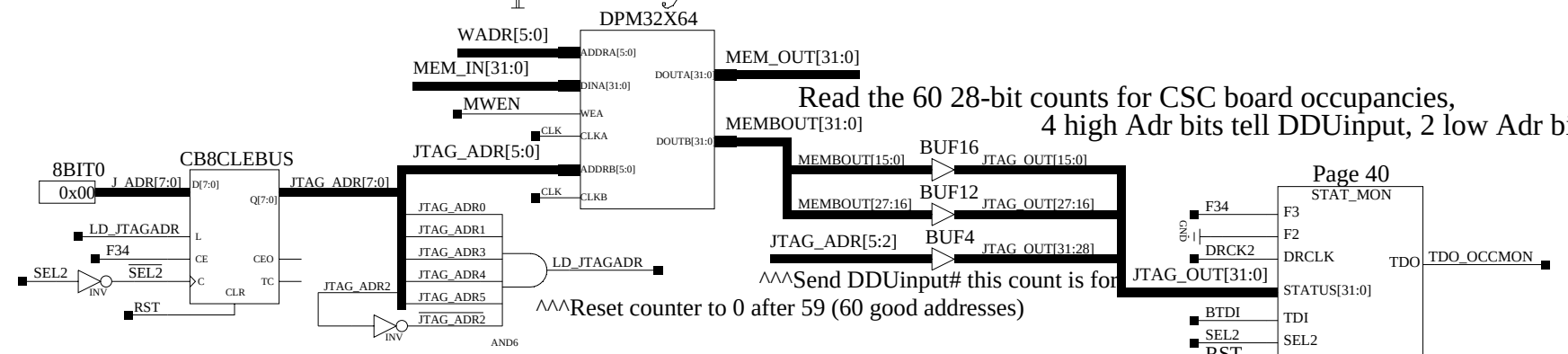


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2006_10:15	FILE: FIFOCTRL . 8	PAGE: 3G



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Critical Error Trap DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 5-23-2006_14:23	FILE: FIFOCTRL . 9	PAGE: 3H

CSC Board Occupancy Tracker: 15 fibers x 4—boards each



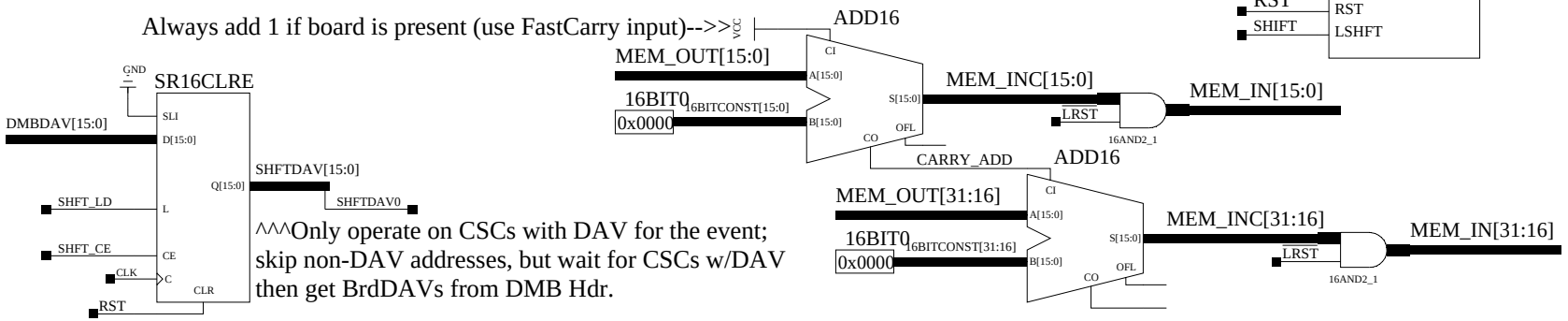
Read the 60 28-bit counts for CSC board occupancies,
4 high Adr bits tell DDUinput, 2 low Adr bits specifiy Board Type:

0 = DMB
1 = ALCT
2 = TMB
3 = CFEB

^^^Send DDUinput# this count is for

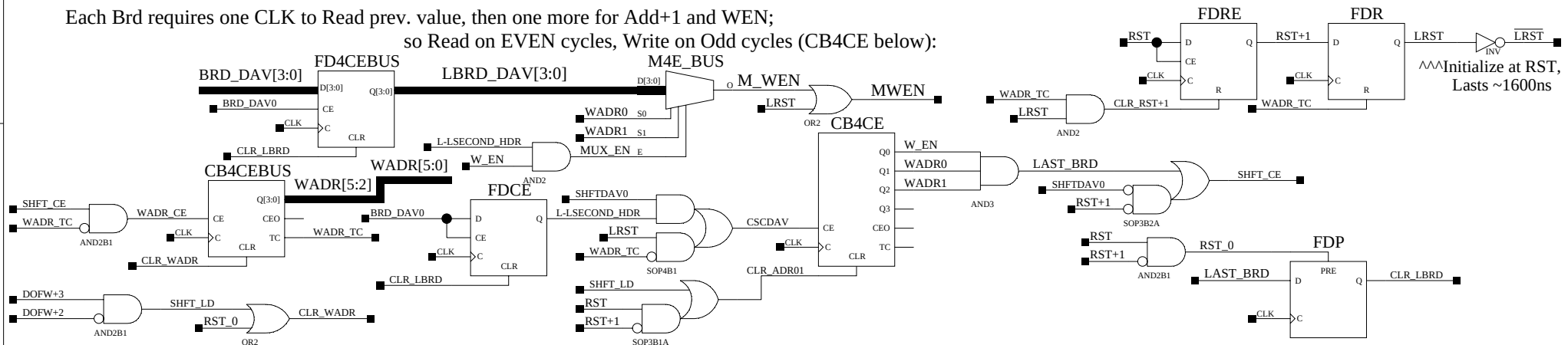
^^^Reset counter to 0 after 59 (60 good addresses)

Always add 1 if board is present (use FastCarry input)-->>>



^^^Only operate on CSCs with DAV for the event; skip non-DAV addresses, but wait for CSCs w/DAV then get BrdDAVs from DMB Hdr.

Each Brd requires one CLK to Read prev. value, then one more for Add+1 and WEN;
so Read on EVEN cycles, Write on Odd cycles (CB4CE below):



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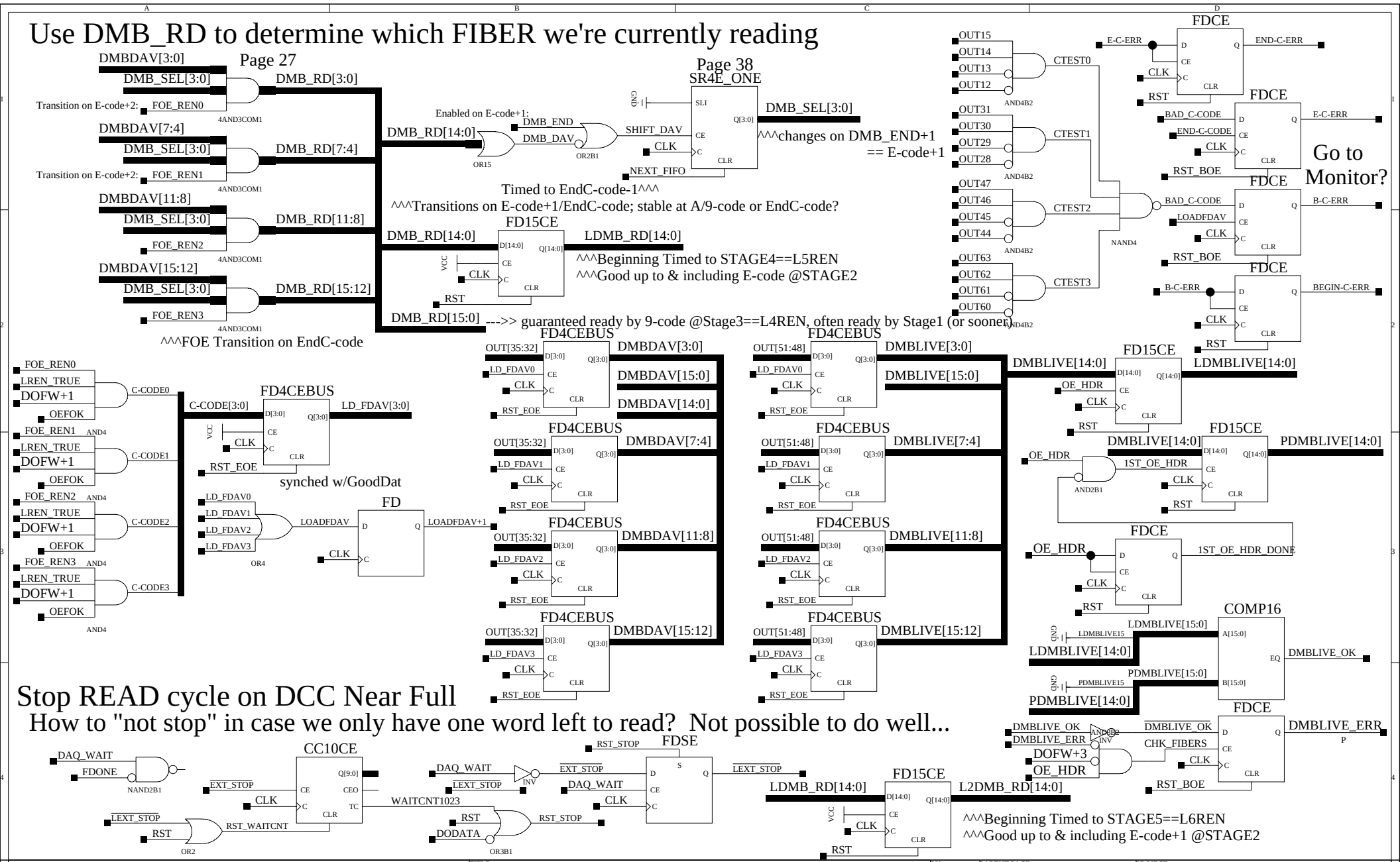
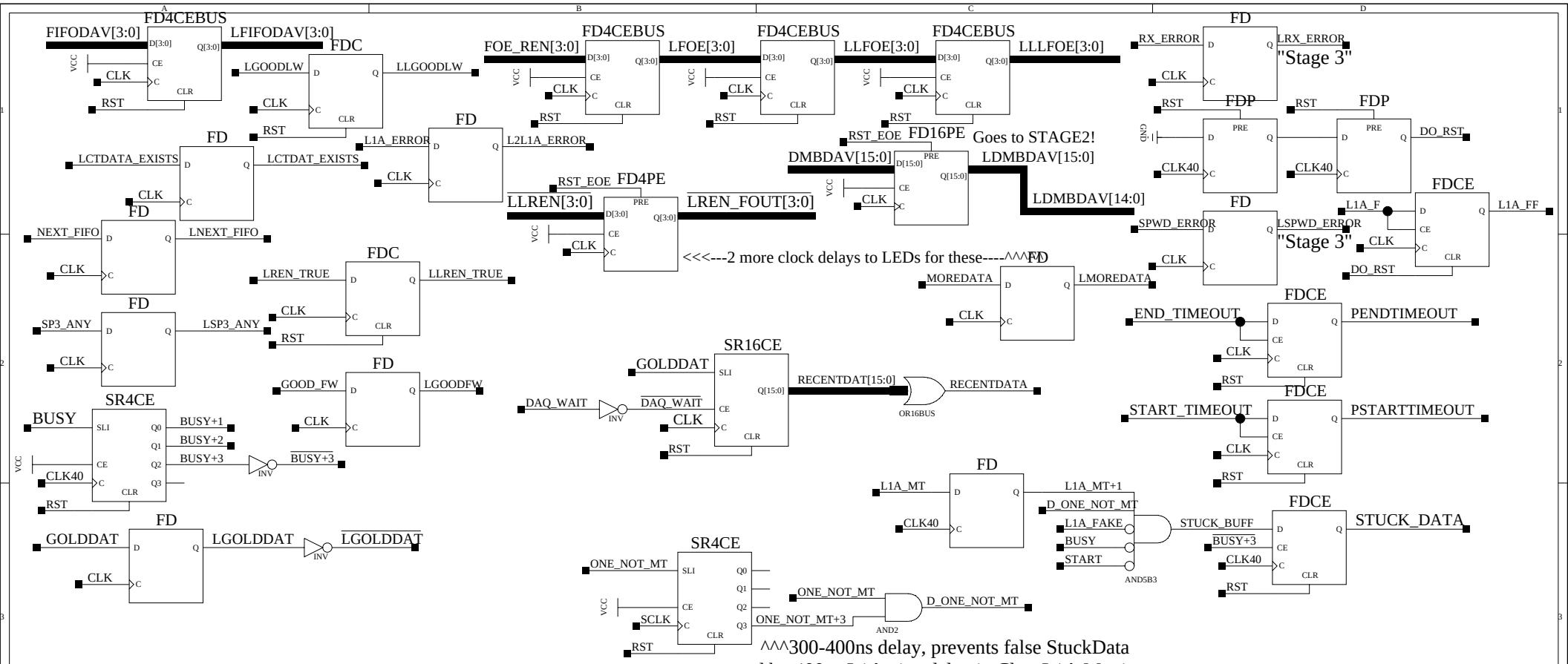
TITLE	DDU Occupancy Monitor DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
		DATE 5-23-2006_14:23	FILE FIFOCTRL . 10	PAGE 3I

Use DMB_RD to determine which FIBER we're currently reading



Stop READ cycle on DCC Near Full

How to "not stop" in case we only have one word left to read? Not possible to do well...

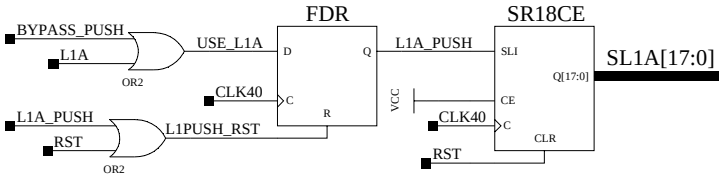


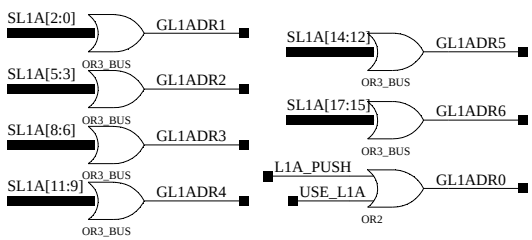
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 5-23-2006_15:26	FILE: FIFOCTRL . 12	PAGE: 3K

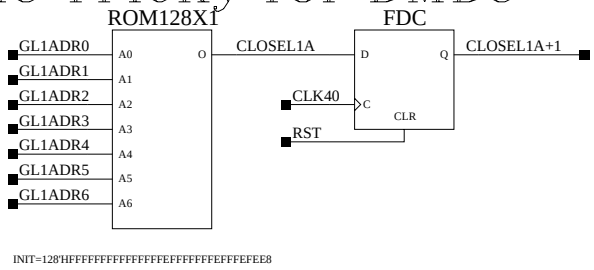
L1A Proximity Tracker: 500ns Close L1A Monitor

closer than 450ns is Tricky for DMBs

END







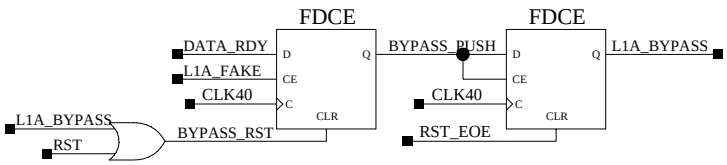
Pipe all L1As for 450ns, if more than 1 then set CloseL1A bit^^^

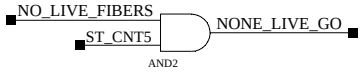
L1As can be combined into 7 3-bin bunches (LHC 75ns rule) to ensure separation 500ns^^^

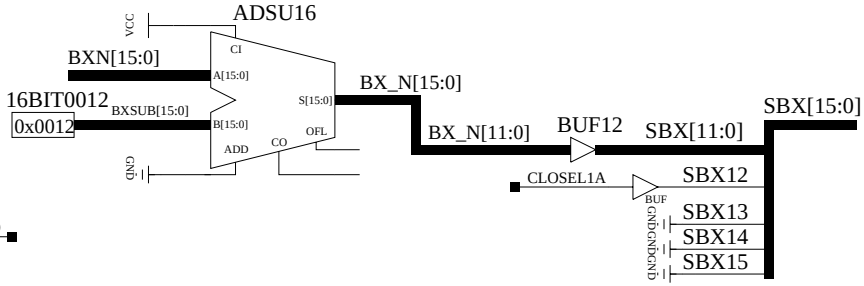
use these 7 bunches as Adr for ROM lookup table for Tricky L1A patterns^^^

Finally, perform BX-18 to correct BXN and store CloseL1A as BXN bit-12.

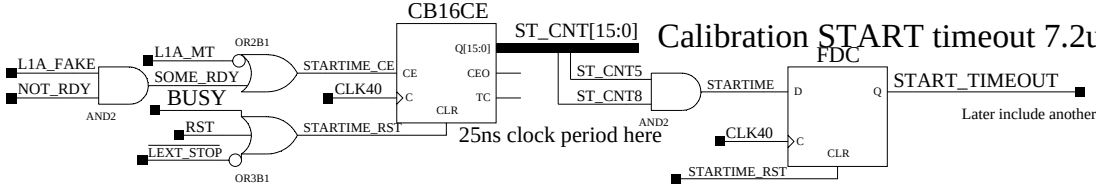
Then use SBXN12 output (Close_L1A) for Stage2 DMB checks: 500ns L1As means that first 2 CFEB samples should always have good L1A#







Event START timeout 3.2usec: 128=1000/0000=0x80....



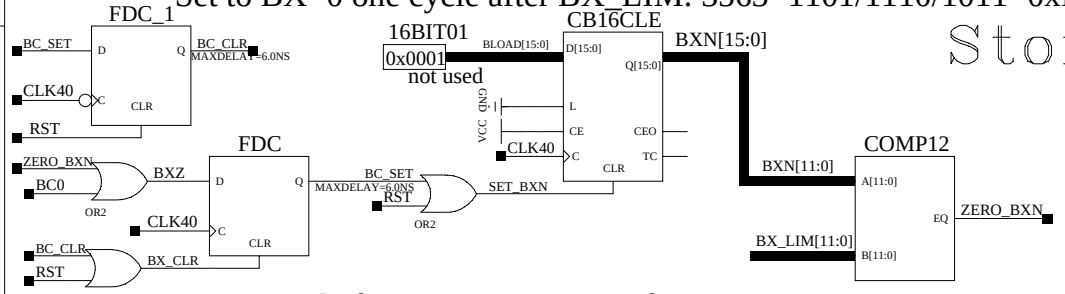
Calibration START timeout 7.2usec: 288=0x0120.

25ns clock period here

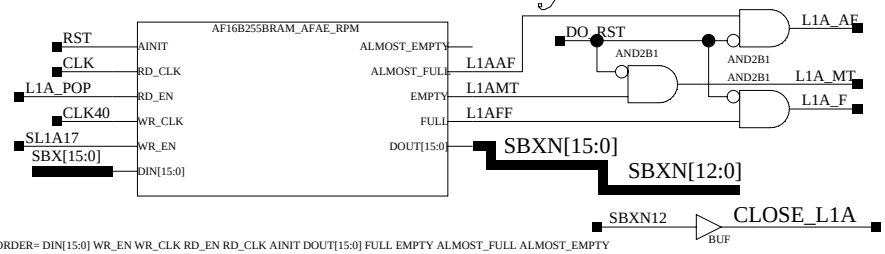
Later include another 16-bit FIFO for Trig/Evt Type?

LHC BXN cycles from 0 to 3563

Set to BX=0 one cycle after BX_LIM: 3563=1101/1110/1011=0xDEB



Store the BXN for every L1A:



PINORDER= DIN[15:0] WR_EN WR_CLK RD_EN RD_CLK AINIT DOUT[15:0] FULL EMPTY ALMOST_FULL ALMOST_EMPTY

SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

THE OHIO STATE UNIVERSITY
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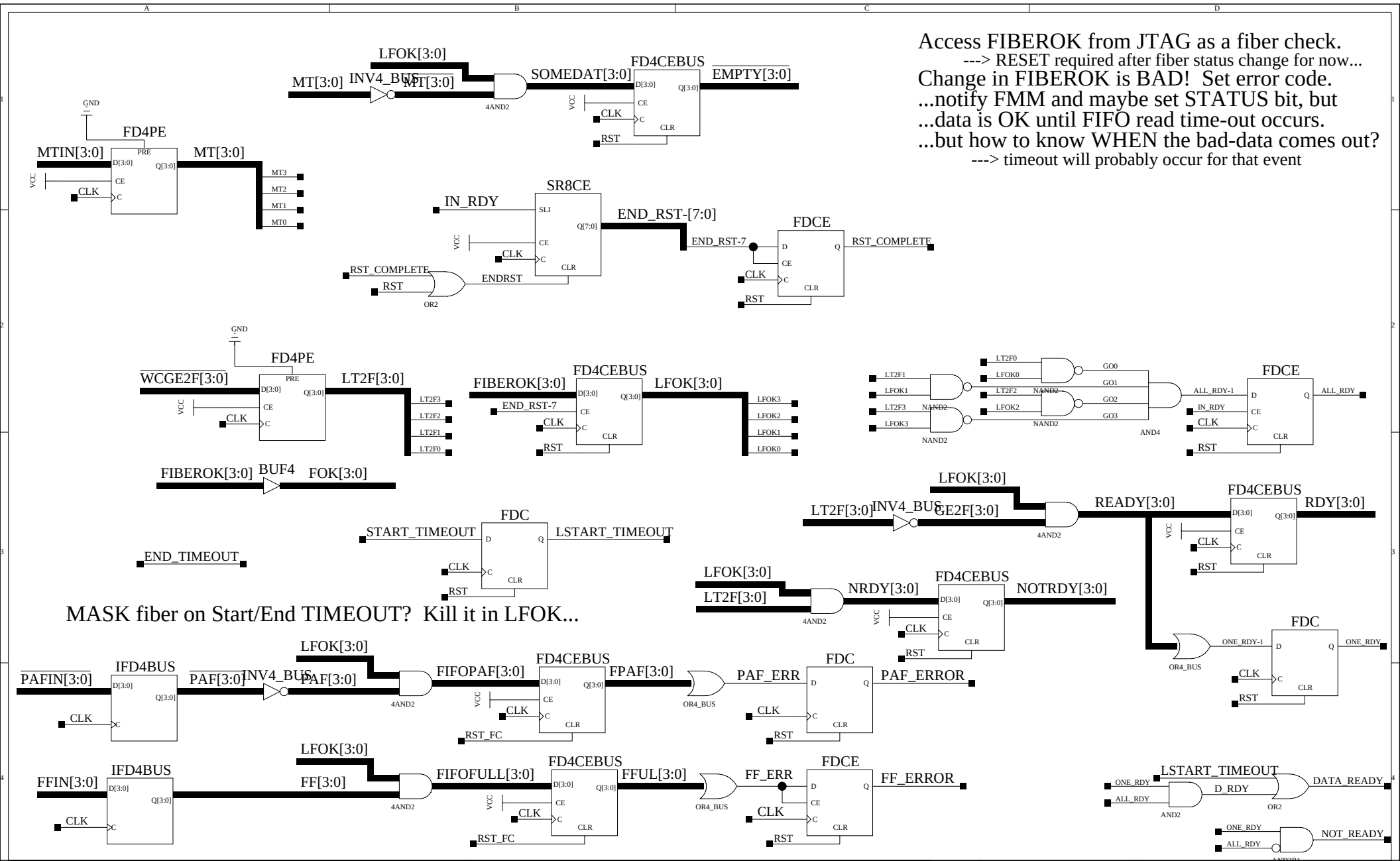
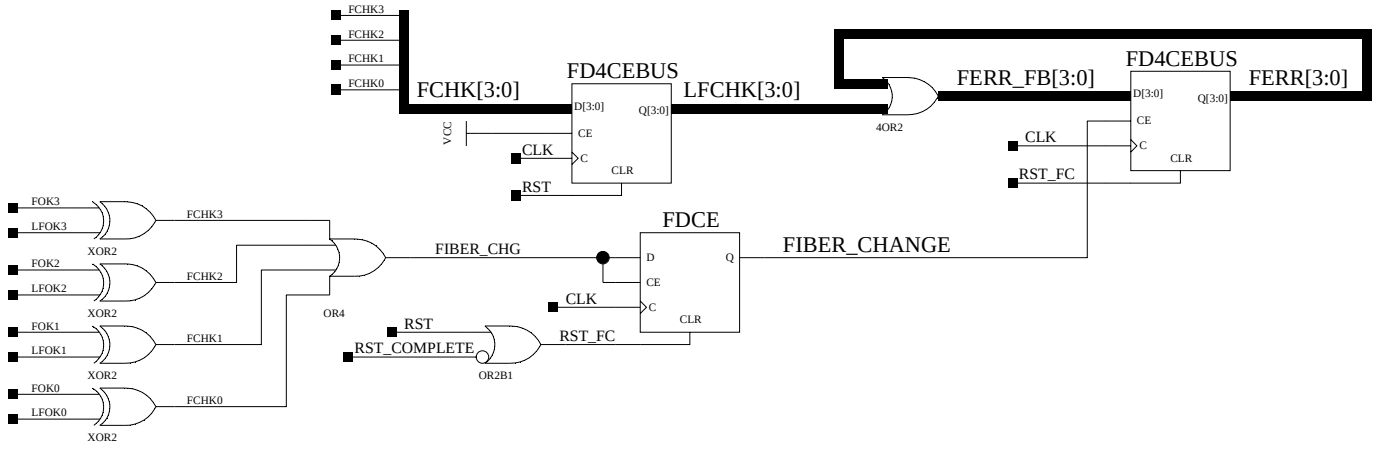
TITLE: DDU Input FIFO Control
DDU Controller
CMS CSC Electronics

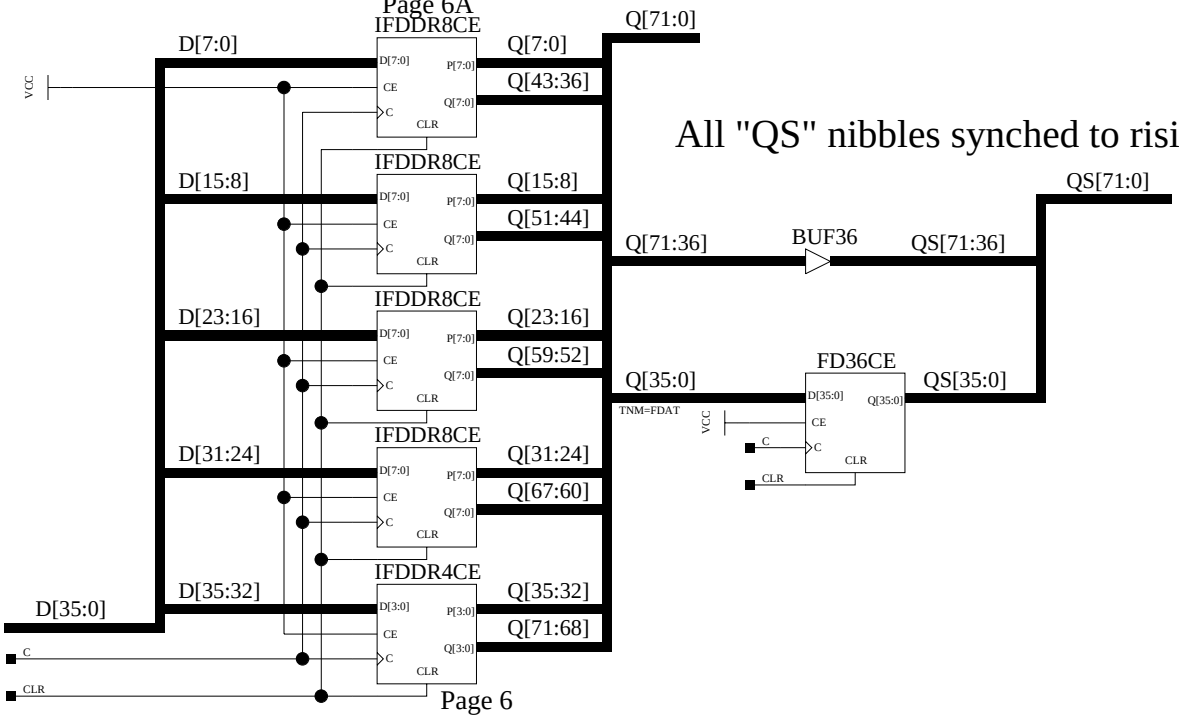
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
9-12-2006_11:38	FIFOCTRL . 13	3L



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input FPGAs Available for DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 9-12-2006_10:43	FILE: FIFO_RDY . 1	PAGE: 4



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C	
		DATE: 9-12-2006_10:43		FILE: FIFO_RDY . 2	PAGE: 4A

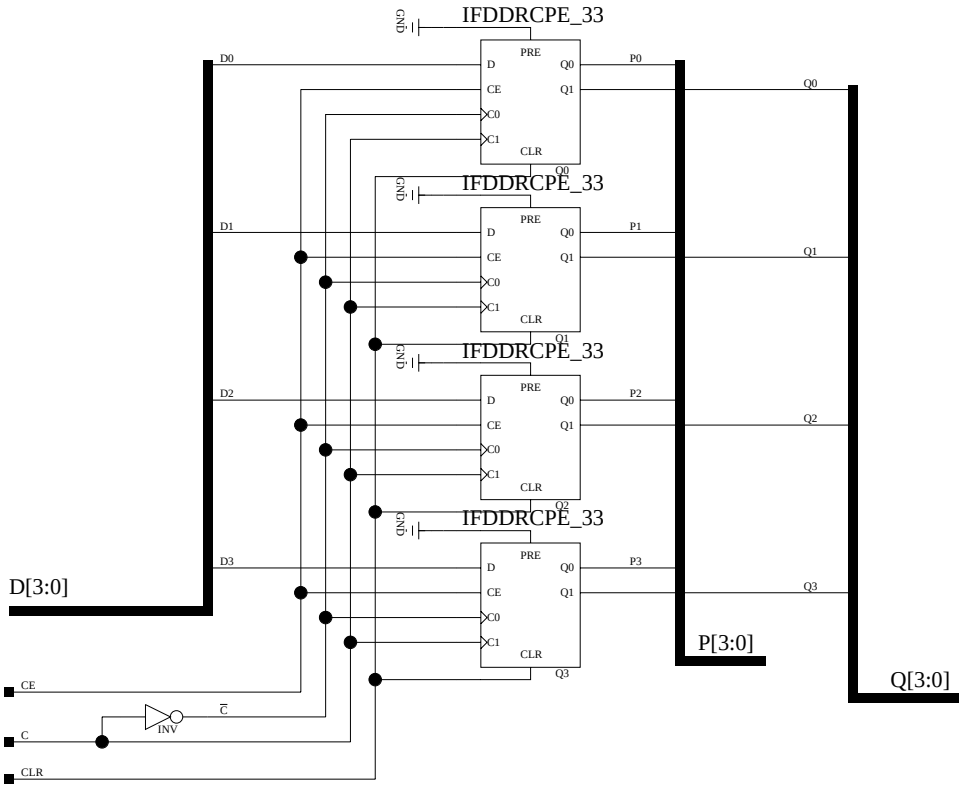


CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

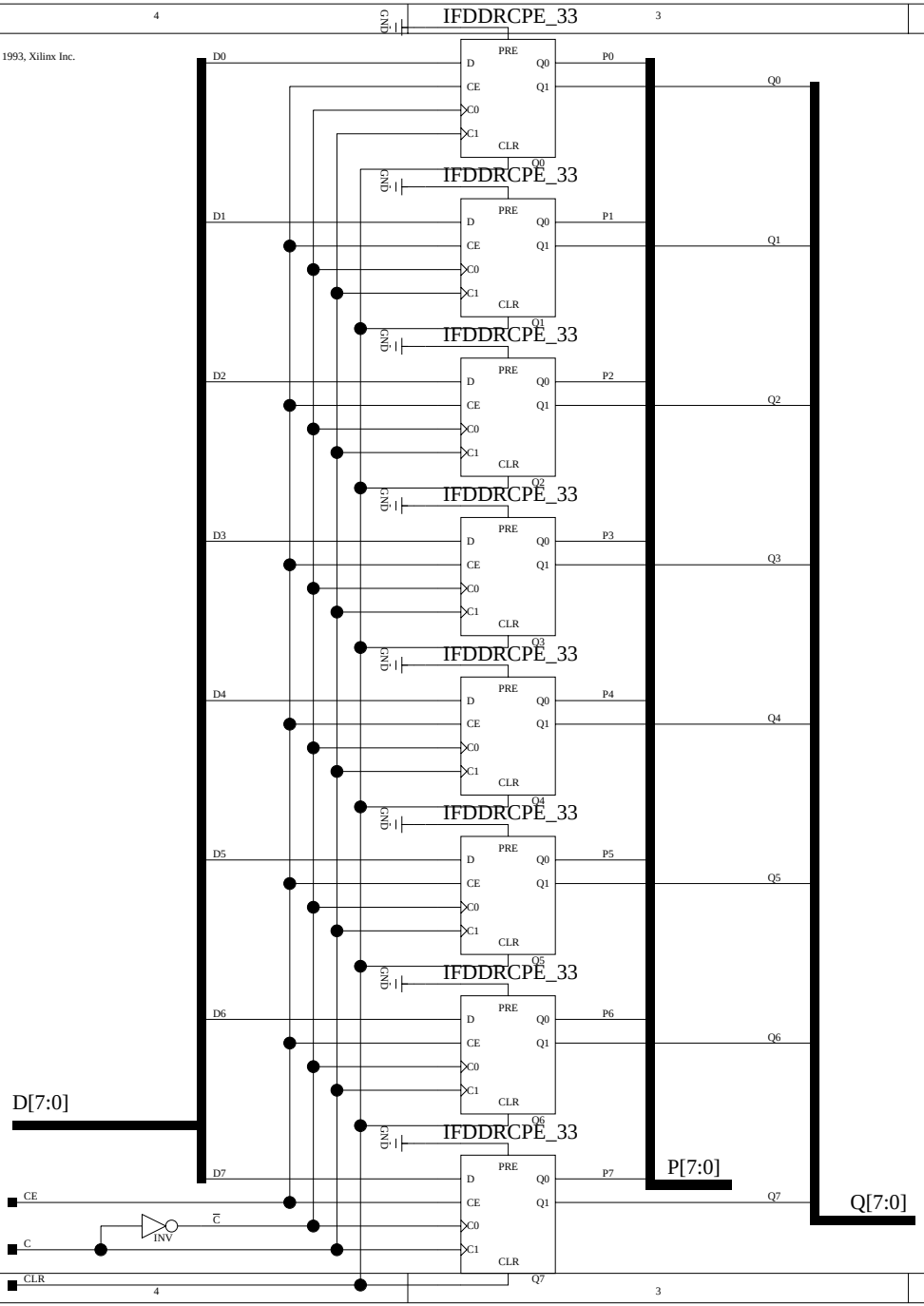
XILINX

Title:	VIRTEX Family IFDDR36C Macro, LVCMOS33		
Comments:	36-Bit DDR Input Flip-Flop with asynchronus clear	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A

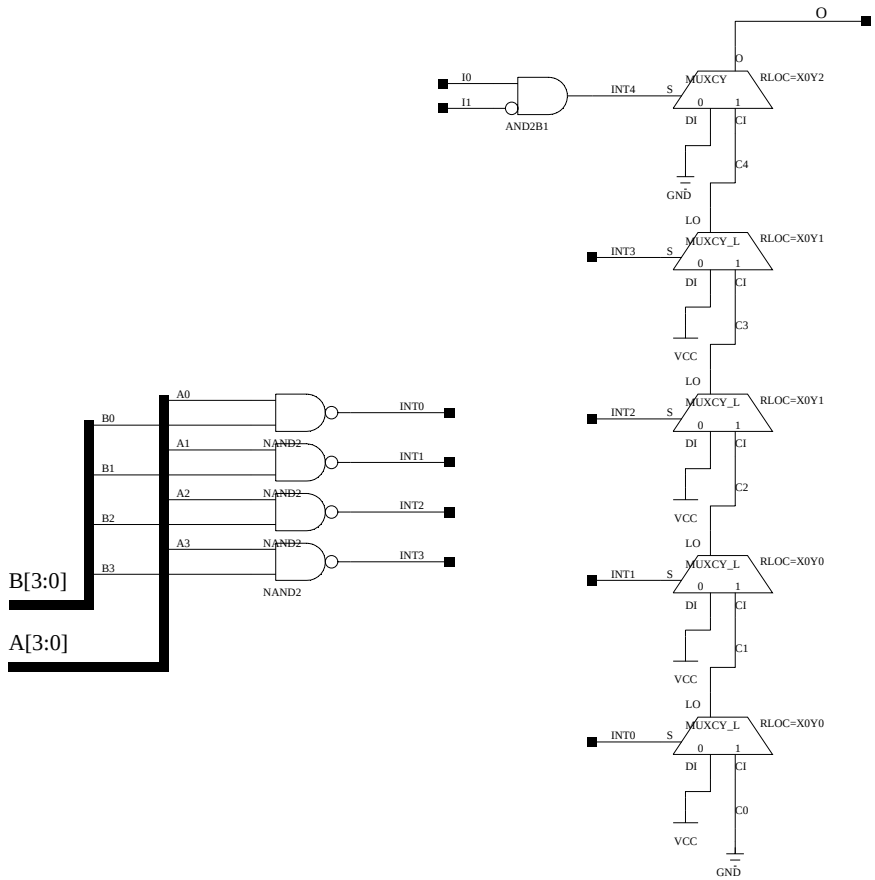
drawn by KS



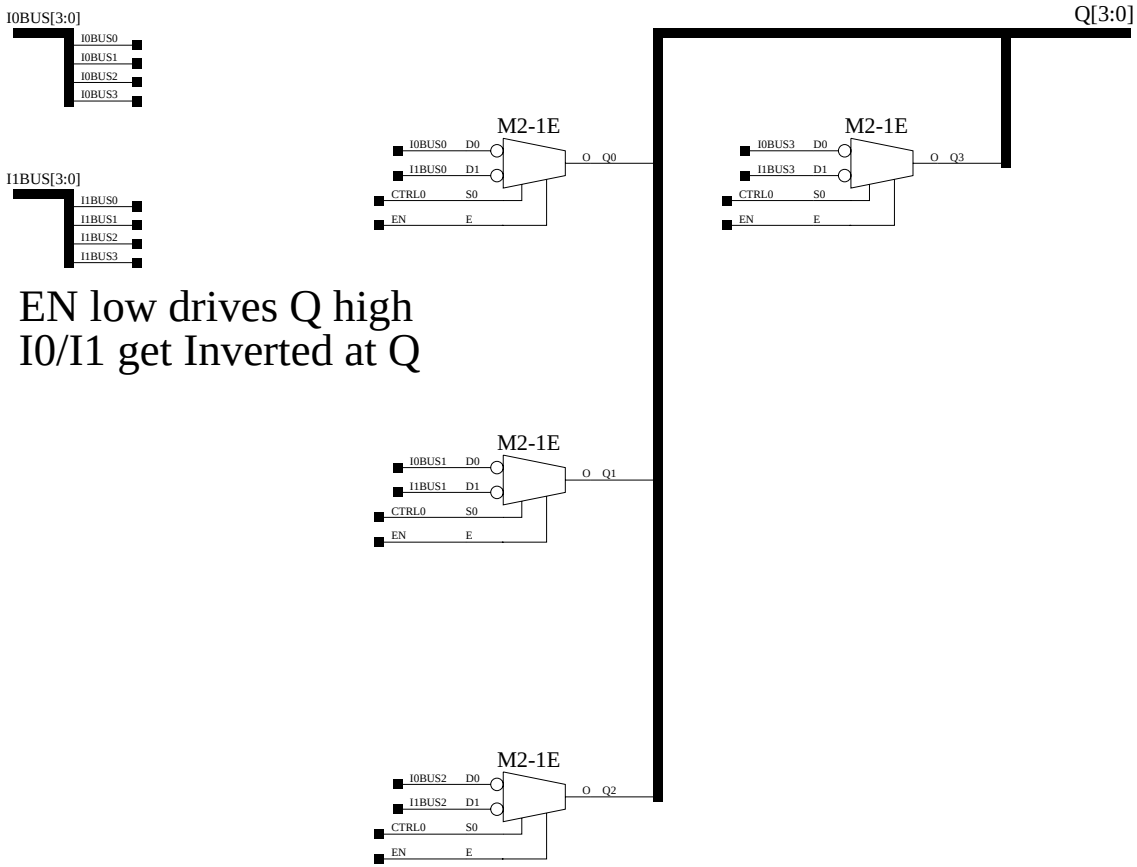
Title:	VIRTEX Family IFDDR4CE Macro, LVCMOS33		JRG
Comments:	4-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



Title:	VIRTEX Family IFDDR8CE Macro, LVCMOS33		JRG
Comments:	8-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



XILINX			JRG
Title:	FAST10B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 .AND. AND2B1		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A



EN low drives Q high
I0/I1 get Inverted at Q

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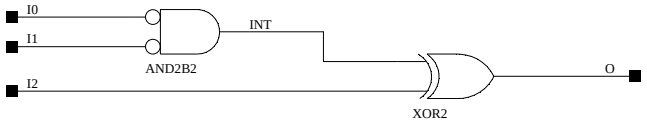
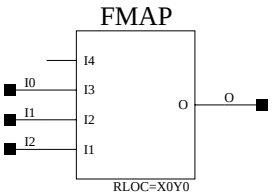
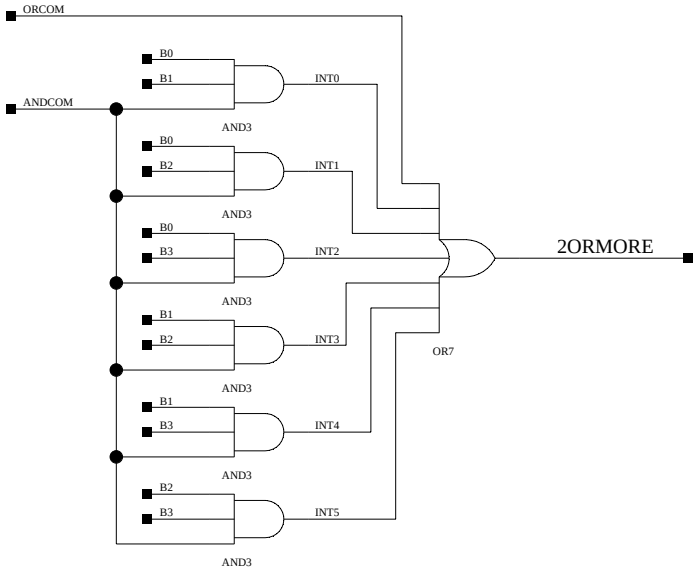
TITLE: 4-bit MUX for 2 4-bit Inputs, w/Enable, invert selected DIN
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	3	D785C
DATE	FILE	PAGE
5-24-2005_14:02	MUX2_4B_INV . 1	8

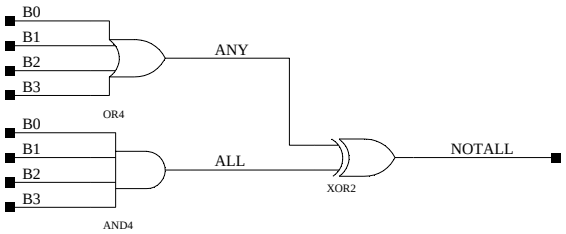




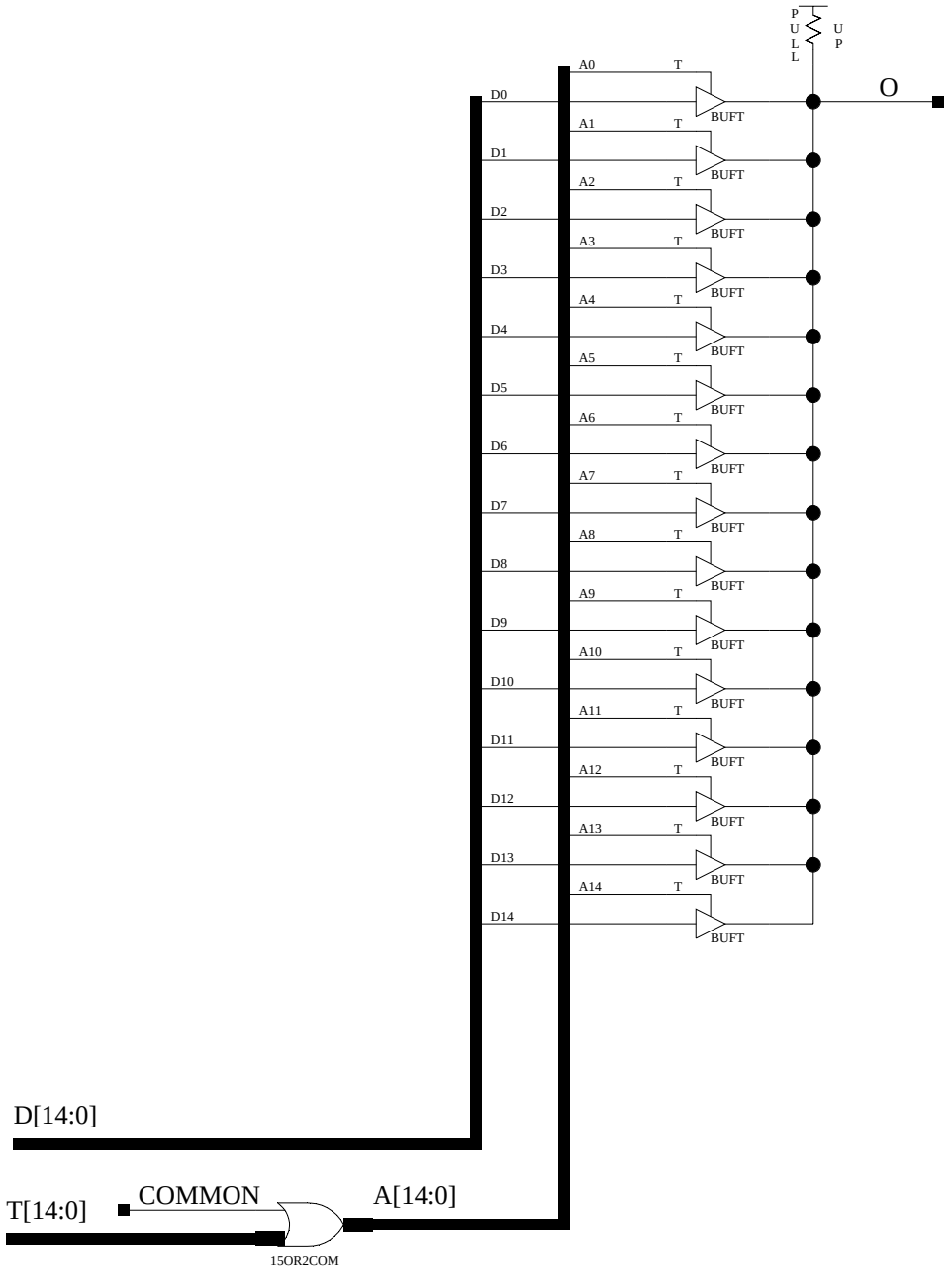
Title:	VIRTEX Family SOP3B2XOR Macro
Comments:	SOP3B2XOR Gate
	JRG
Date: 11th December 2003	Ver: 1
Sheet Size: A	Rev: A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3	PROJECT D785C
			DATE 7-18-2005_17:01	FILE 2ORMOREP . 1	PAGE 10



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for ALL bits set, ANY bits set and NOTALL bits set DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_17:01	PARENT PAGE: 3 FILE: ANYORALL . 1	PROJECT: D785C PAGE: 10A



XILINX

Title: VIRTEX Family 15-BufTOR Macro

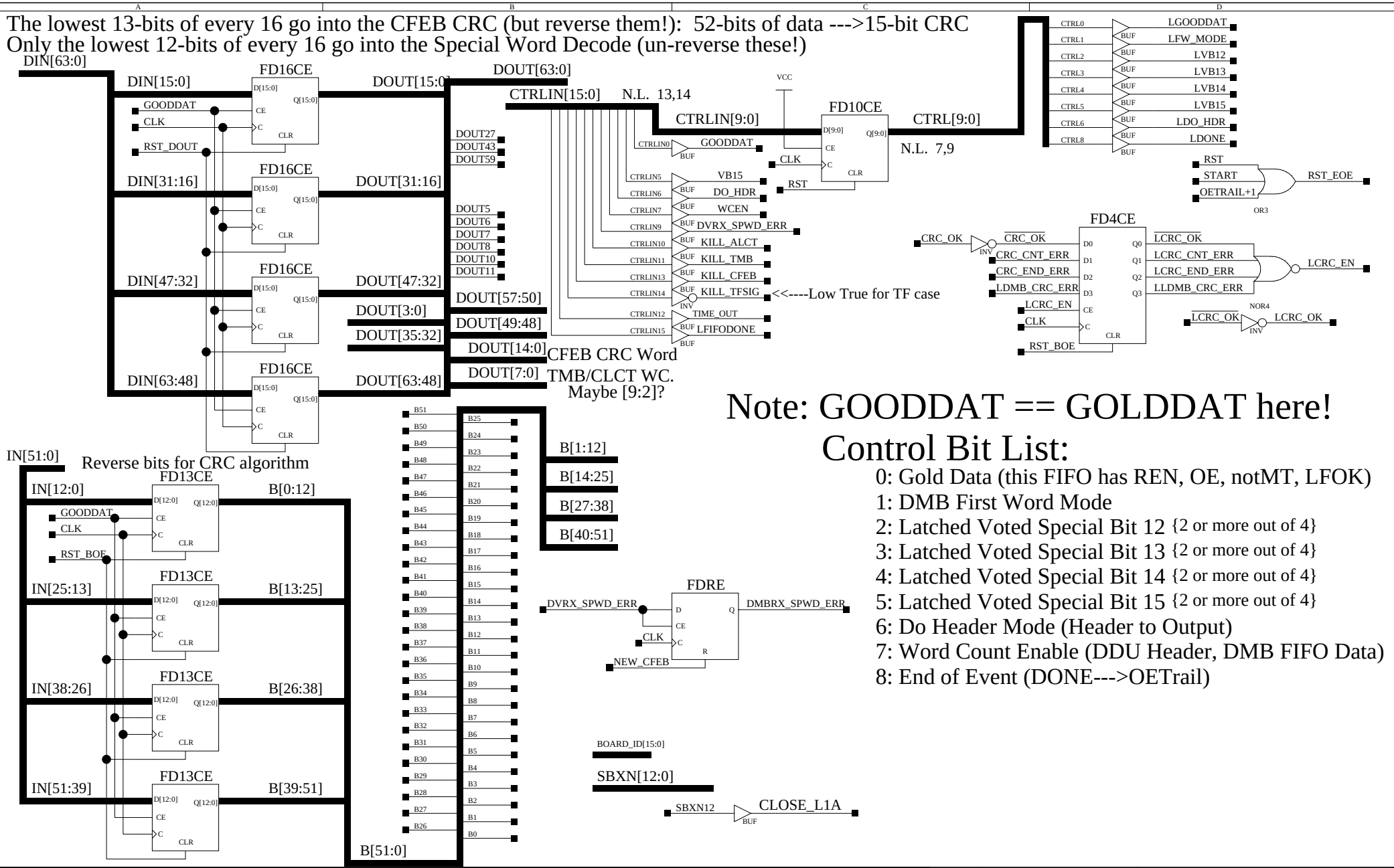
Comments: 15-BufT Bus Gate with Bus-OR-Common control

JRG

Date: 27th December 2001 Ver: 1

Sheet Size: A Rev: A

drawn by KS



THE OHIO STATE UNIVERSITY
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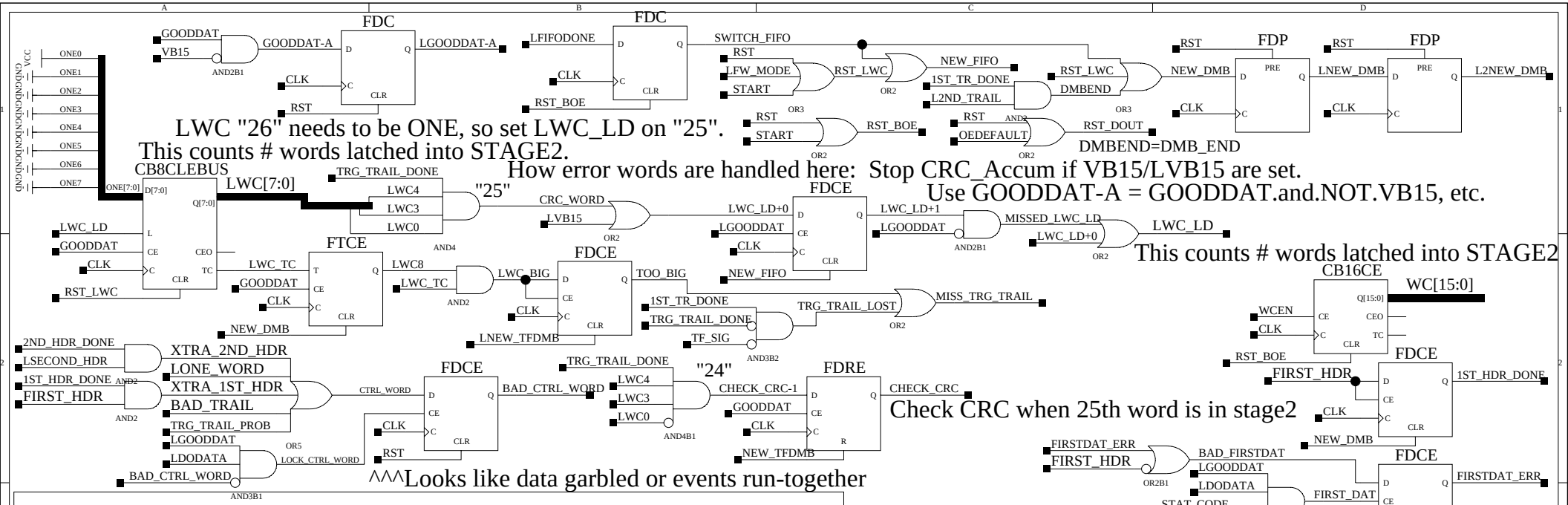
TITLE: Stage 2 Logic: WC/CRC Accumulators
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
10-2-2006_13:22	STAGE2 . 1	12



Critical DMB Monitoring Information (Production DMB) UPDATE!

See http://www.physics.ohio-state.edu/~cms/dmb/dmbdatafmt.html

Within each time sample: word100[15:0] = dummy = 0x7FFF <<----What about SCA Over-Written Event error?
word97[14:0] = CRC15 result ----->> *DDU Compare*

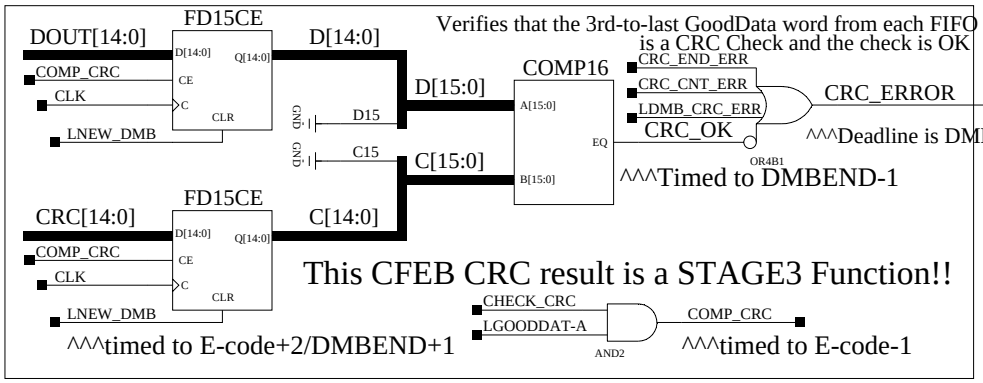
word98[9] = CFEB L1A_FIFO_Full error ----->> *****DDU Error*****
----->> ***DDU Warning***

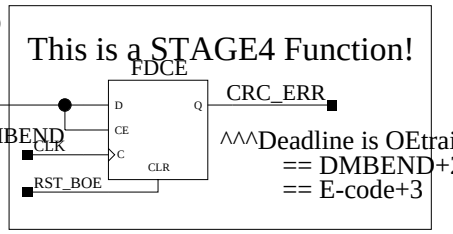
Header7[11:7] = CFEB_Multi-Overlap[5:1] = Garbage Event ----->> *****DDU Error*****
Trailer6,7,8[11:0] = DMB End/Start Timeout error, 3 repeats ----->> *****DDU Error*****
Header5 = TMB/ALCT DAV bits, 3 repeats ----->> **DDU Control**
Header1,5[4:0] = CFEB_DAV[CFEB5:1], 2 repeats \
Header1[9:5] = CFEB_CLCT[CFEB5:1], 1 repeat / =====>> *DDU Compare Together*
L1AN[23:0] = HDR3[11:0],HDR2[11:0] ----->> *DDU Compare*
----->> *DDU Compare*

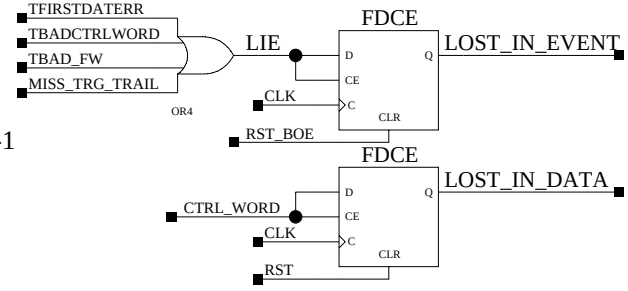
to ERB only?

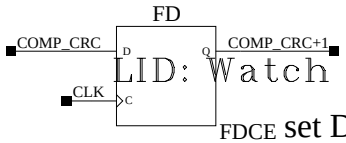
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
			DATE 10-3-2006_11:10	FILE STAGE2 . 2	PAGE 12A

CFEB/DMB Comparisons and Error Checks

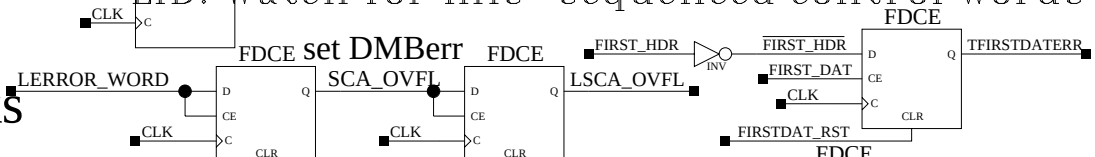


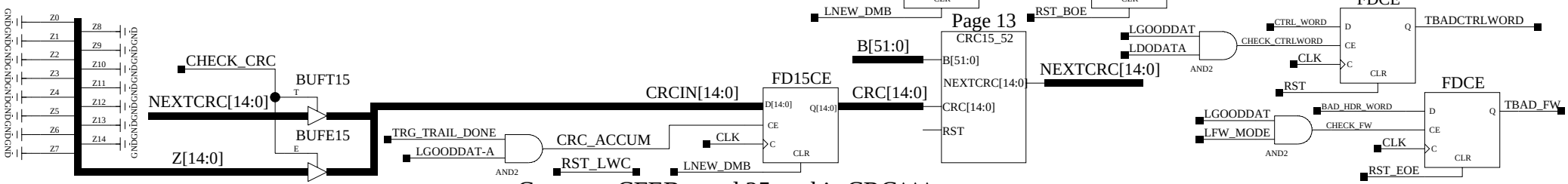






LID: Watch for mis-sequenced control words

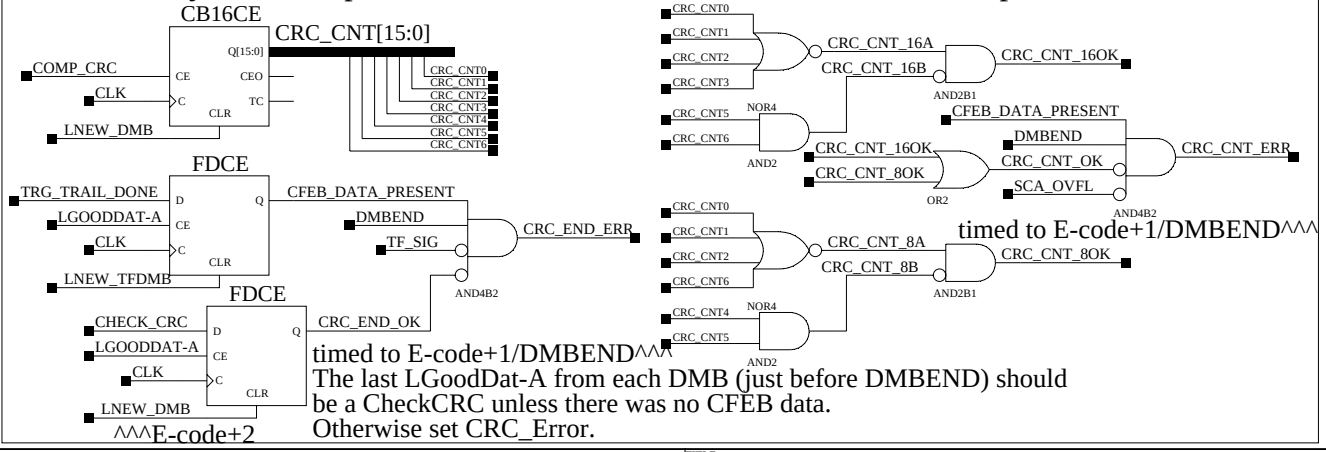




Load Zero on CRC when LWC loads ONE^^^

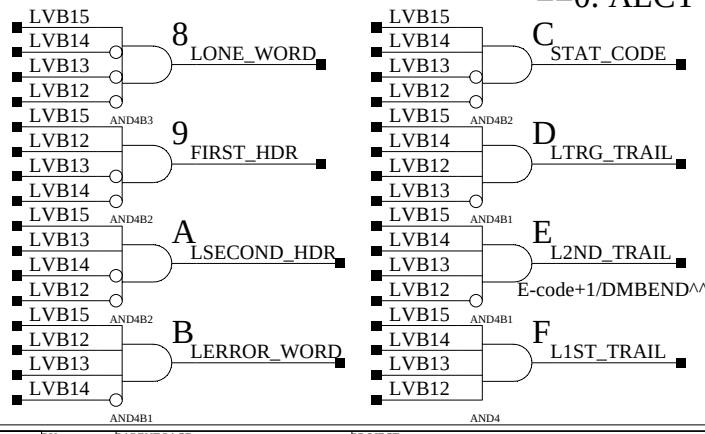
Compare CFEB word 25 to this CRC^^^

CFEB CRC Checks Done for this FIFO? Last non-control word S.B. CRC check. Verify that multiple of 8 /16 CRC Checks are done if CFEB data present.

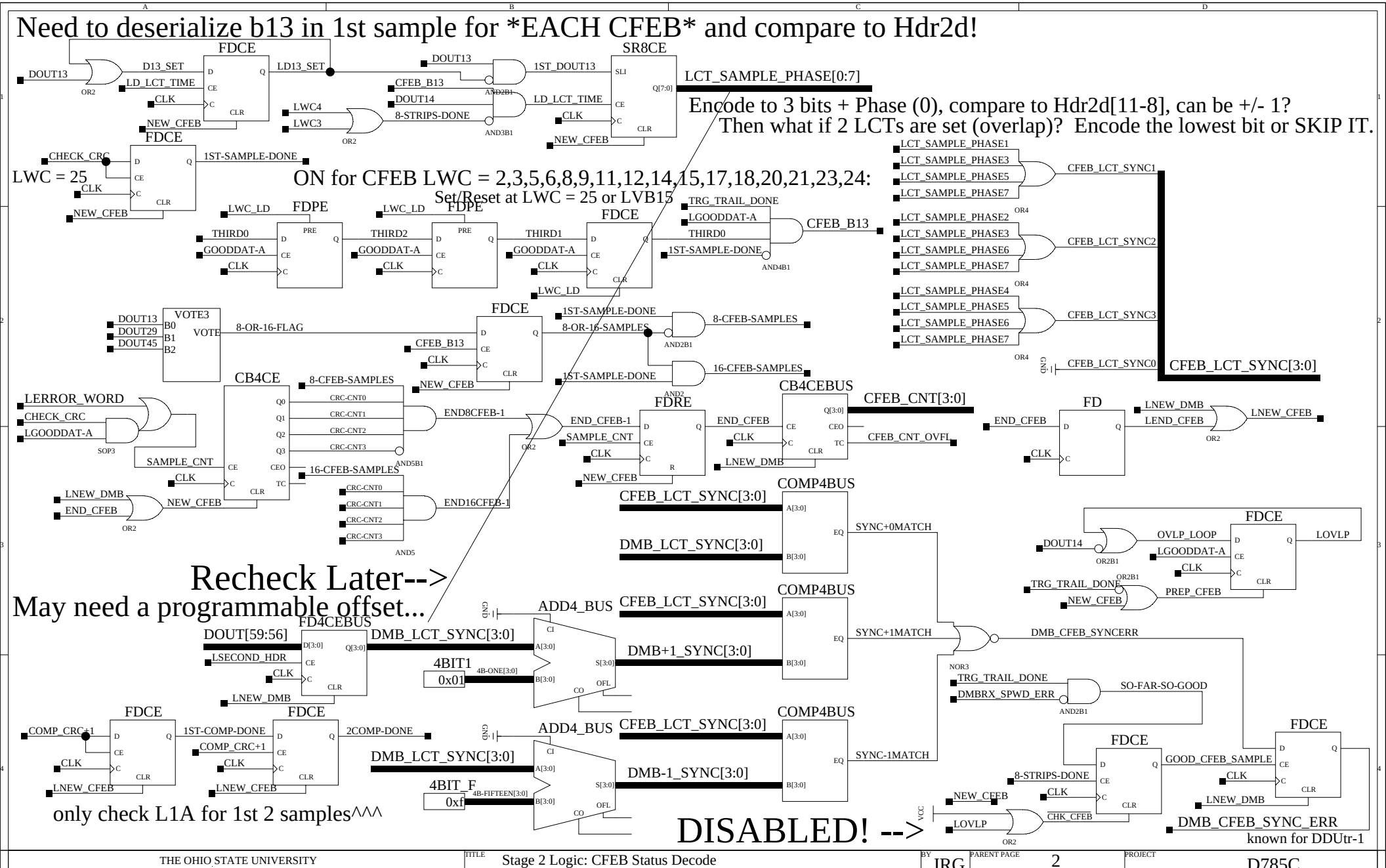


Latched Voted Special Bit Decode
Timed with LgoodDat=GoodDat+1

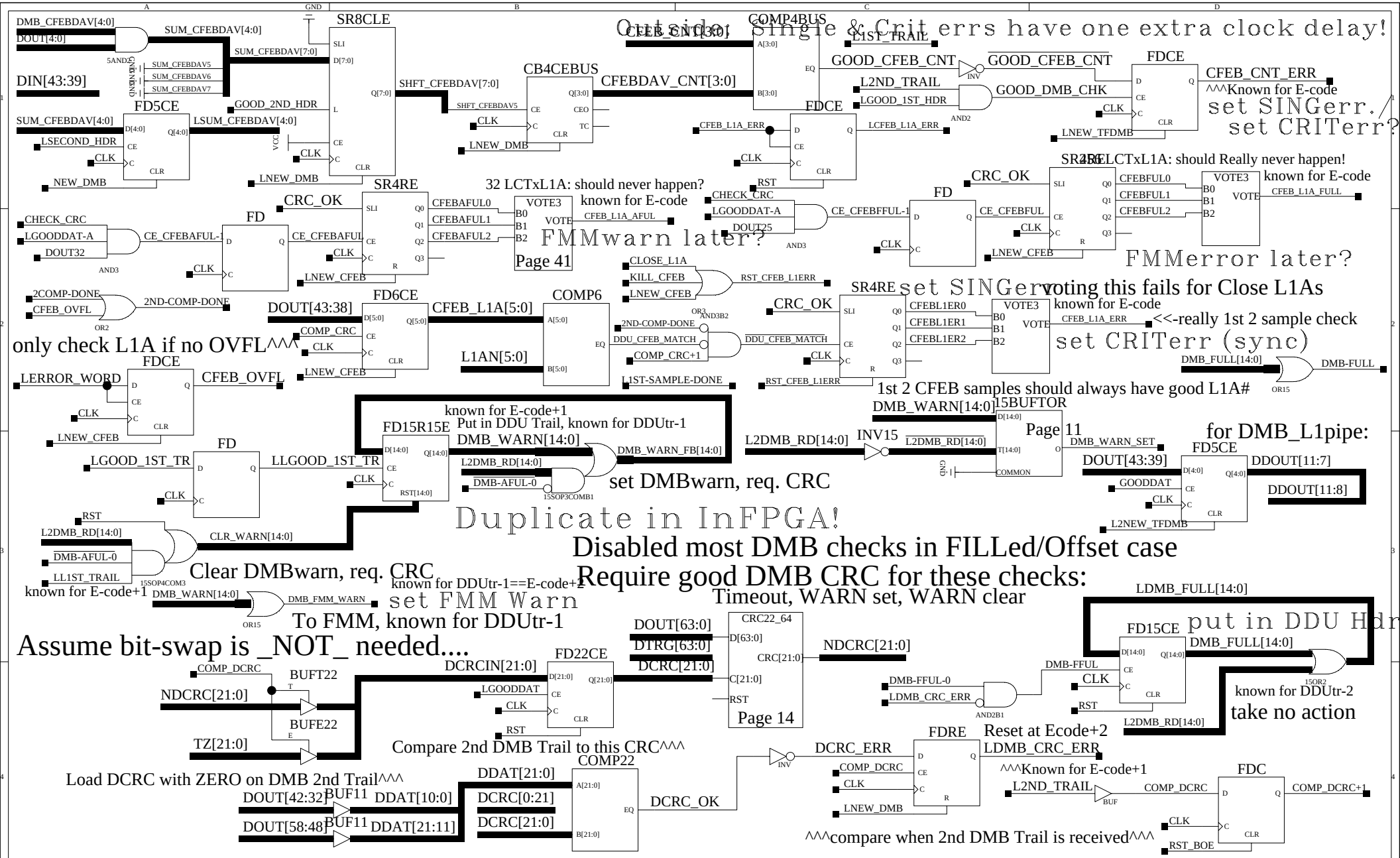
d-code, LVB11==1: TMB
==0: ALCT



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG DATE: 10-2-2006_13:18	PARENT PAGE: 2 FILE: STAGE2 . 3
		PROJECT: D785C	PAGE: 12B

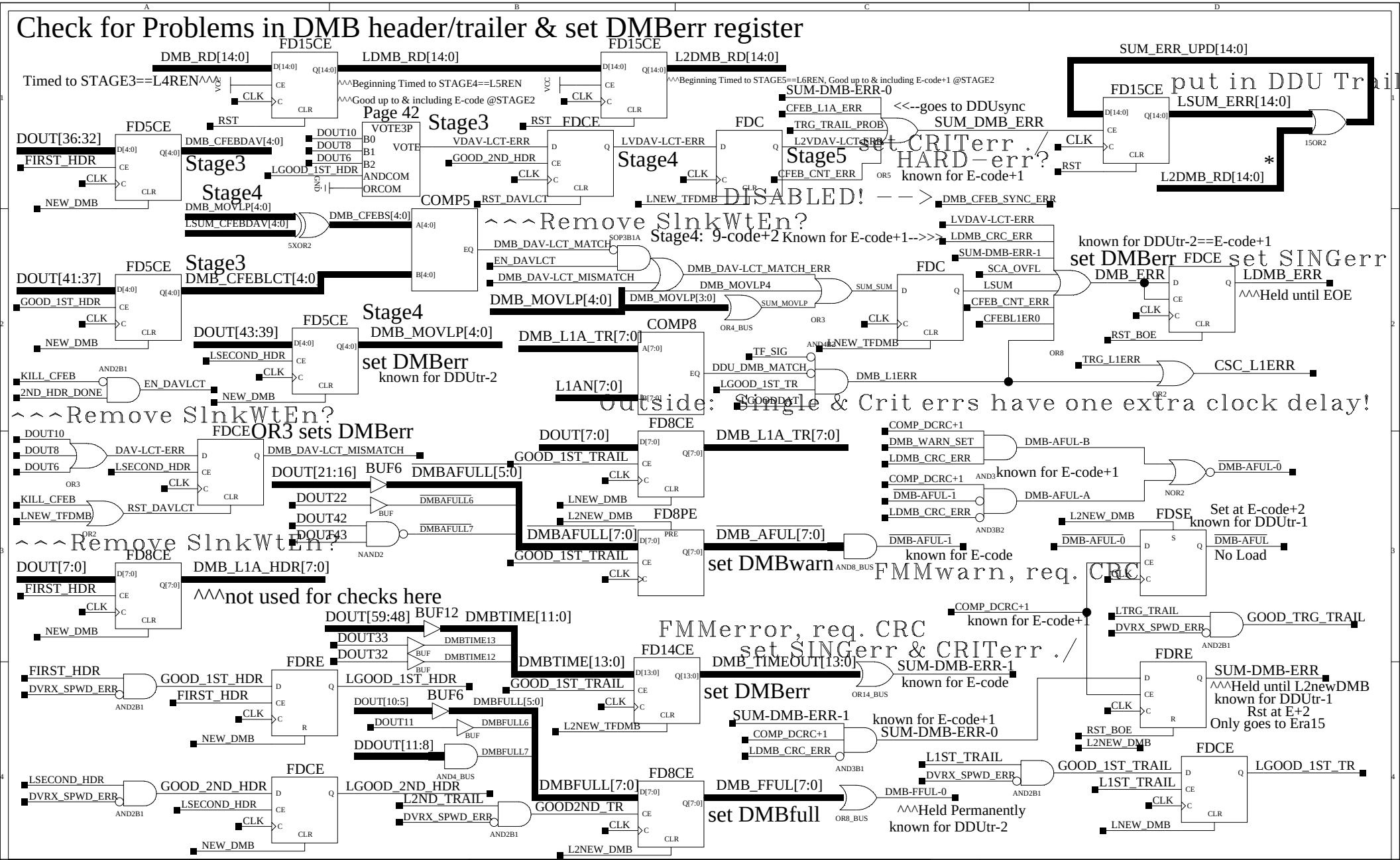


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Status Decode DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-13-2006_16:38	FILE: STAGE2 . 4	PAGE: 12C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Count & DMB CRC Check DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C	
		DATE: 9-19-2006_17:00		FILE: STAGE2 . 5	PAGE: 12D

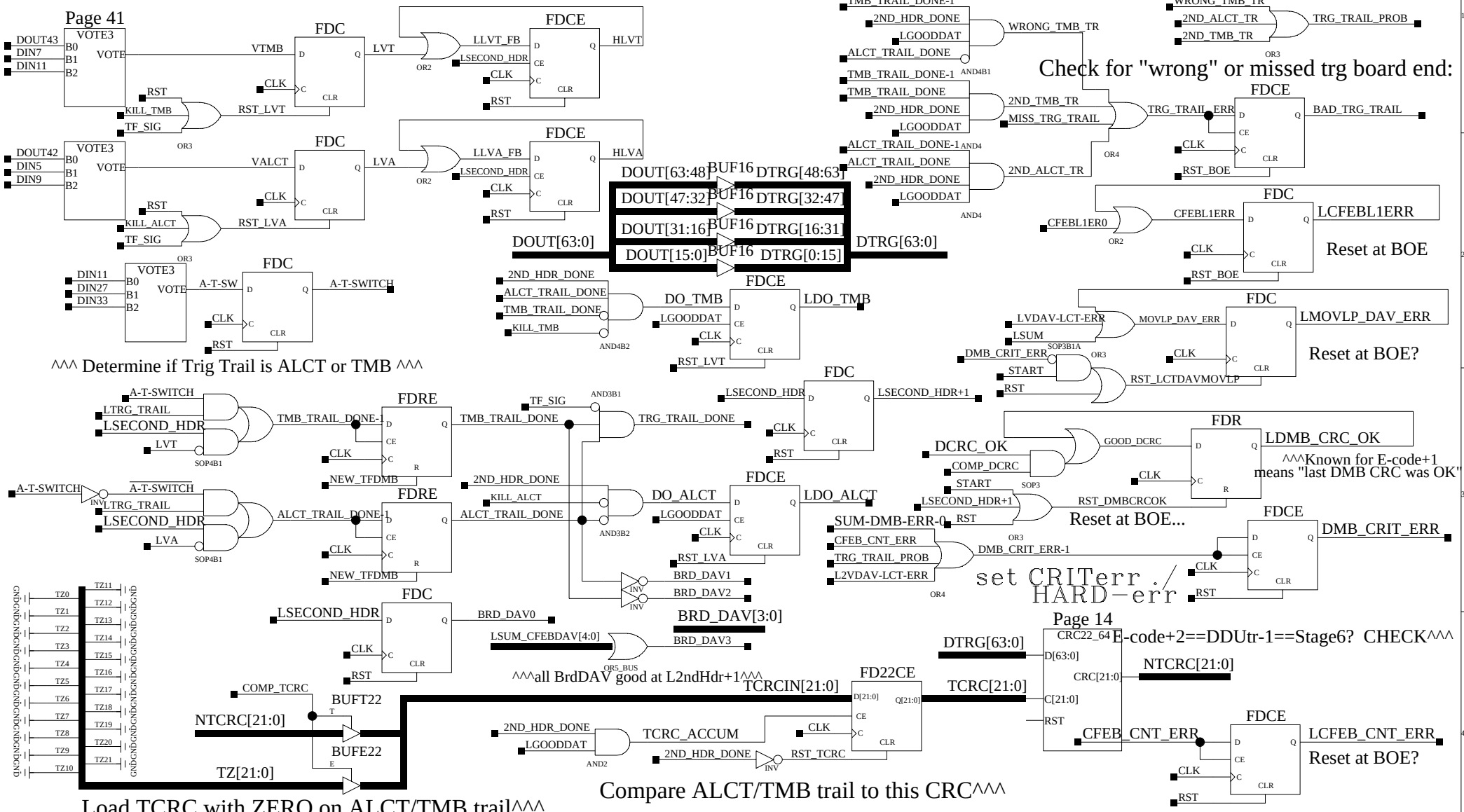
Check for Problems in DMB header/trailer & set DMBerr register



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DMB Status Checks DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2006_11:26	FILE: STAGE2 . 6	PAGE: 12E

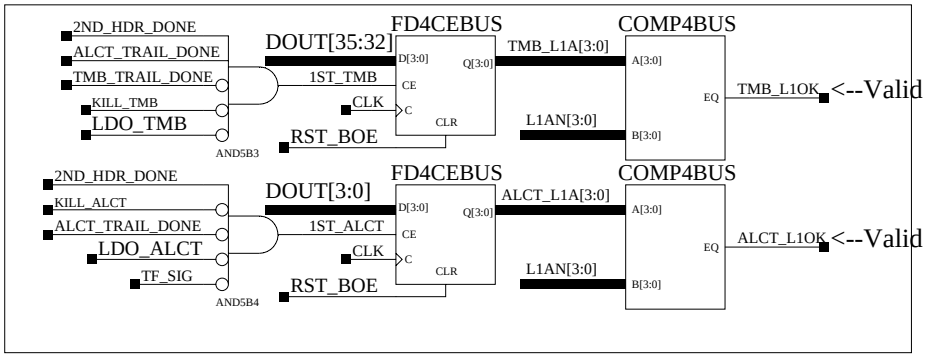
Trigger CRC Check Control: assume that TMB comes after ALCT!

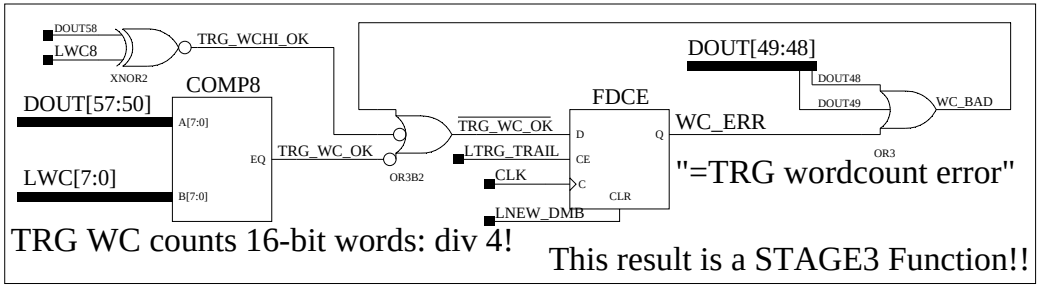
^^^affects L1A check: DoTMB, 1st_TMB/1st_ALCT

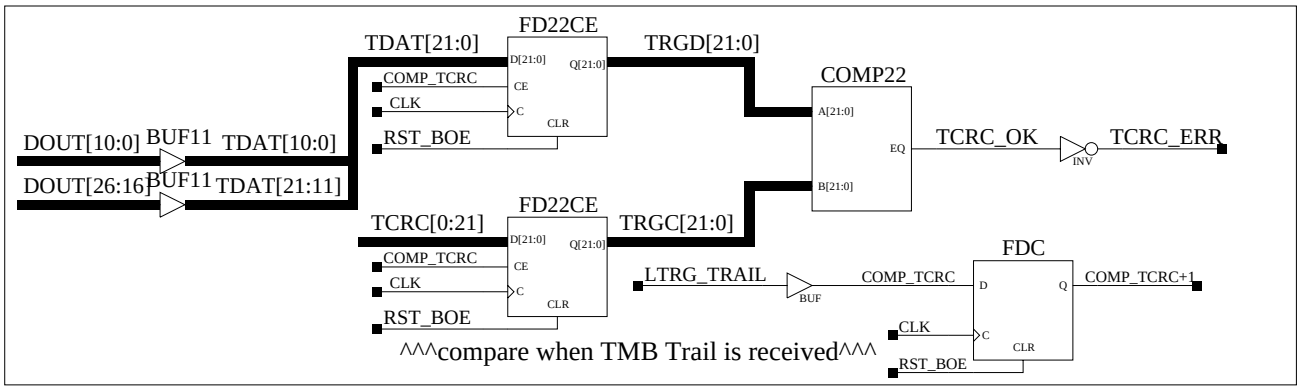


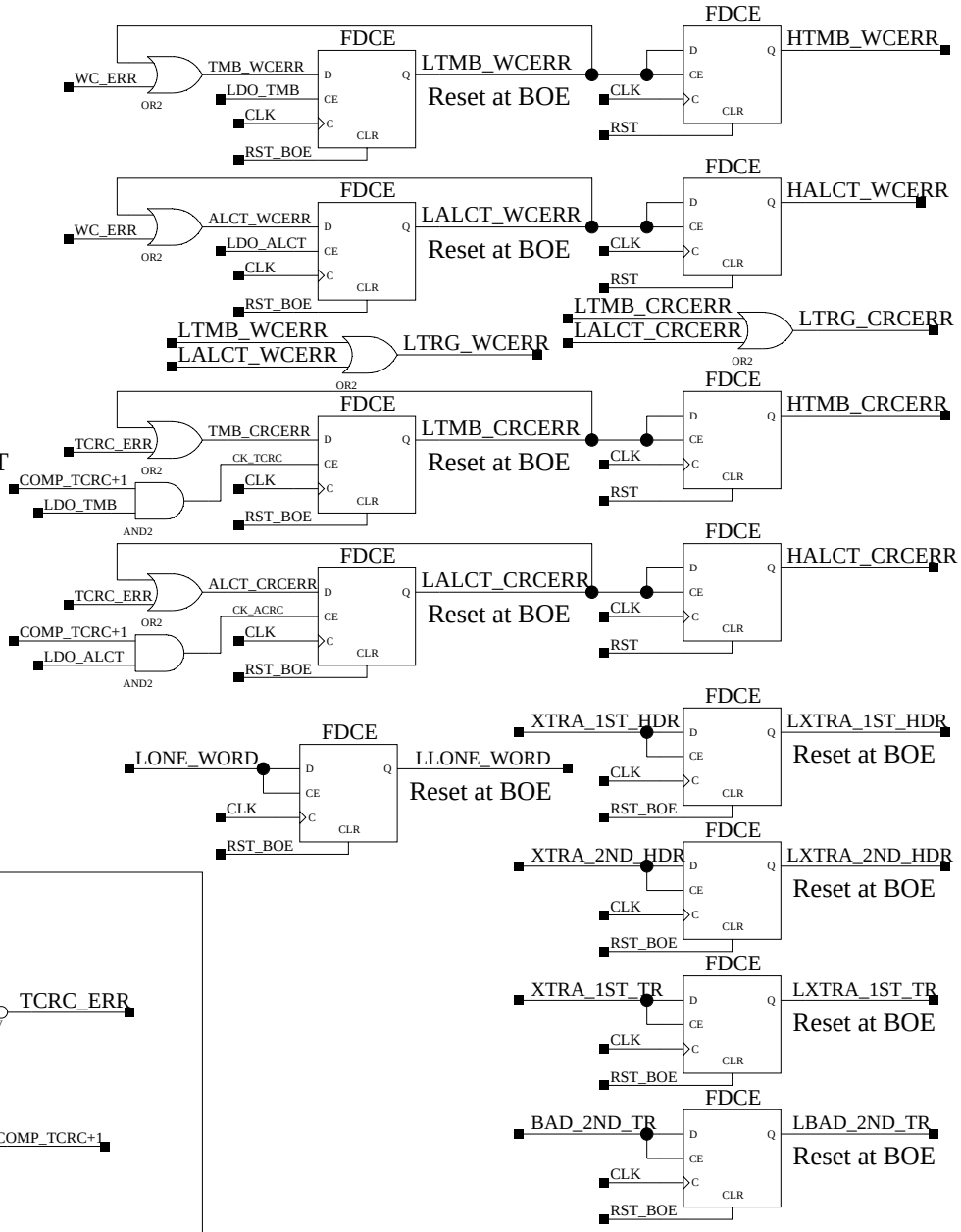
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Board Flags DDU Controller CMS CSC Electronics	BY: JRG DATE: 10-4-2006_15:13	PARENT PAGE: 2 FILE: STAGE2 . 7	PROJECT: D785C PAGE: 12F

Trigger Comparisons and Error Checks



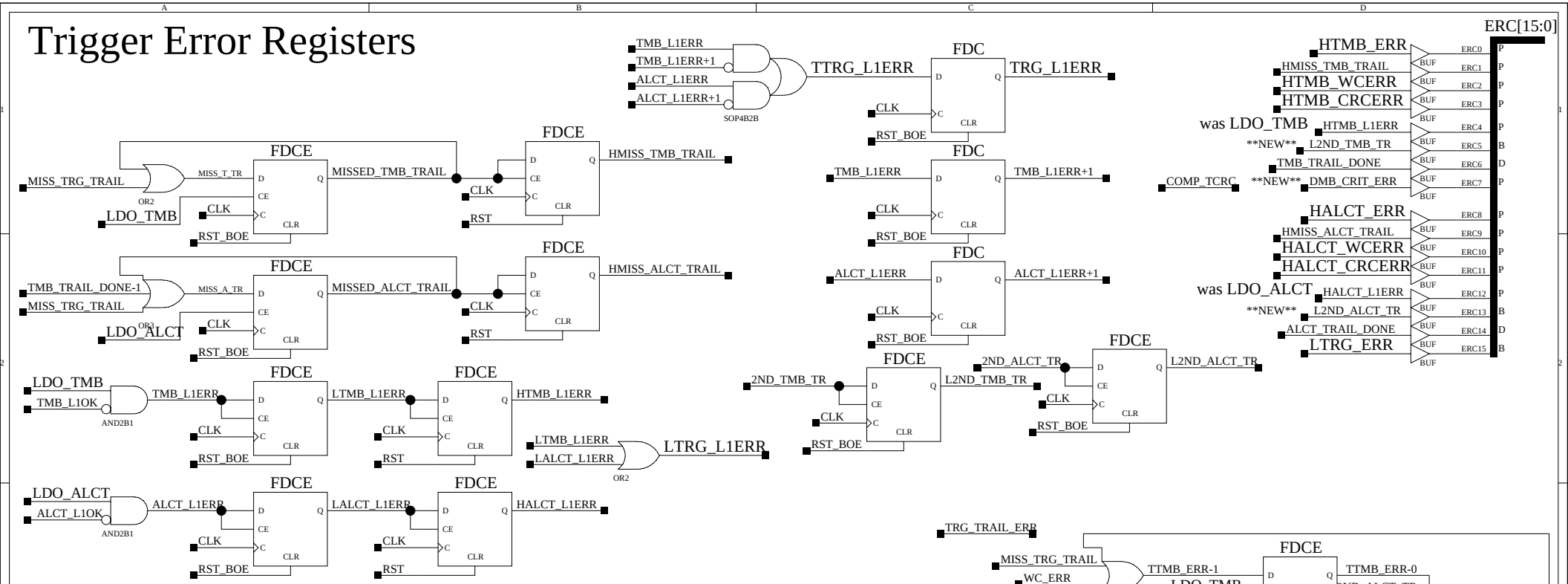






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Error Checks DDU Controller CMS CSC Electronics	BY: JRG DATE: 3-16-2006_15:43	PARENT PAGE: 2 FILE: STAGE2 . 8	PROJECT: D785C PAGE: 12G

Trigger Error Registers

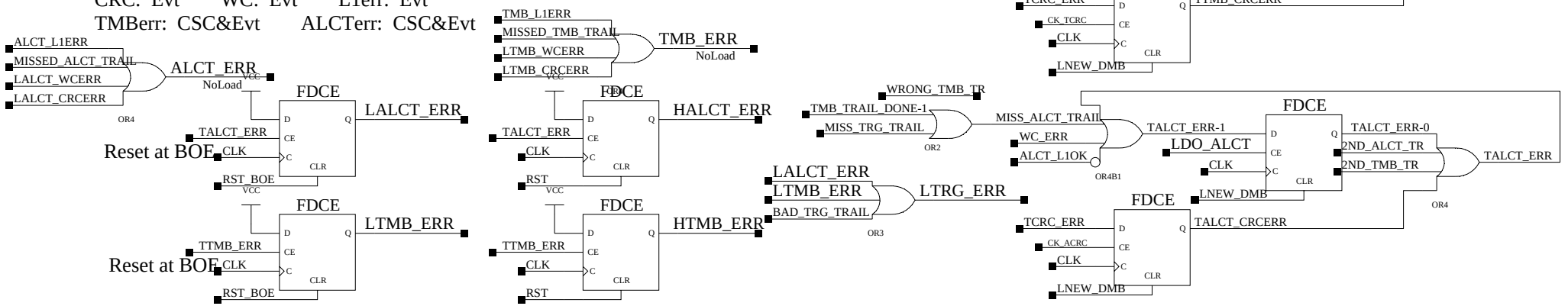


CSC case by LTRG_Trail+1?

TMB/ALCT need Err Reg's for CSC/EVT

CRC: Evt WC: Evt L1err: Evt

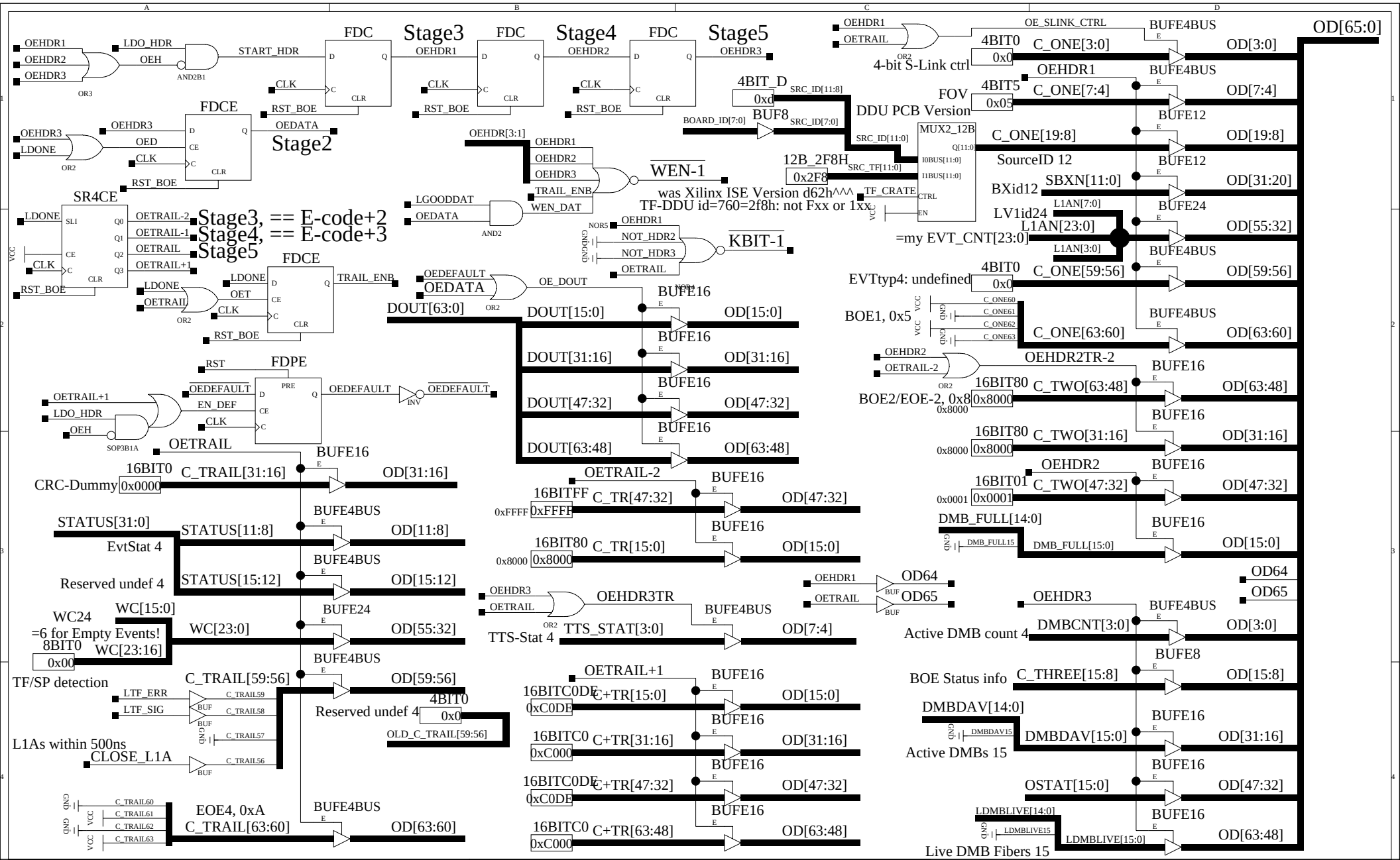
TMBerr: CSC&Evt ALCTerr: CSC&Evt



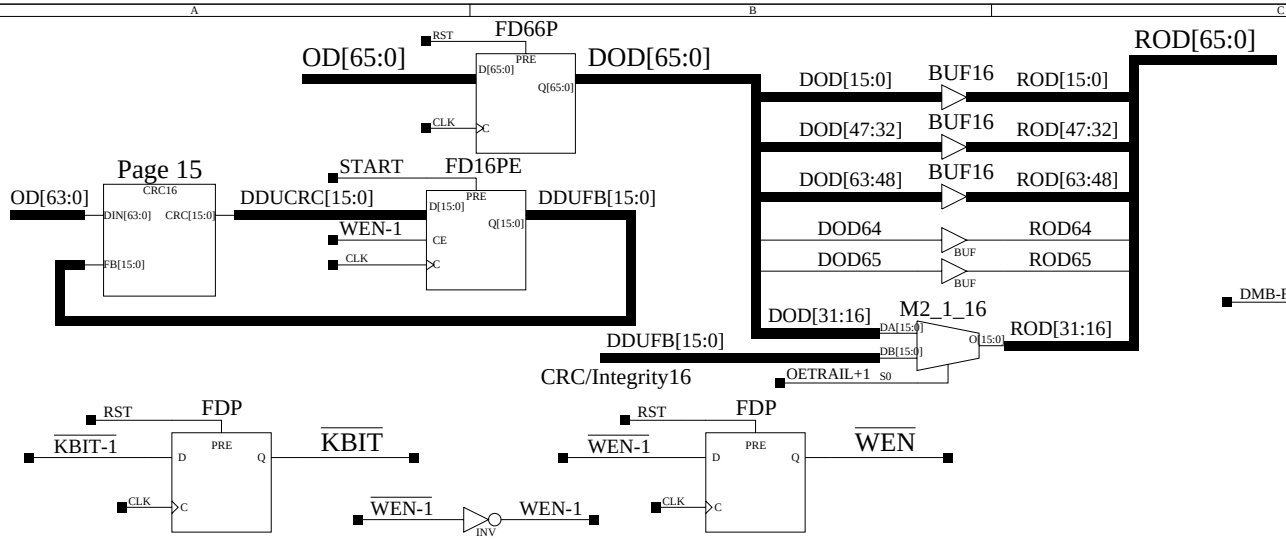
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

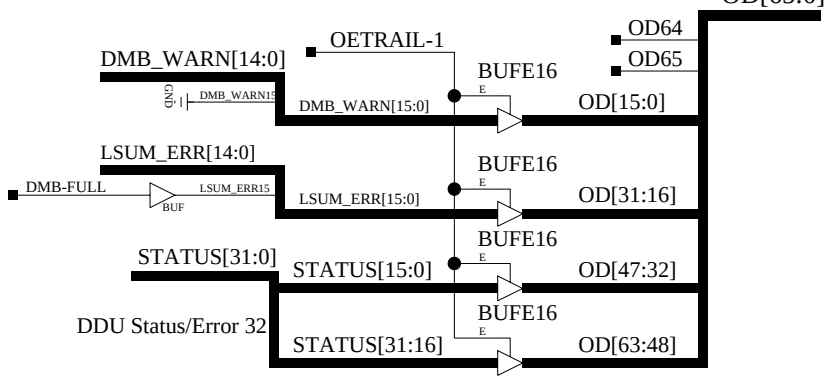
TITLE: Stage 2 Logic: Trigger Error Registers
DDU Controller
CMS CSC Electronics

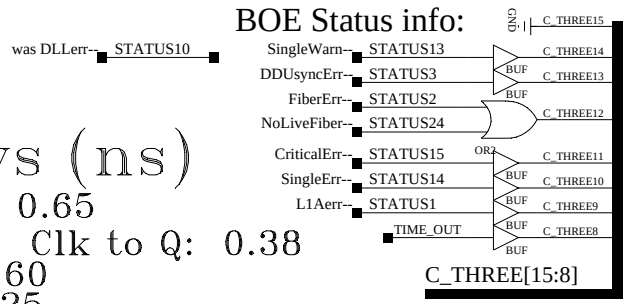
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
10-4-2006_15:14	STAGE2 . 9	12H



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DDU Header/Trailer Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 6-27-2006_11:21	PARENT PAGE: 2 FILE: STAGE2 . 10	PROJECT: D785C PAGE: 12I







DDU Timing Info

DDUctrl to InFIFO signals: 2" – 4", .3ns – .6ns
IRCLK has 4 loads, may slow signal by 0.1–0.5ns
CKFBout has normal drive, IRCLK has ~1.1ns Faster drive

FPGA I/O Delays (lvcmos33, ns)

IBUF: 0.92
IFD set/hold: 0.92/–0.12 Clk to Q: 0.65

OBUF: 2.33
OFD set/hold: 0.26/0.14 Clk to Q: 2.41
*modifiers for drive/slew settings:
6mA: add 2.60 for Slow, 1.28 for Fast
8mA: add 1.69 for Slow, 0.46 for Fast
12mA: add 1.18 for Slow, 0.26 for Fast
16mA: add 0.52 for Slow, 0.02 for Fast
24mA: +0.44 for Slow, –0.08 for Fast

FPGA CLB Delays (ns)

4–FG: 0.32 5–FG: 0.65
FD set/hold: 0/0.14 Clk to Q: 0.38
Sync. set–rst setup: 0.60
Async. pre–clr to Q: 1.25
SR16 Clk to Q: 3.12
SR32 Clk to Q: 3.49
SI set/hold: 0.34/0.01

TI FIFO I/O Delays (ns)

Meas'd on FIFO test board

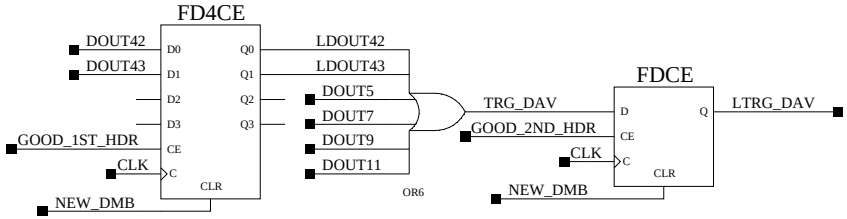
	Vcc: 3.38V	3.04V
RCLK to Empty (low state) Max: 3.6, Min: 2.5	3.02–3.18	3.20–3.29
to Not Empty (high state)	3.22–3.34	3.23–3.31
RCLK to Q11 False (low state) Max: 4.3, Min: 2.5	3.32–3.62	3.40–3.64
to Q11 True (high state)	3.31–3.87	3.51–4.06
to Q11 (low state)	3.22–3.34	3.2

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

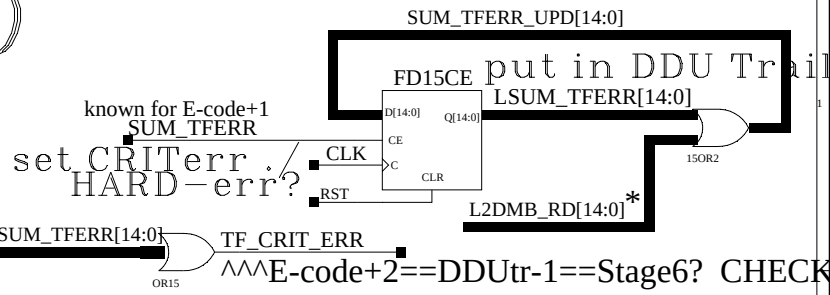
TITLE: DDU CRC Logic for SLINK/C.D.F. Compatibility
DDU Controller
CMS CSC Electronics

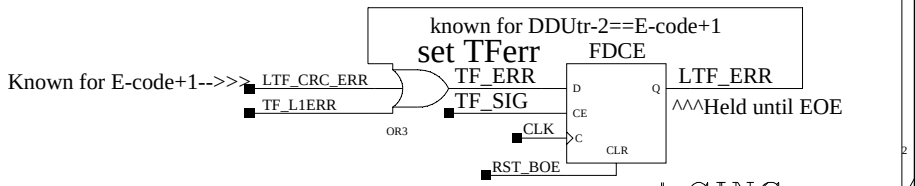
BY: JRG | PARENT PAGE: 2 | PROJECT: D785C
DATE: 6-1-2006_16:30 | FILE: STAGE2 . 11 | PAGE: 12J

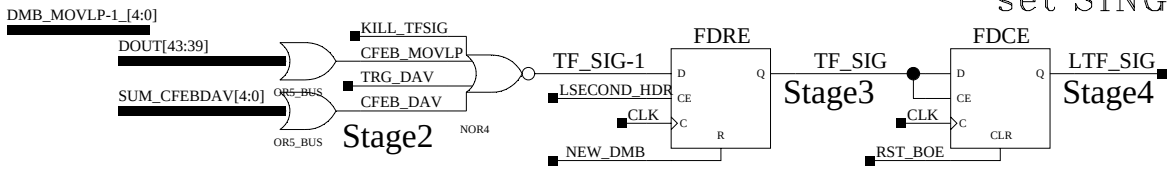
Check for Track Finder signal, record TF errors

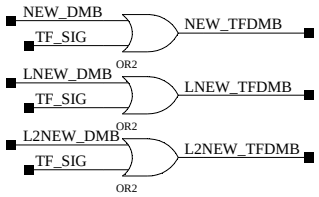


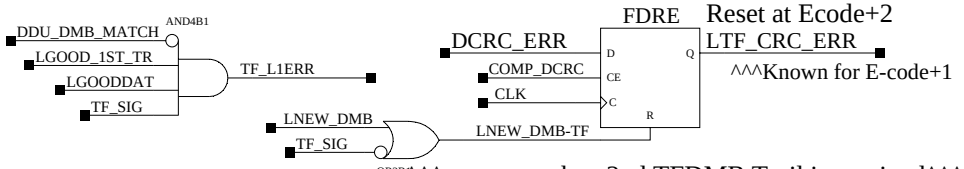
END



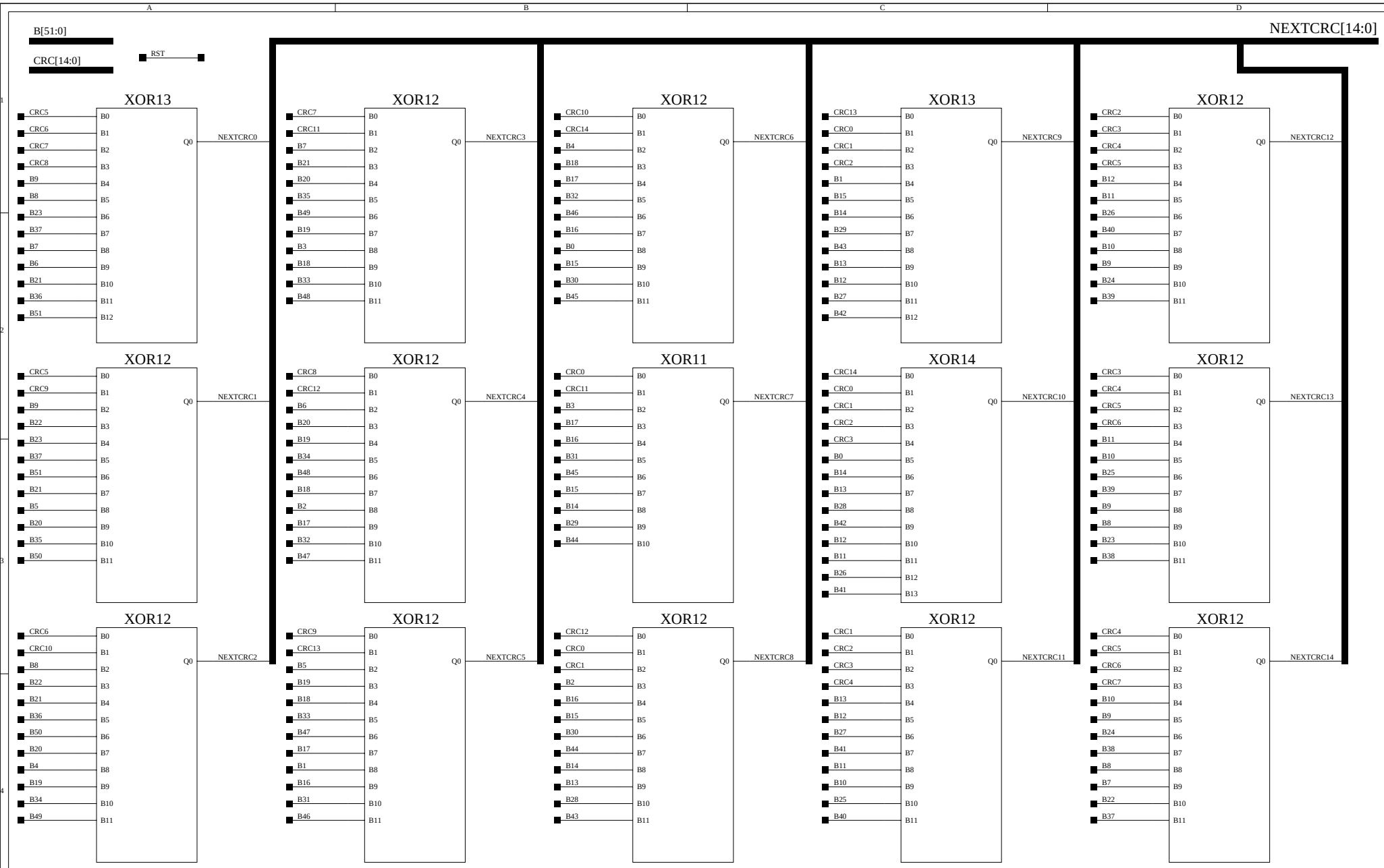




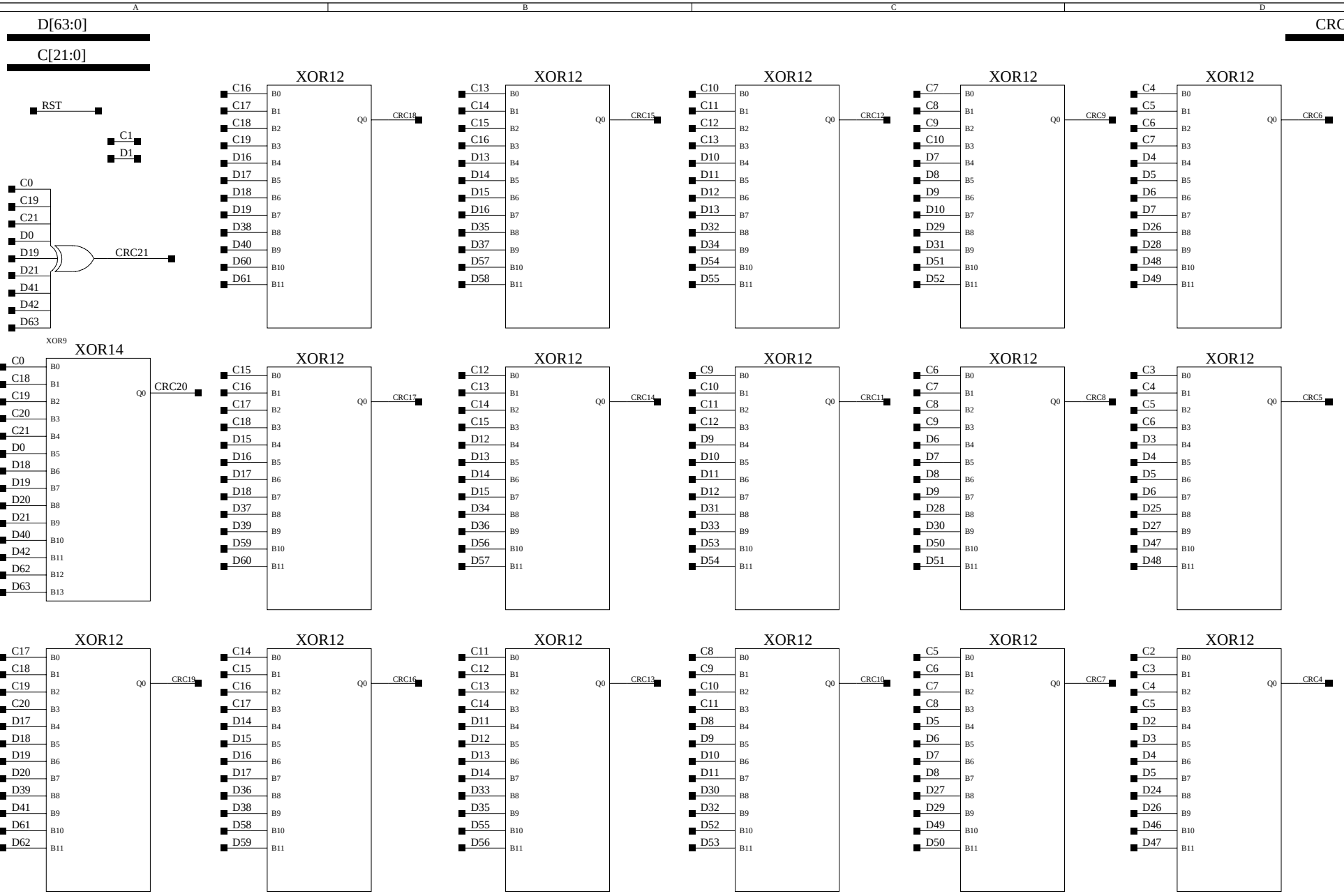




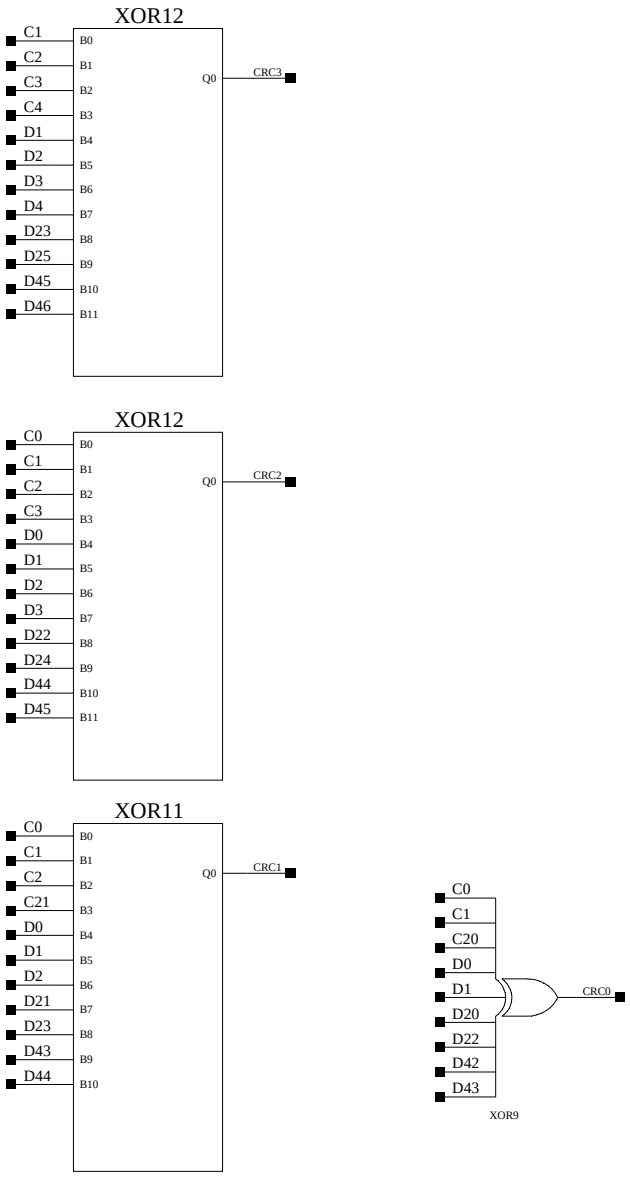
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DMB Status Checks DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 8-15-2006_15:15	FILE: STAGE2 . 12	PAGE: 12K



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC15, 52-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12B	PROJECT: D785C
		DATE: 1-26-2005_11:33	FILE: CRC15_52 . 1	PAGE: 13

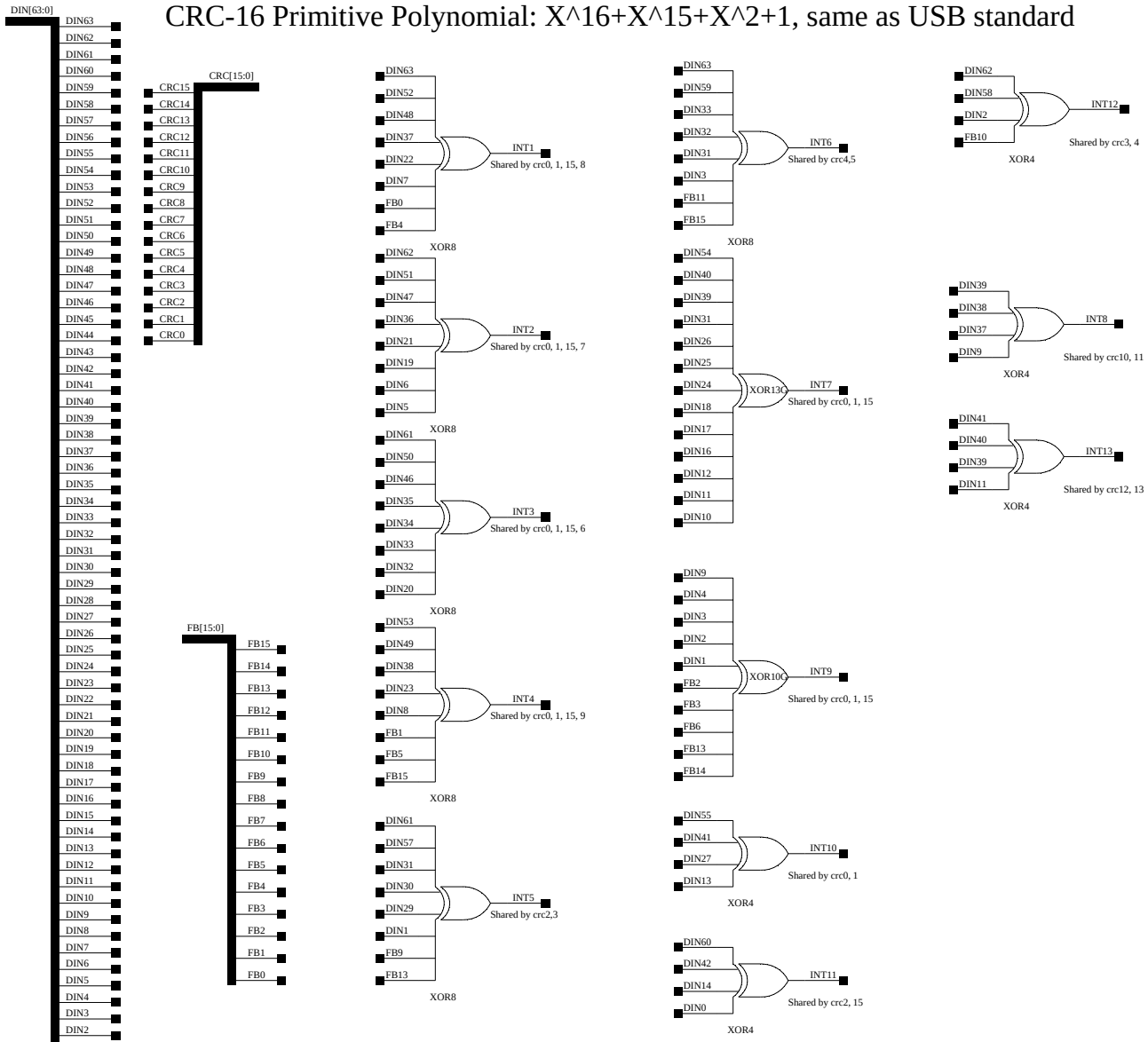


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C
		DATE: 1-26-2005_11:33	FILE: CRC22_64 . 1	PAGE: 14

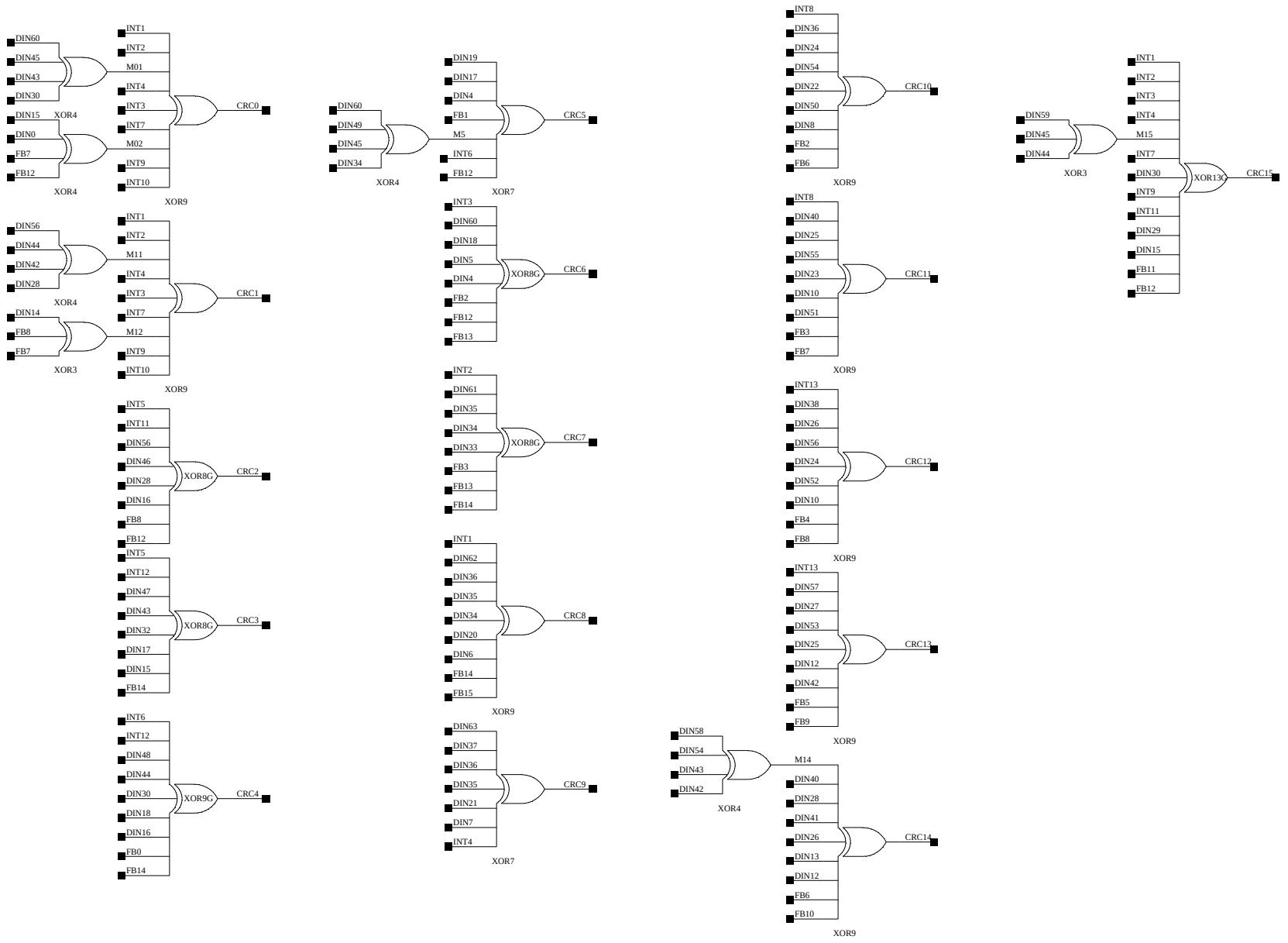


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C	
		DATE: 1-26-2005_11:34		FILE: CRC22_64 . 2	PAGE: 14A

CRC-16 Primitive Polynomial: X^16+X^15+X^2+1, same as USB standard



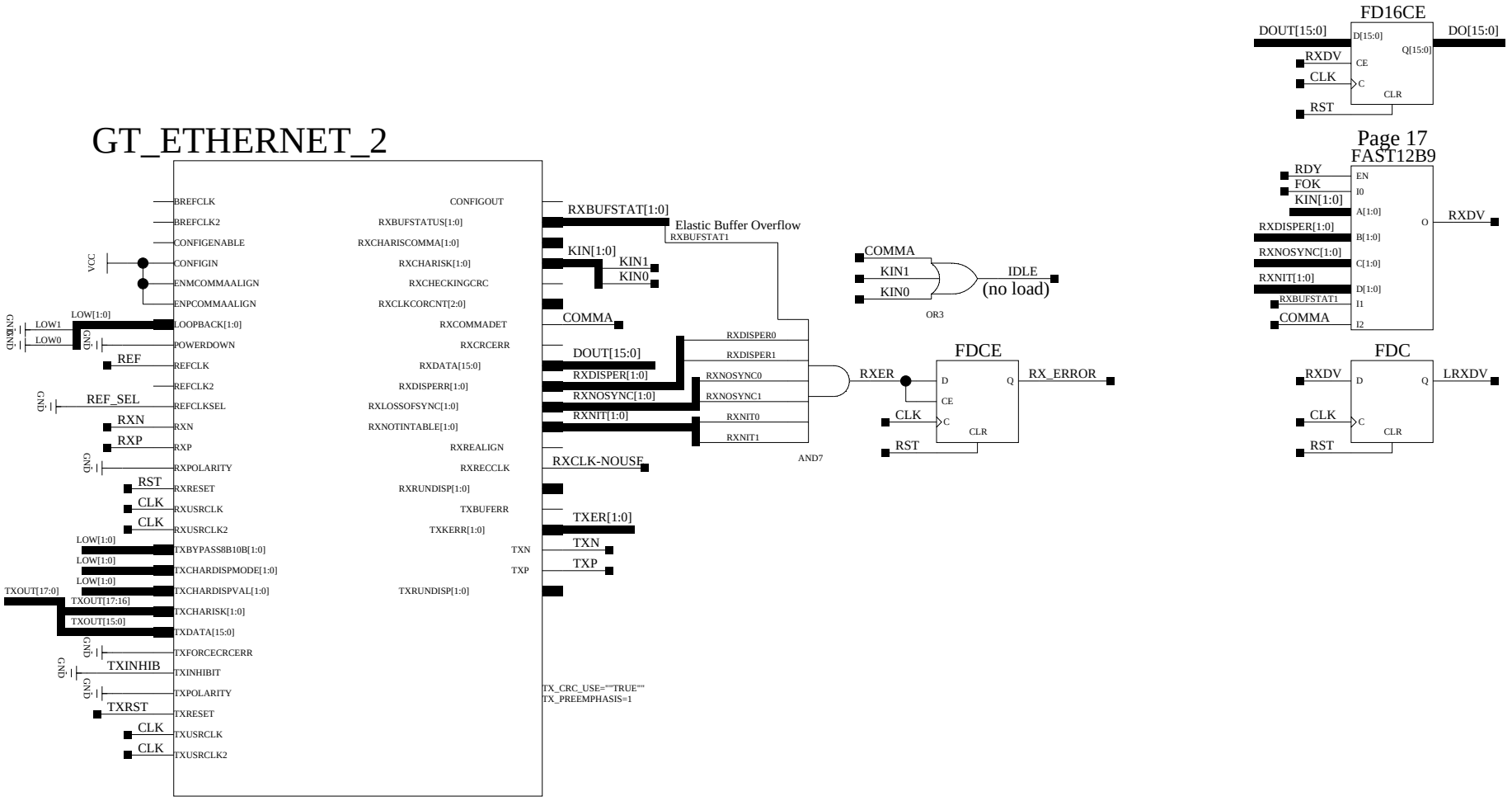
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	SLINK CRC16 Calculation, common components DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
			DATE 2-7-2005_17:50	FILE CRC16 . 1	PAGE 15



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE SLINK CRC16 Calculation DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
		DATE 2-7-2005_17:50	FILE CRC16 . 2	PAGE 15A

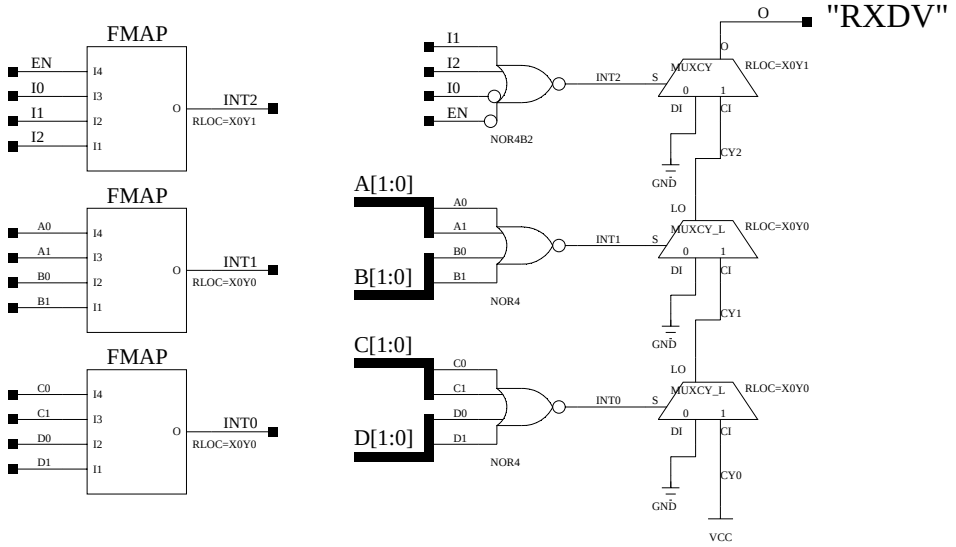
Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.

---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.



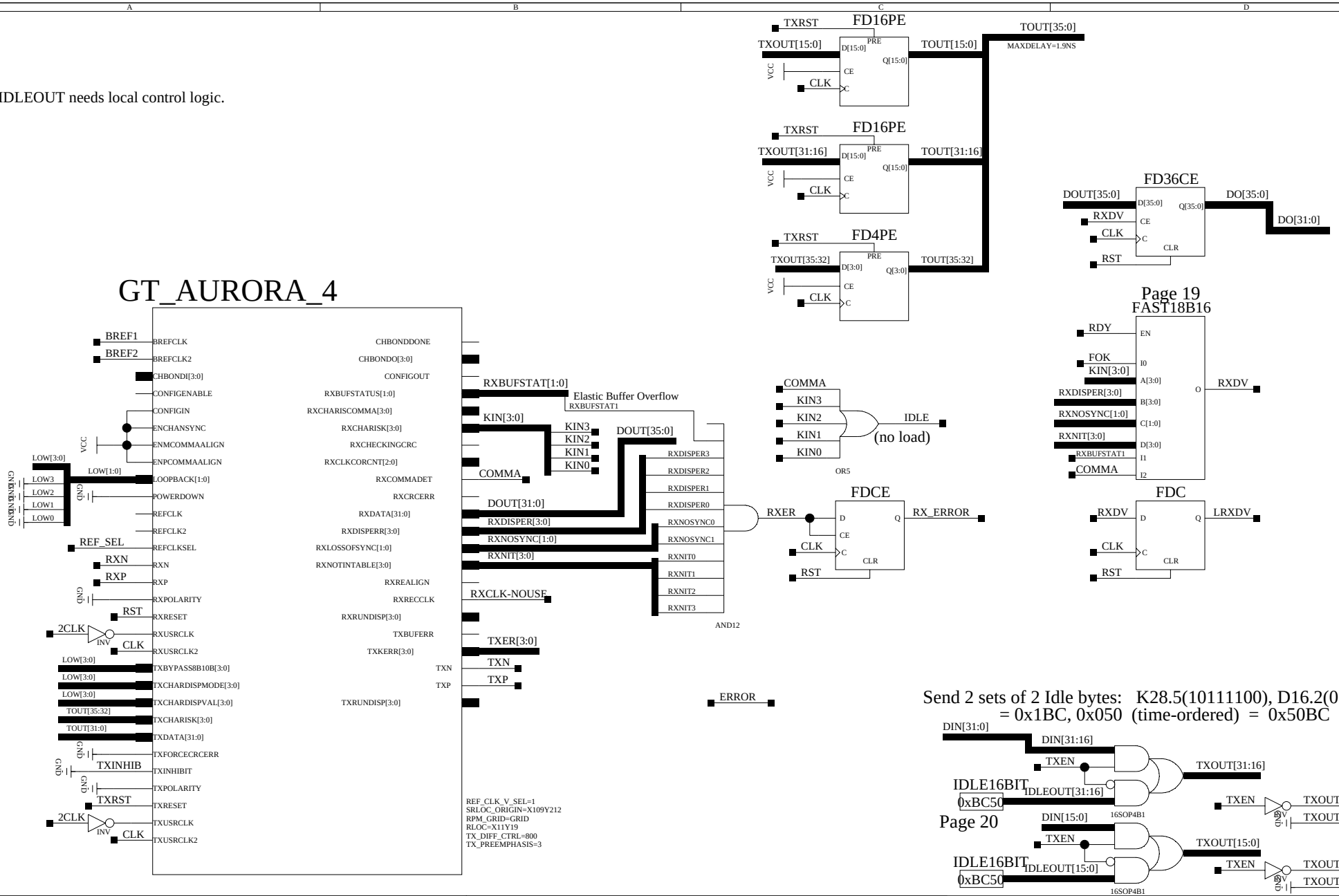
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE	Gigabit Ethernet Tranceiver DDU Controller Logic CMS CSC Electronics		
BY JRG	PARENT PAGE 2E	PROJECT D785C	
DATE 7-18-2005_16:14		FILE OUT_GBE . 1	PAGE 16



XILINX			JRG
Title:	FAST12B9		
Comments:	Custom Logic for DDU similar to: AND12B9		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

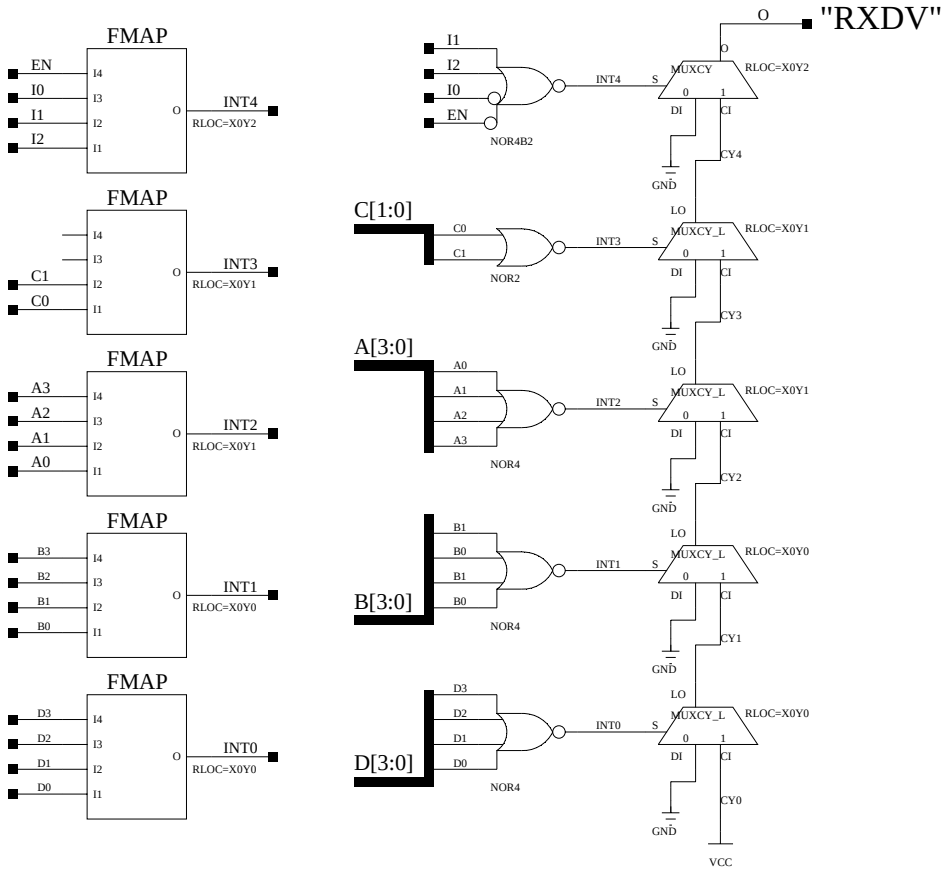
IDLEOUT needs local control logic.



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Multi Gigabit Tranceiver
DDU Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2E	D785C
DATE	FILE	PAGE
7-18-2005_16:15	OUT_UNIT . 1	18



XILINX

JRG

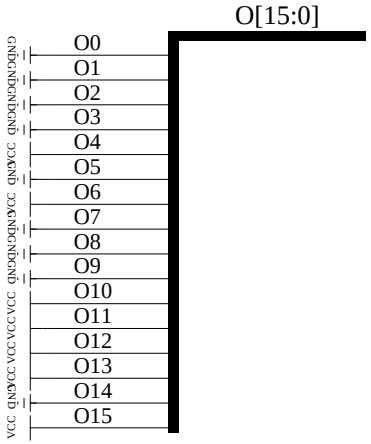
Title:	FAST13B10
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)
Date: 19th December 2003	Ver: 1
Sheet Size: B	Rev: A

Send 2 Idle bytes:

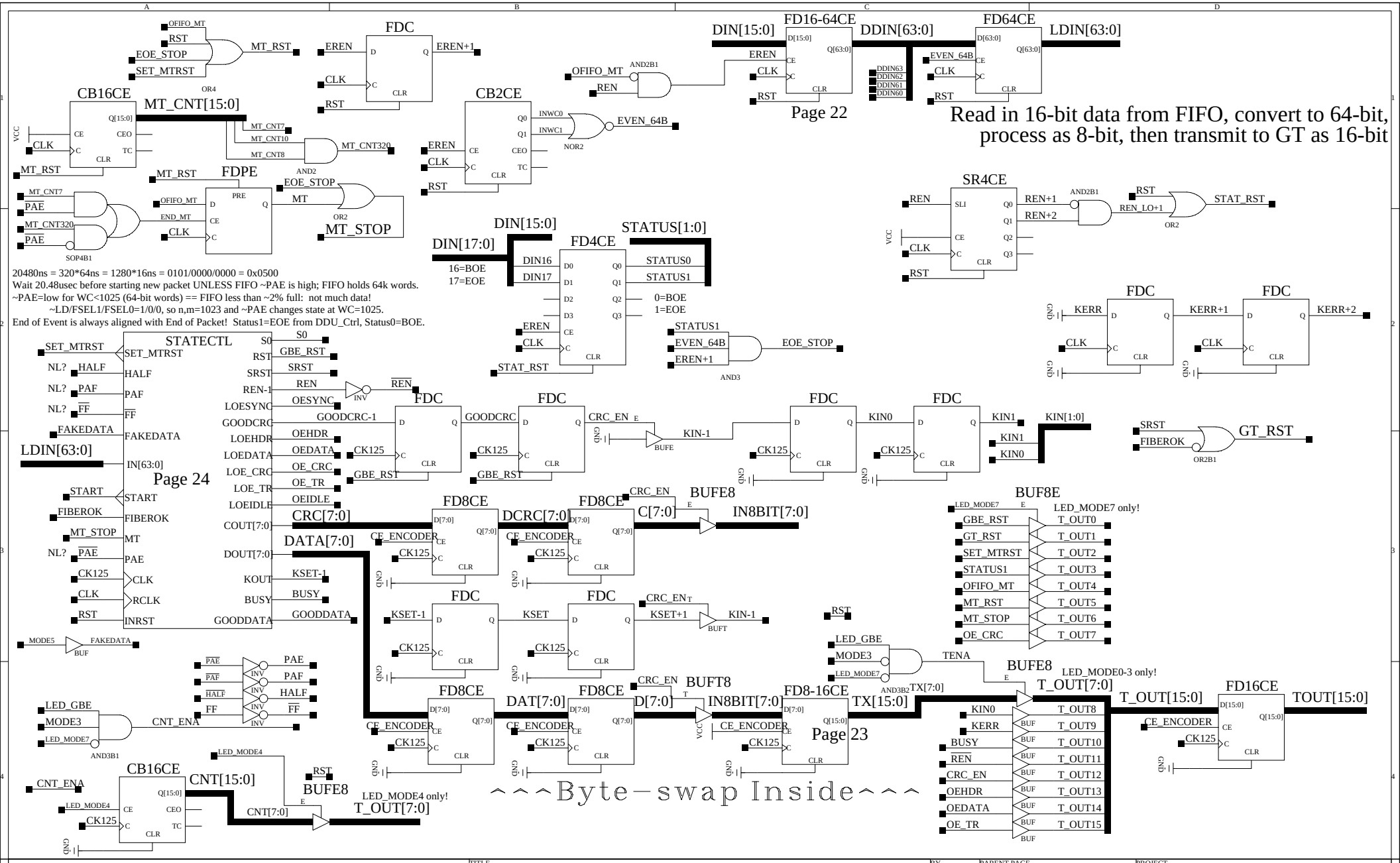
K28.5(10111100)+D16.2(01010000)

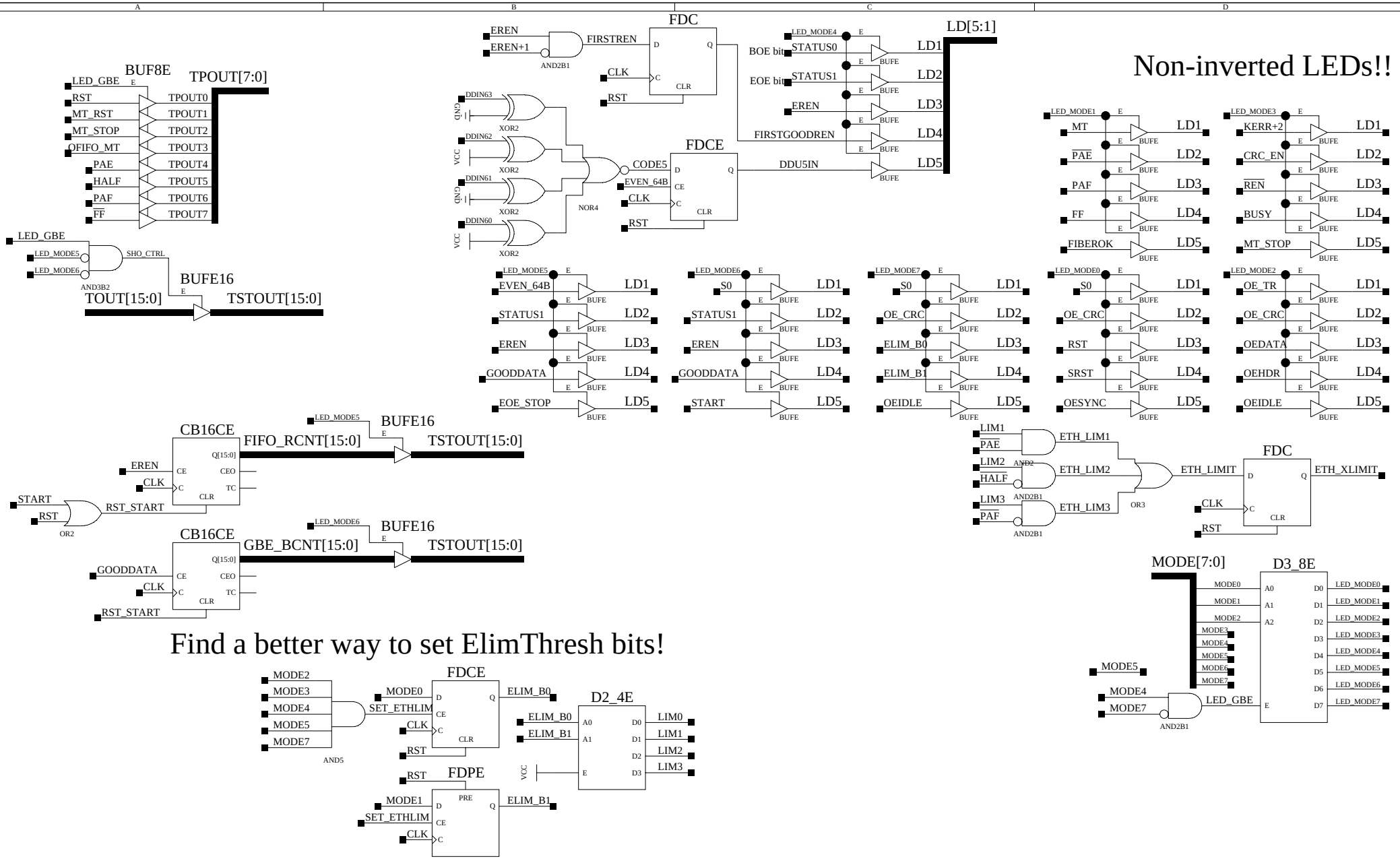
= 0x1BC + 0x050 (time-ordered)

= 0xBC50 (in parallel)

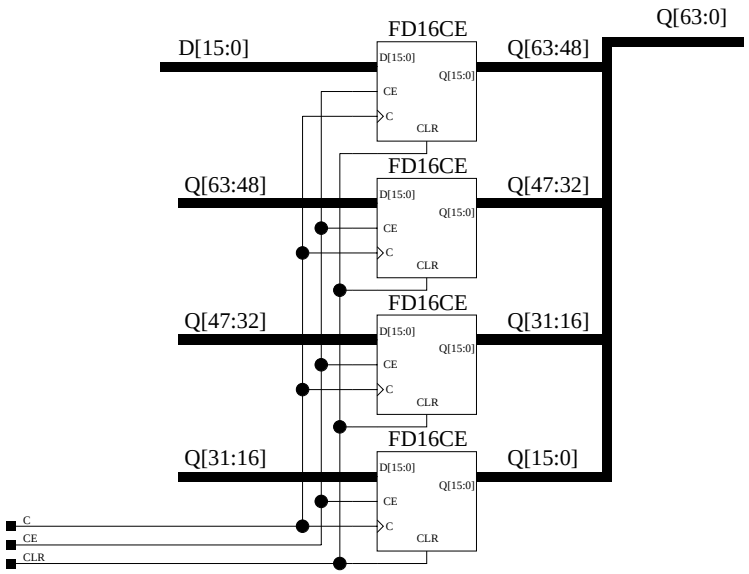


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Gigabit "Idle" Code Constant Bus Settings CMS CSC Electronics	BY: JRG	PARENT PAGE: 18	PROJECT: D785C	
		DATE: 1-26-2005_11:43		FILE: IDLE16BIT . 1	PAGE: 20

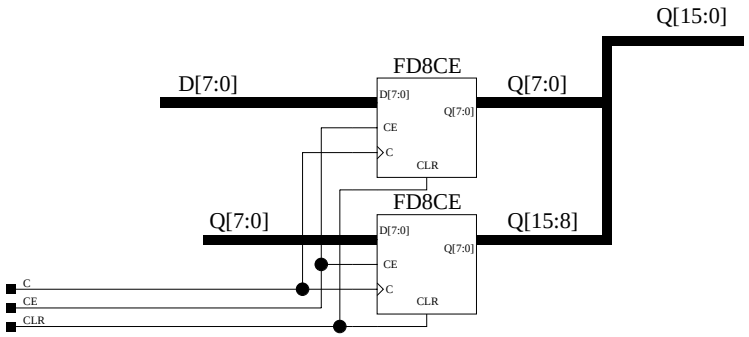

Read in 16-bit data from FIFO, convert to 64-bit, process as 8-bit, then transmit to GT as 16-bit
20480ns = 320*64ns = 1280*16ns = 0101/0000/0000 = 0x0500
Wait 20.48usec before starting new packet UNLESS FIFO ~PAE is high; FIFO holds 64k words.
~PAE=low for WC<1025 (64-bit words) == FIFO less than ~2% full: not much data!
~LD/FSEL1/FSEL0=1/0/0, so n,m=1023 and ~PAE changes state at WC=1025.
End of Event is always aligned with End of Packet! Status1=EOE from DDU_Ctrl, Status0=BOE.
Page 22
Page 24
Page 23
^^^Byte-swap Inside^^^
STATECTL
CB16CE
CB2CE
FDC
FD16-64CE
FD64CE
FDPE
FD4CE
FD8CE
FD8-16CE
SR4CE
FDCE
BUFE8
BUFT8
BUF8E
FD16CE
MT_CNT[15:0]
DIN[15:0]
DDIN[63:0]
LDIN[63:0]
STATUS[1:0]
CRC[7:0]
DATA[7:0]
DCRC[7:0]
C[7:0]
IN8BIT[7:0]
D[7:0]
DAT[7:0]
TX[15:0]
T_OUT[7:0]
T_OUT[15:0]
TOUT[15:0]
CNT[15:0]
KIN-1
KIN[1:0]
KSET-1
KSET+1
KERR+1
KERR+2
GT_RST
LED_MODE7 only!
LED_MODE0-3 only!
LED_MODE4 only!
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
Ethernet Control
DDU Ethernet Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 2F
PROJECT D785C
DATE 8-1-2005_12:56
FILE ETHCNTRL . 1
PAGE 21



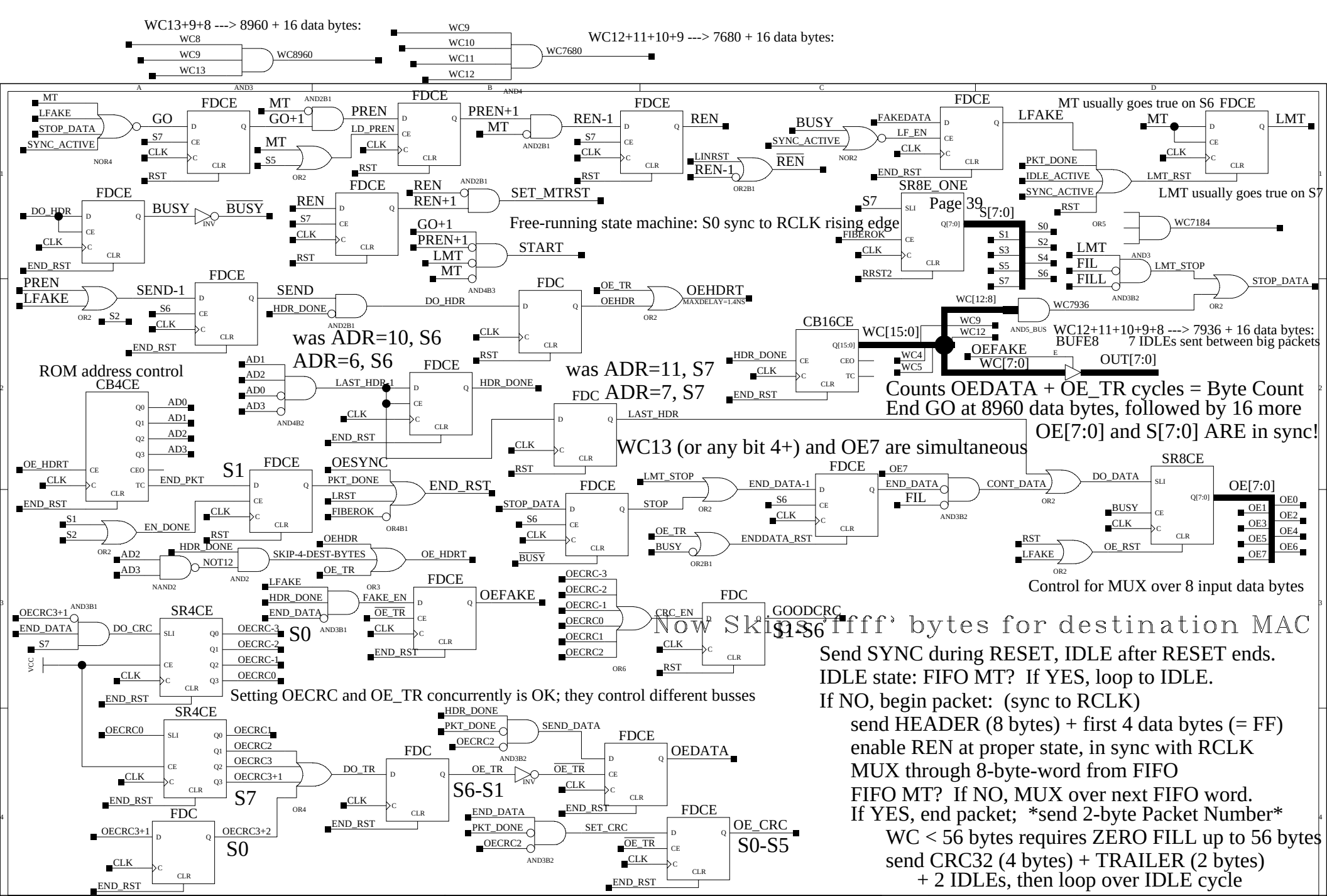
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2F	PROJECT: D785C	
		DATE: 7-22-2005_16:55		FILE: ETHCNTRL . 2	PAGE: 21A



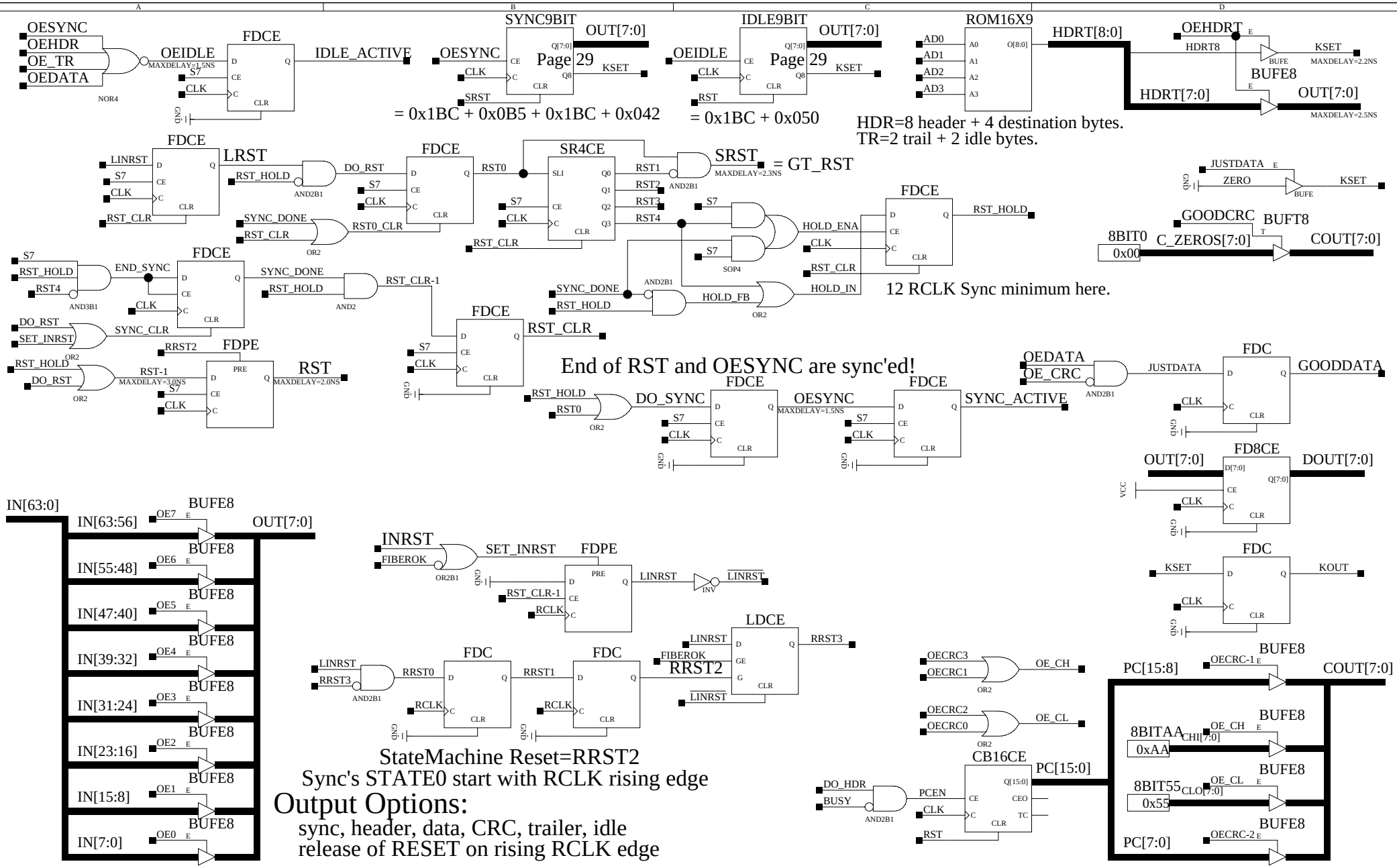
XILINX		JRG	
Title:	VIRTEX Family FD16-64CE Macro		
Comments:	16-64 Bit Bus Matching Register with Asynchronus Clear and Chip Enable		
Date:	2nd February 2004	Ver:	1
Sheet Size: B		Rev:	A



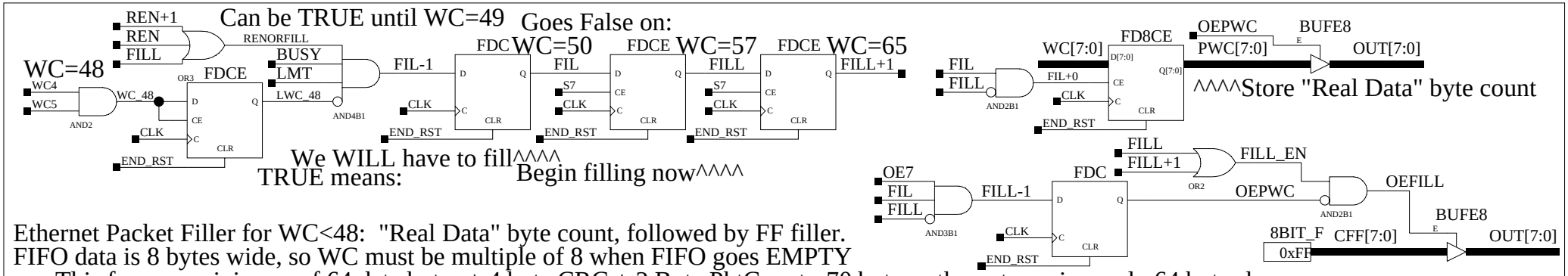
XILINX	JRG	
Title:	VIRTEX Family FD8-16CE Macro	
Comments:	8-16-Bit Bus Matching Register with Asynchronus Clear and Chip Enable	
Date:	4th February 2004	Ver: 1
Sheet Size: B		Rev: A



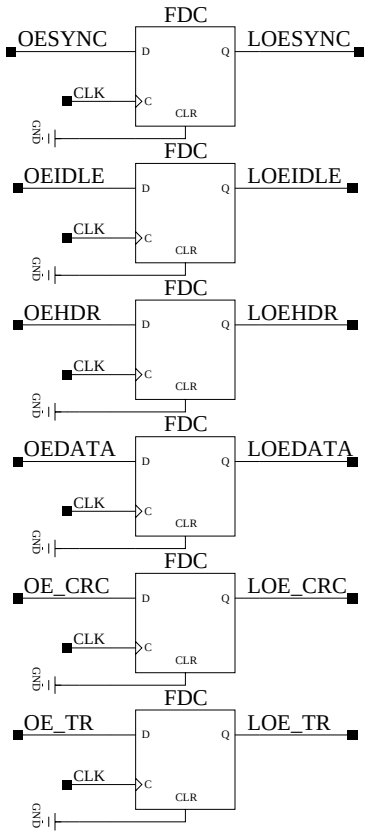
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 21A	PROJECT: D785C
		DATE: 7-29-2005_13:26	FILE: STATECTL . 1	PAGE: 24



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 21A	PROJECT: D785C
		DATE: 7-18-2005_16:19	FILE: STATECTL . 2	PAGE: 24A



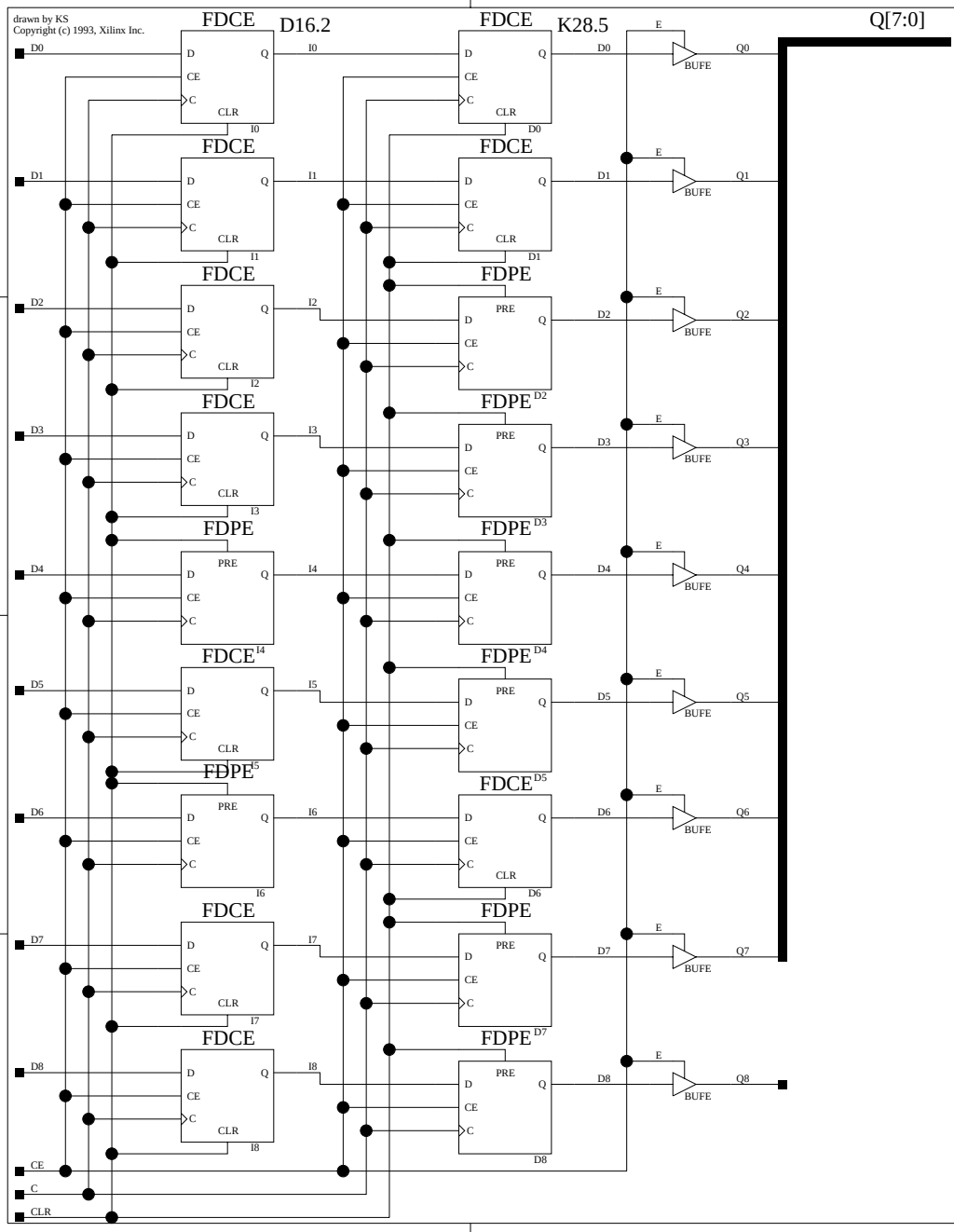
Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: JTAG Control Signals
DDU Ethernet Logic
CMS CSC Electronics

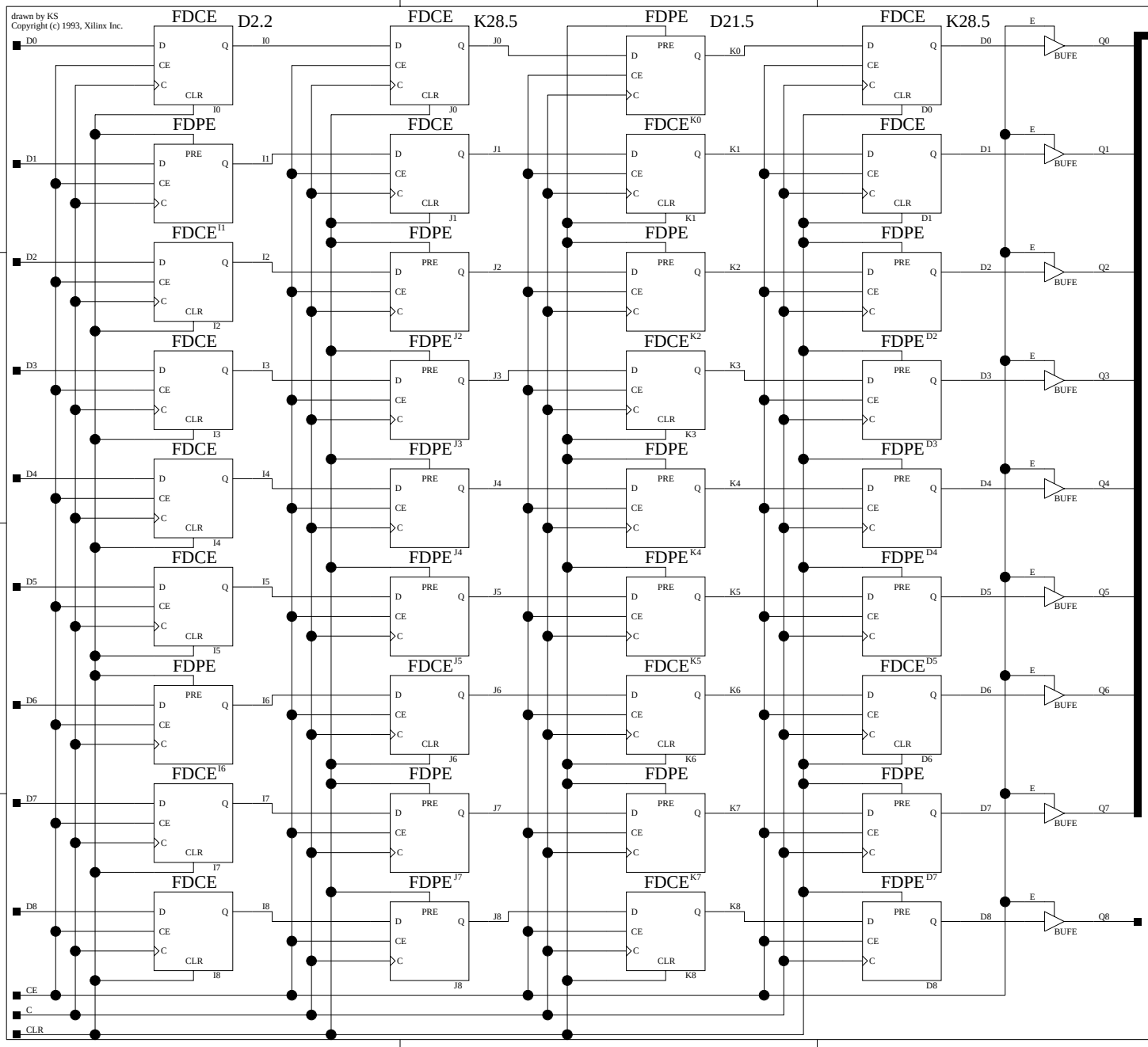
BY: JRG	PARENT PAGE: 21A	PROJECT: D785C	
DATE: 5-25-2005_15:01		FILE: STATECTL . 4	PAGE: 24C



Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050

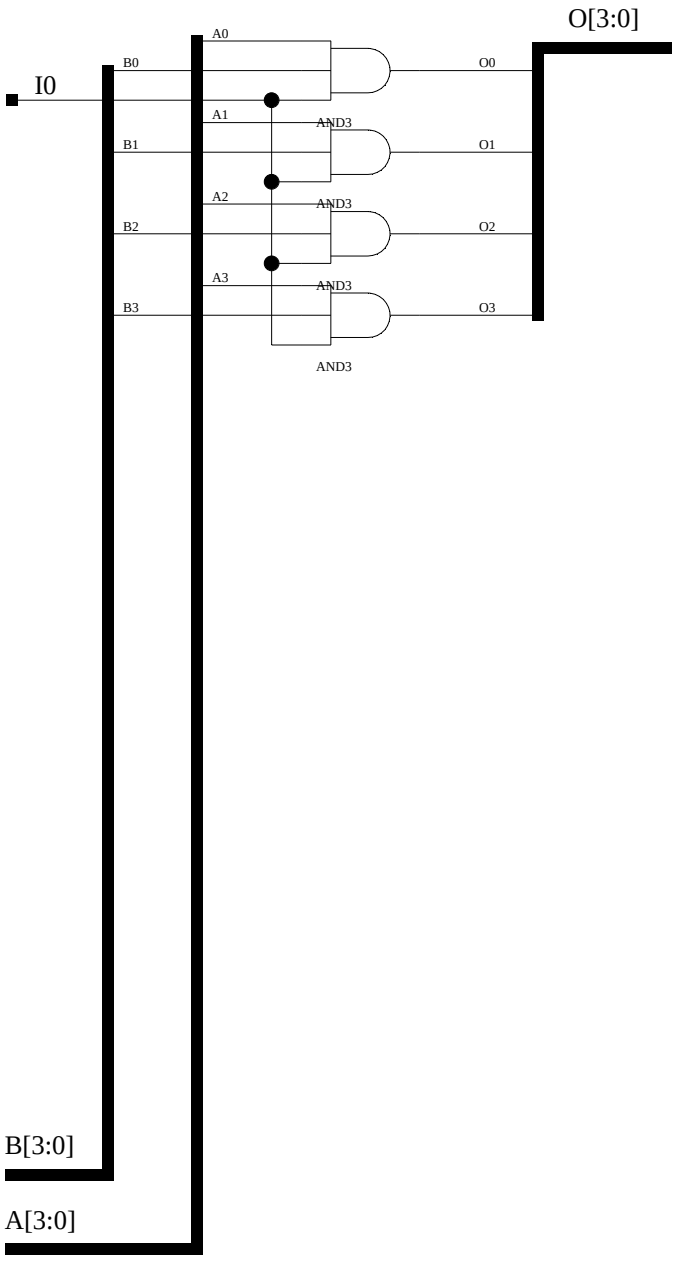
Title:	VIRTEX Family Ethernet Idle Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



Send 4 Sync bytes:

K28.5(10111100)+D21.5(010110101)
+K28.5(10111100)+D2.2(001000010)
= 0x1BC + 0x0B5 + 0x1BC + 0x042

Title:	VIRTEX Family Ethernet Sync Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Sync cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



XILINX

Title: VIRTEX Family 4-AND3COM1 Macro

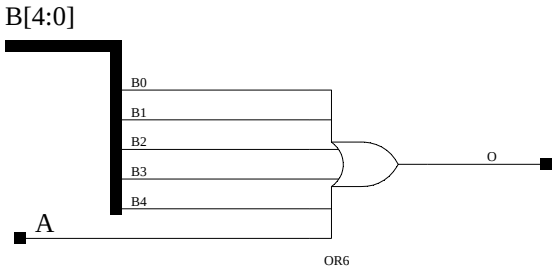
Comments: 4-AND3 Bus Gate plus 1 common bit

JRG

Date: 1st October 2003 Ver: 1

Sheet Size: A Rev: A

drawn by KS

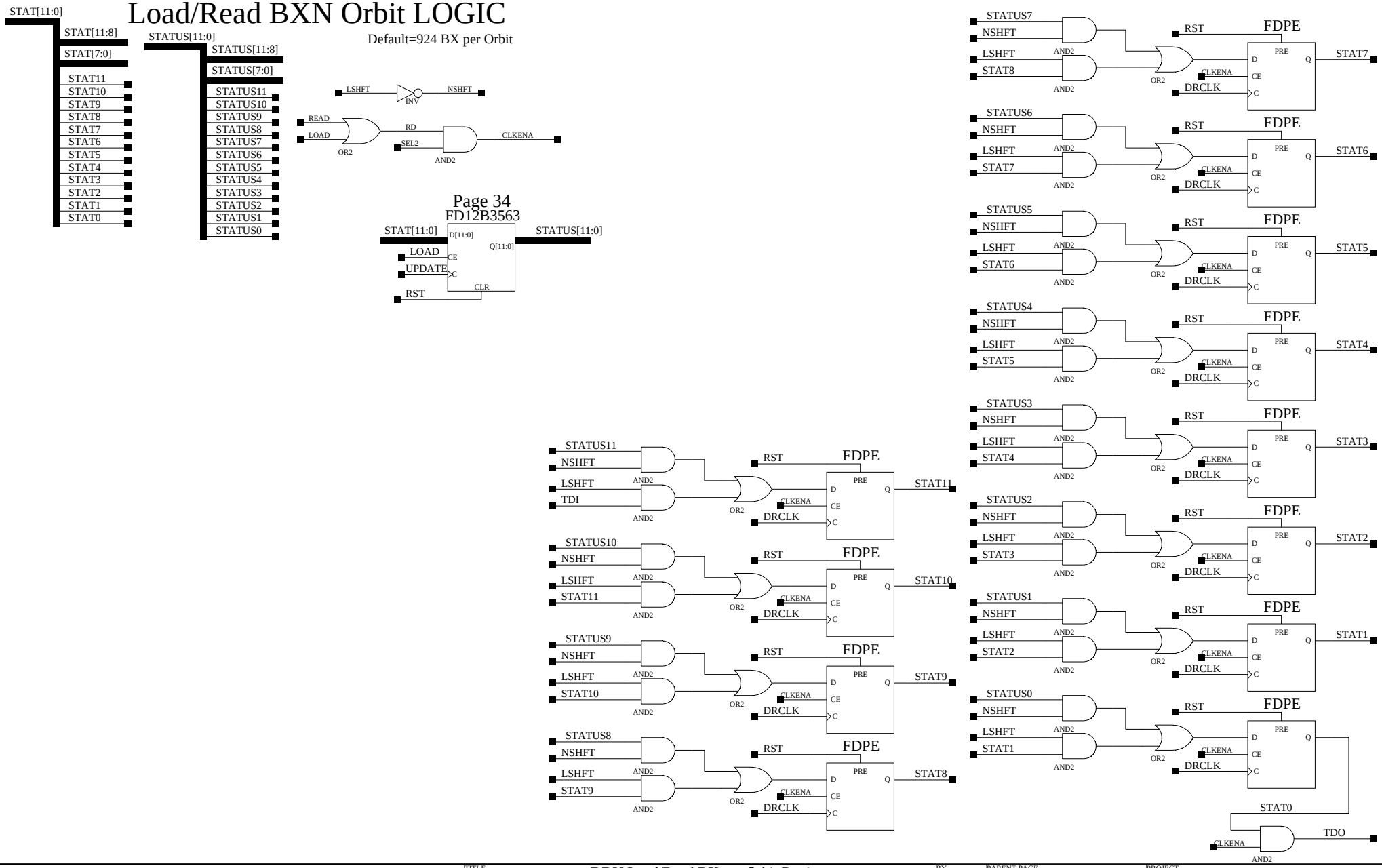


Title:	VIRTEX Family OR5+1 Macro
Comments:	OR5 Bus Gate w/Common
	JRG
Date:	27th December 2001
Ver:	1
Sheet Size: A	
Rev:	A

drawn by KS

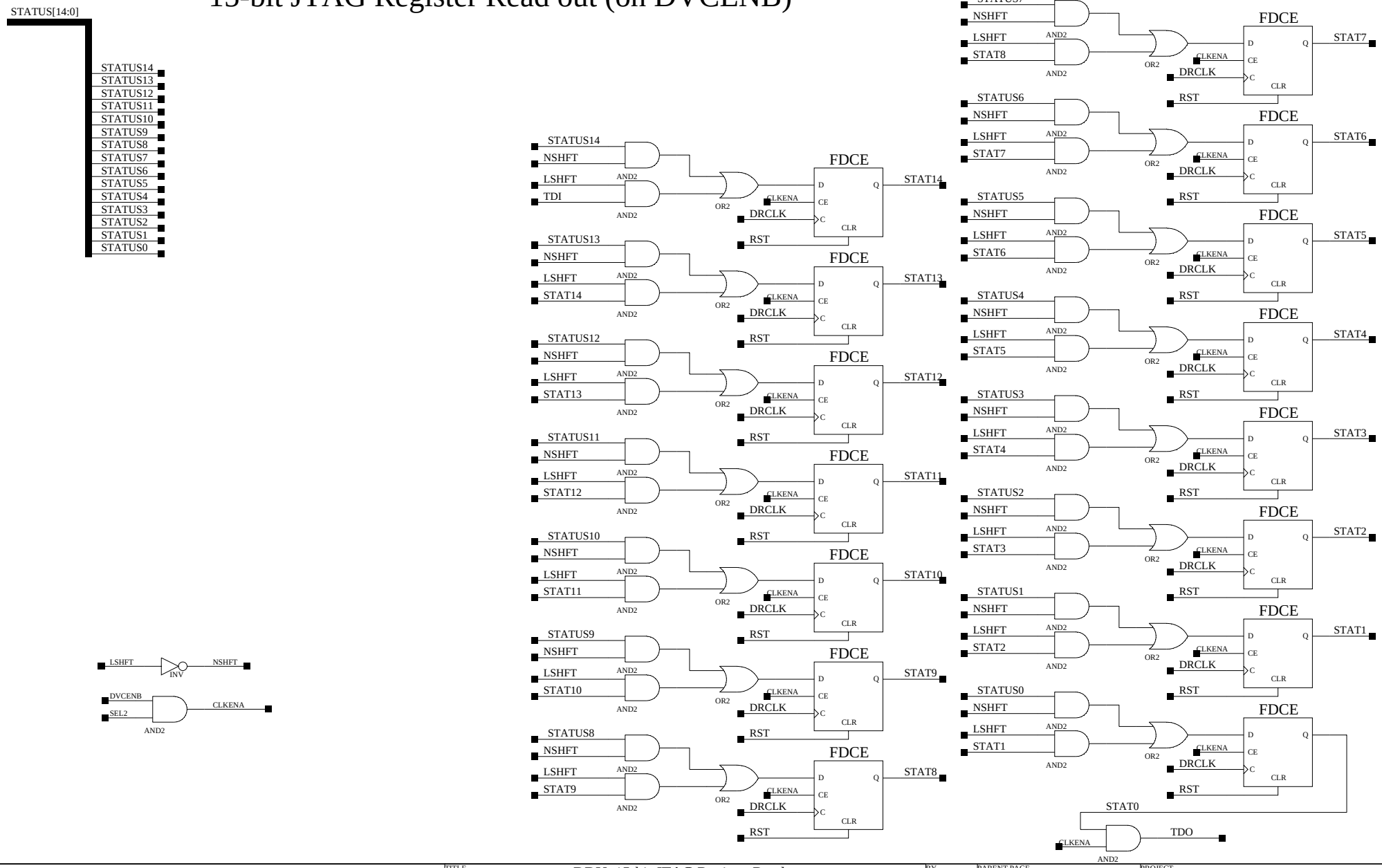
Load/Read BXN Orbit LOGIC

Default=924 BX per Orbit



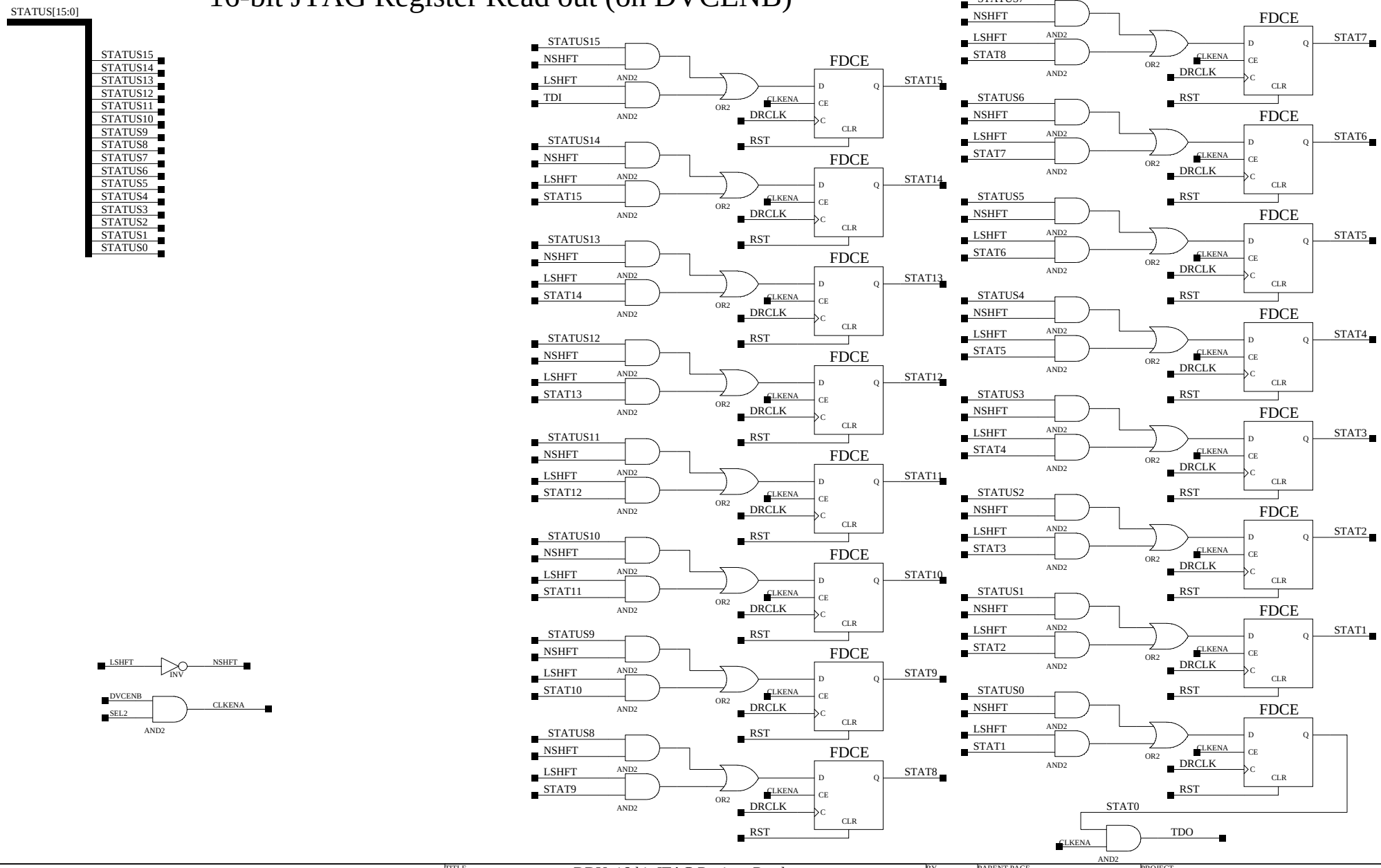
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Read BX per Orbit Register DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3F	PROJECT: D785C
		DATE: 9-19-2005_9:55	FILE: BXN_REG . 1	PAGE: 29

15-bit JTAG Register Read out (on DVCENB)



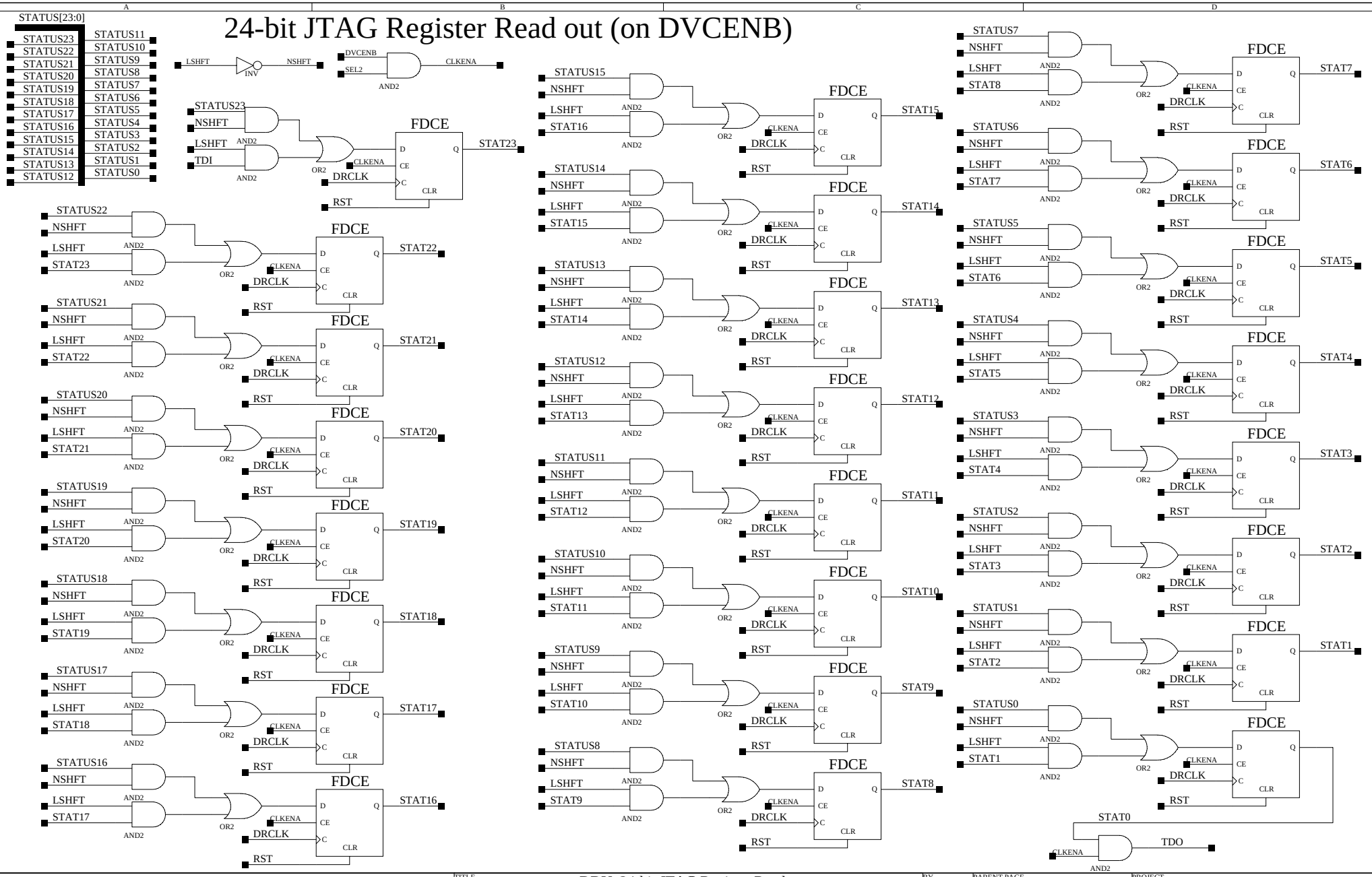
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 15-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_15_1	PAGE: 31

16-bit JTAG Register Read out (on DVCENB)



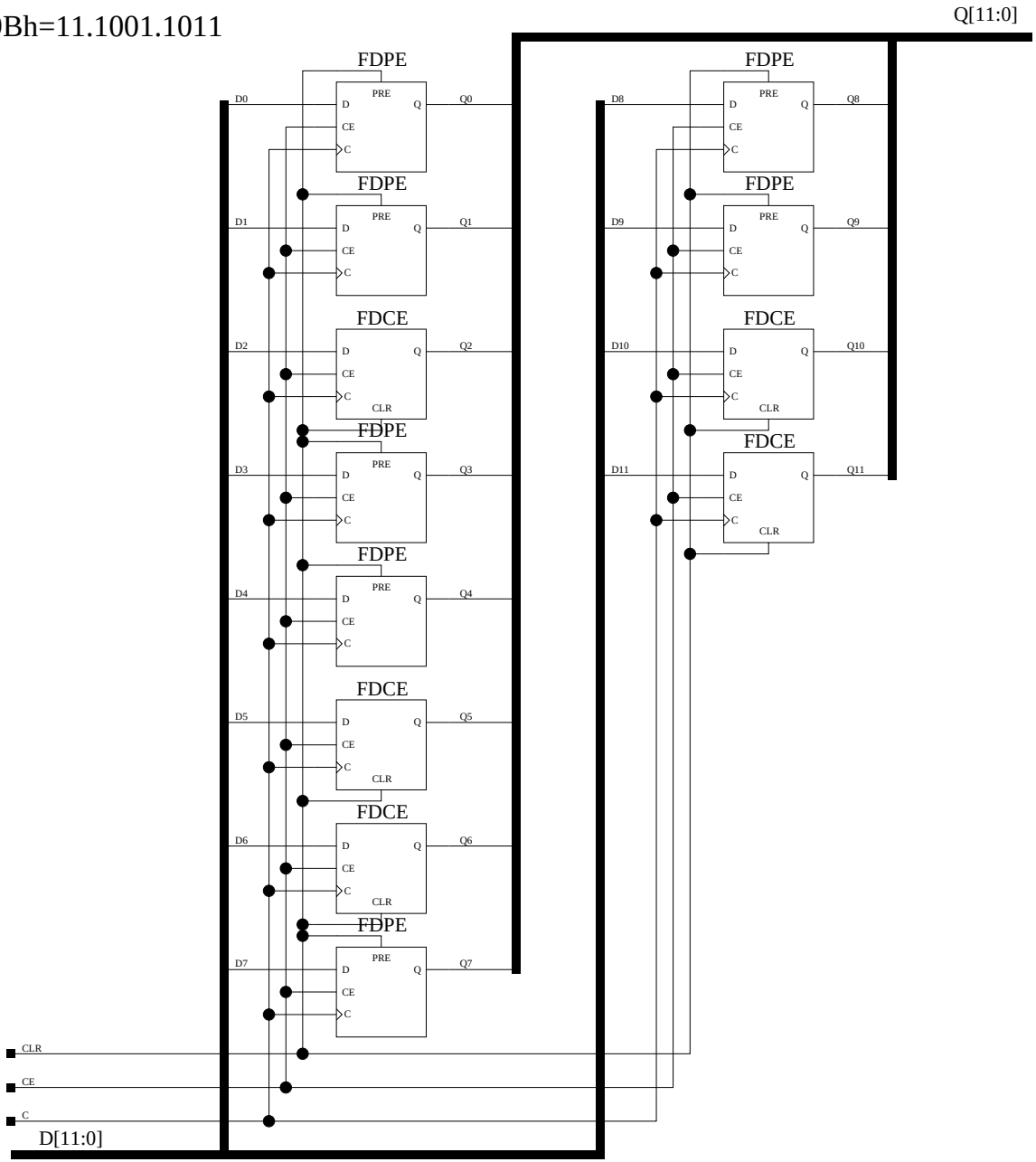
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 16-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_16 . 1	PAGE: 32

24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:17	FILE: CHECK_24_1	PAGE: 33

def=923=39Bh=11.1001.1011



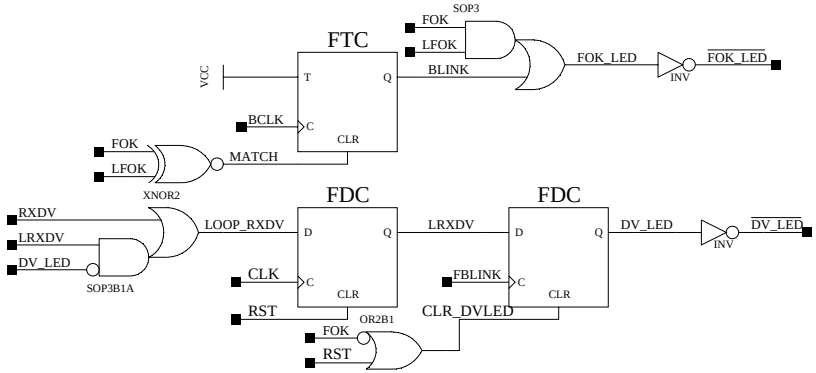
Title:	VIRTEX Family FD12b923 Macro		
Comments:	12-Bit D Flip-Flop with Preset to 923d and Enable	JRG	
Date:	8th May 2003	Ver:	1
Sheet Size: B		Rev:	A

FOK LED

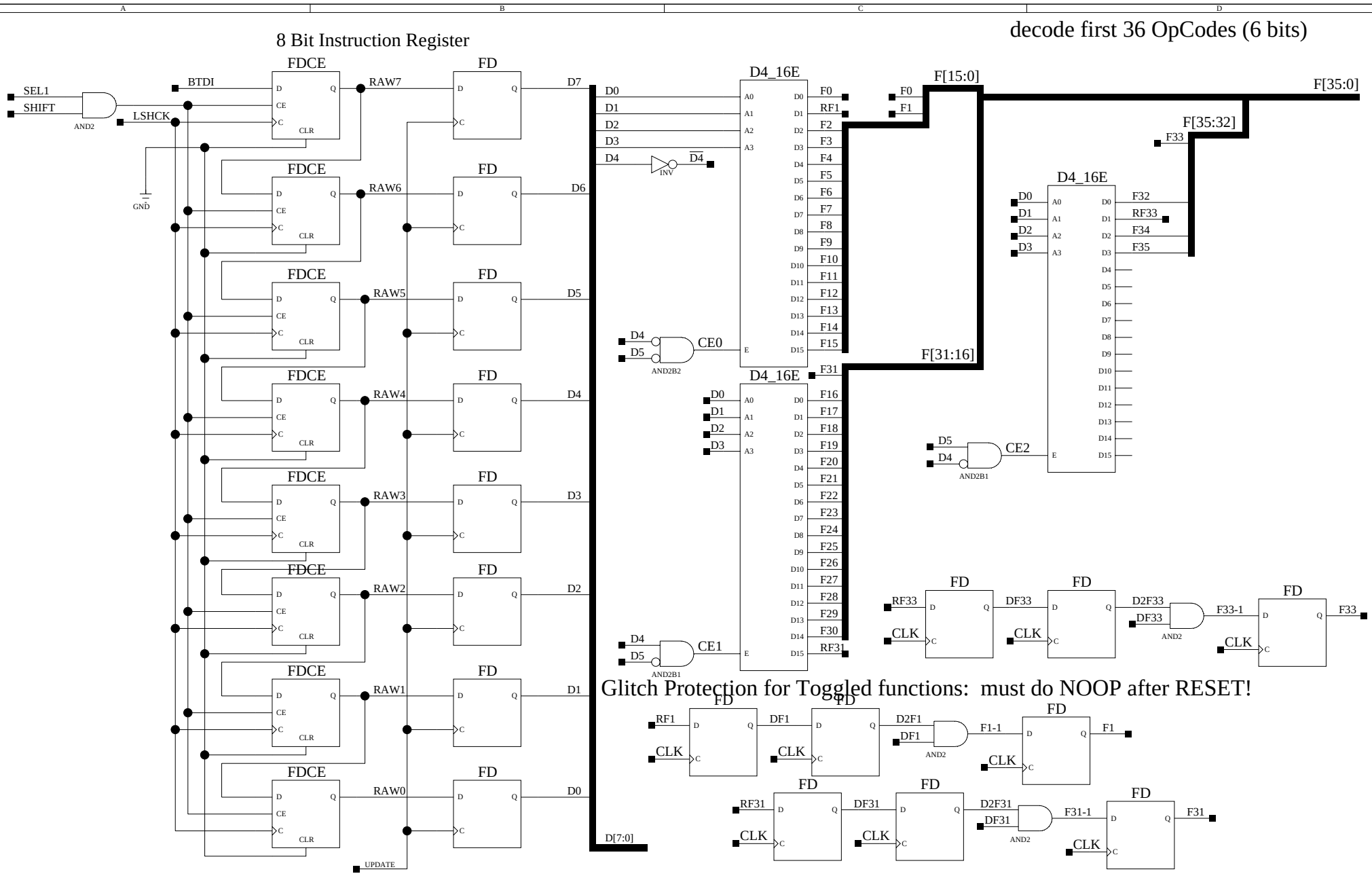
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED

--LIT == Active Data Xmit
--OFF == No data to Xmit

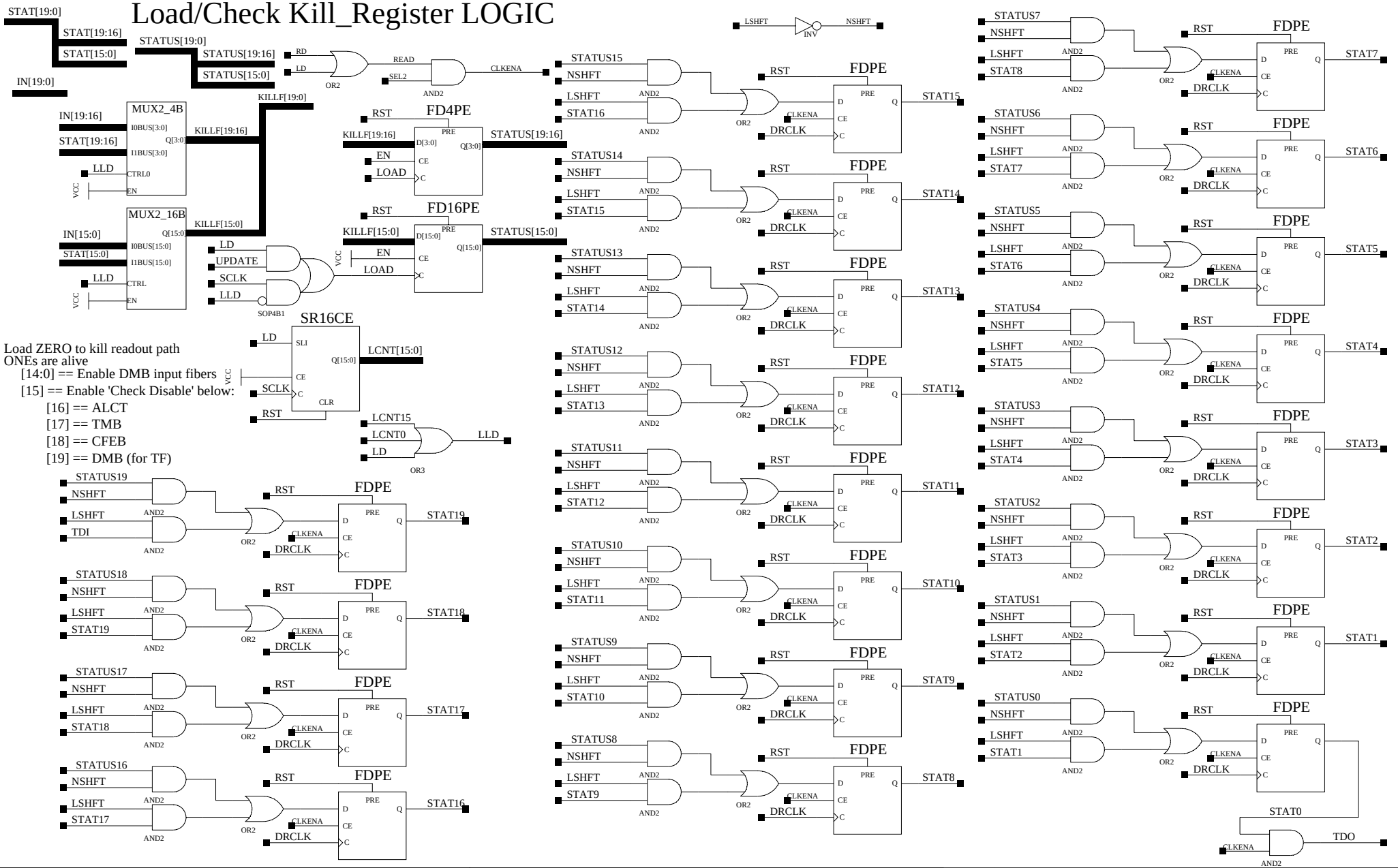


XILINX			JRG
Title:	FIBERLED		
Comments:	Custom LED Slow-Blink Control for Fiber Inputs		
Date:	27th January 2004	Ver:	1
Sheet Size: B		Rev:	A

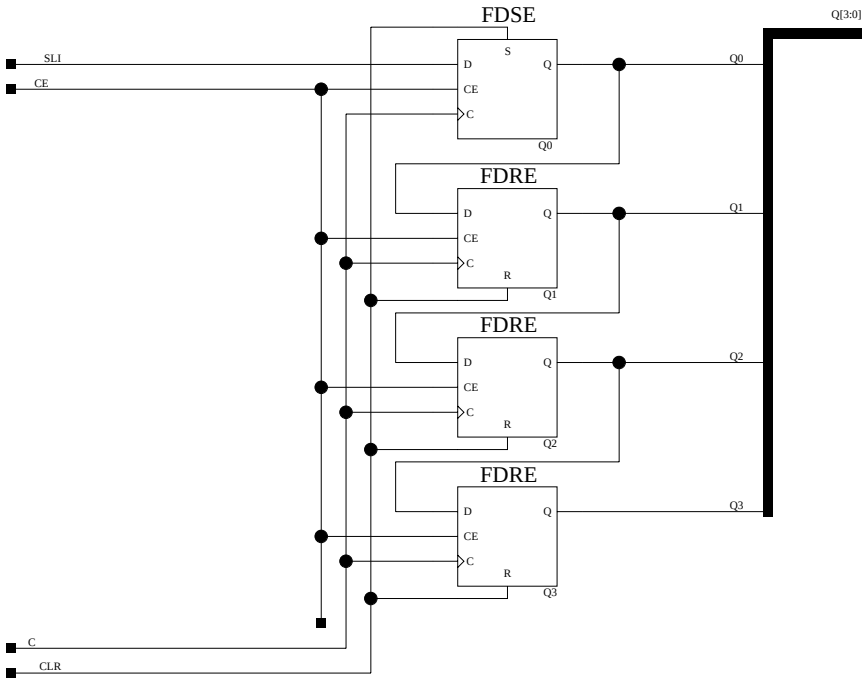


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE JTAG Instruction Decode DDU Controller CMS CSC ELECTRONICS	BY JRG	PARENT PAGE 3D	PROJECT D785C
		DATE 1-26-2005_12:19	FILE INSTRGDC . 1	PAGE 36

Load/Check Kill_Register LOGIC



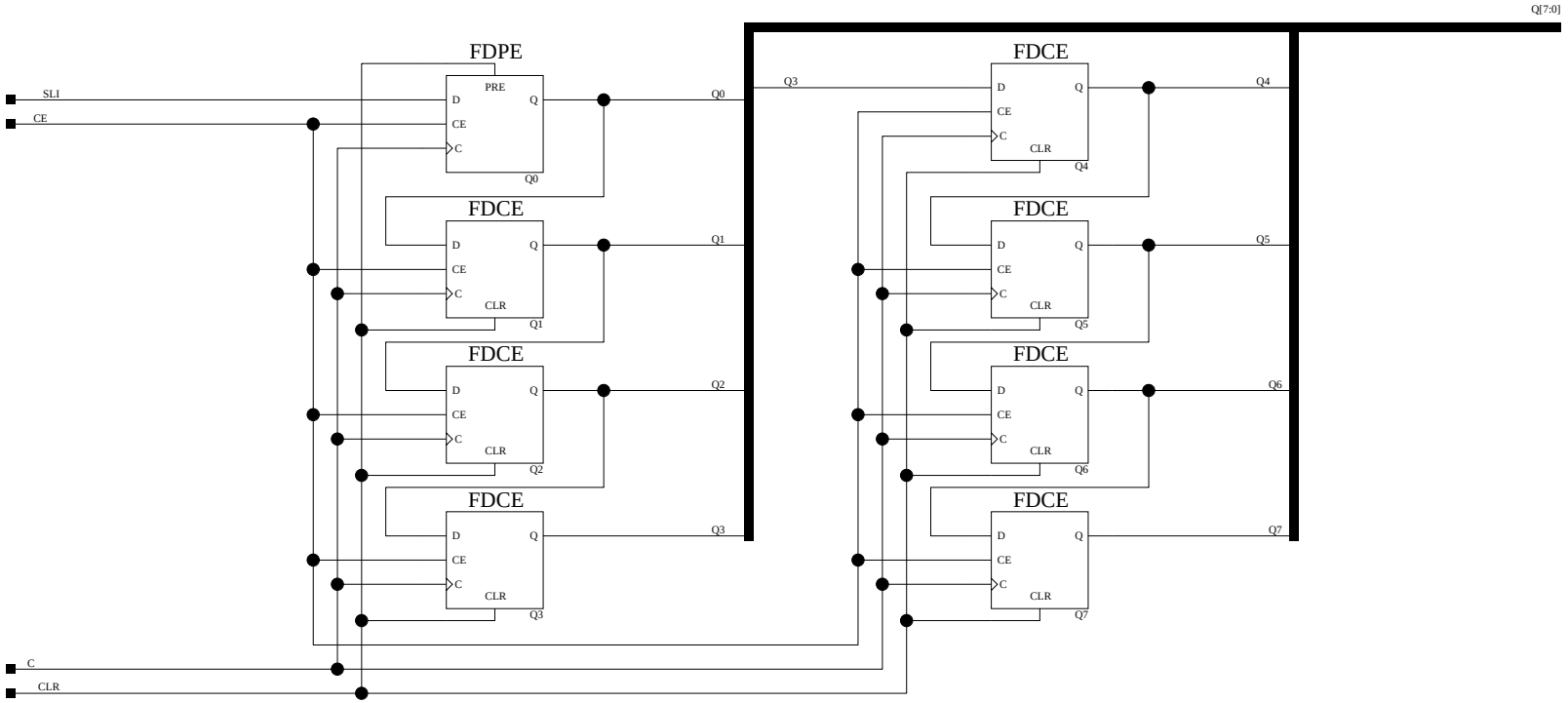
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Check Kill_Register Logic DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 5-22-2006_16:20	FILE: KILL_REG . 1	PAGE: 37



drawn by KS

XILINX

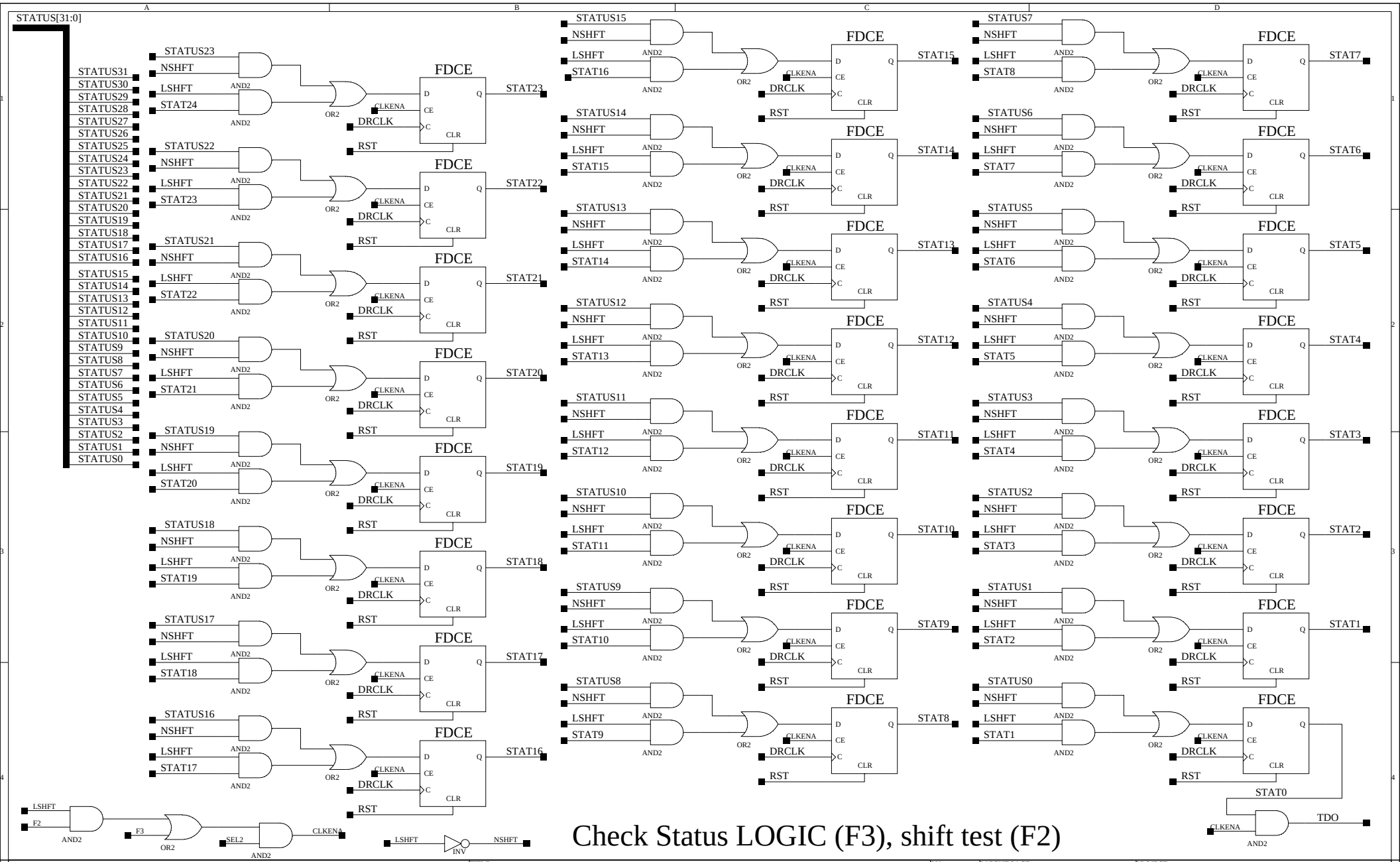
Title:	VIRTEX Family SR4CE Macro	JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single "one" on Sync Reset	
Date:	7th August 2001	Ver: 1
Sheet Size: B		Rev: A



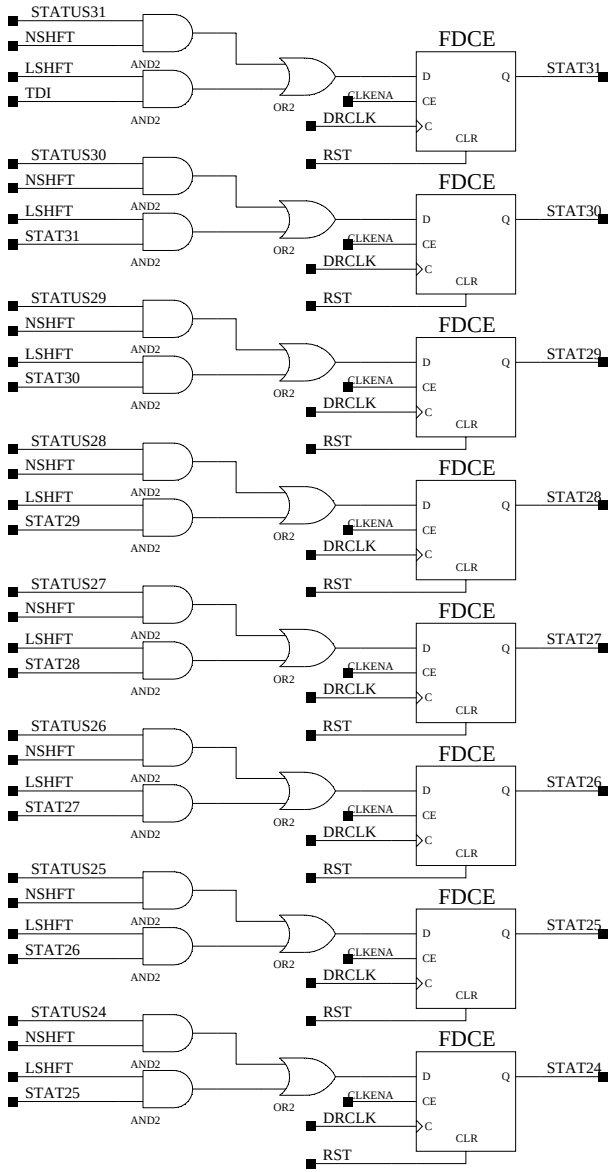
drawn by KS

XILINX

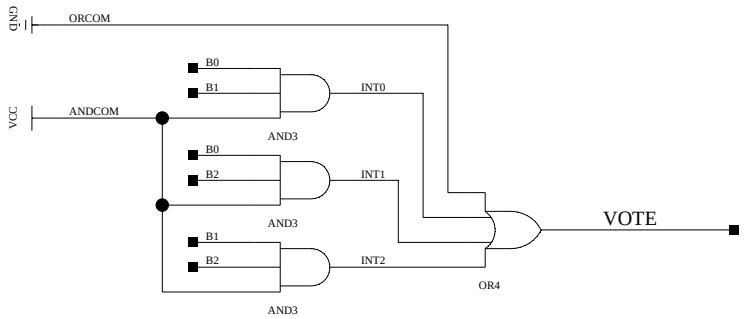
Title:	VIRTEX Family SR8CE Macro	JRG
Comments:	8-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single one on Async Clr	
Date: 7th August 2001		Ver: 1
Sheet Size: B		Rev: A



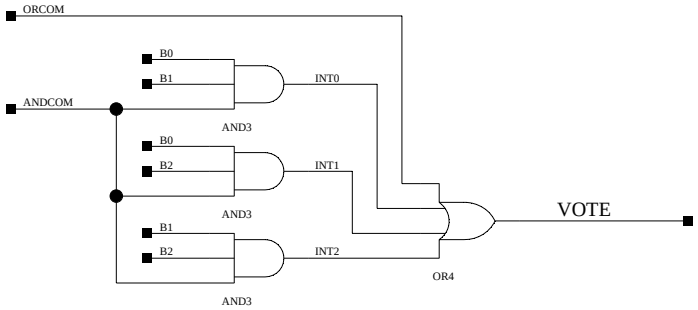
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:27	FILE: STAT_MON_1	PAGE: 40



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:27	FILE: STAT_MON_2	PAGE: 40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3 DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C	
		DATE: 1-26-2005_12:28		FILE: VOTE3 . 1	PAGE: 41



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:56	PARENT PAGE: ? FILE: VOTE3P . 1	PROJECT: D785C PAGE: 42