Set all Banks to 3.3 V I/O

**Depend Clocks:** elckB, slck

**Verilog Module Syntax notes:**

**Command line options:** -bufg 0 -iof false -iobuf

**PROGRAM takes < 55 ms (28ms this FPGA):**

**PART=XC2V500-5-FG456**

**VME Broadcast Addresses:**
- 24 = OSU-TCB "Test Control Board"
- 25 = DMB
- 26 = TMB
- 27 = Both DMB and TMB
- 28 = DDU
- 22 = DCC

**Reset-to-DDU Ready time:**
- Sync: < 600 ms
- Soft: < 20 ms
- Hard: < 62 ms

**DDUctrl-PROGRAM < 27.6 ms**
- DDUctrl-PROGRAM < 30.1 ms
- Nctrl-PROGRAM < 51.8 ms

**DDU Format Since DDUctrl v15:**

**v1:** Begin vme5ctrl from vme4ctrl v5, new DDU5 pinout
**v3-8:** All PROM JTAG lines now have 3-state drivers, fixed UCF FMM pins
**v9-10:** Add VME Serial ADC control (Device 8...13 in r2), debug on LEDmode14; tune DLLs
**v11-13:** Modify FMM LEDs, add 3 IRQ pins, add VME Registers for GbE/SLINK_WAIT, Fake_L1A_Enable & DDU production testing
**v14:** Add Restore-Idle after SoftReset, add Busy/Warn history on VMEparDev5/6, tune RealFMM logic
**v14r2-4:** Tune Busy/Warn history

**v15:** Tune ToVME and AS timing, also VMEpar_Info Reg; sets IRQ1 on Error; add debug LEDmode12

**v16:** Tune 12-bit SADC, add verilog-Cascade bit_counter for CSC Sync/Err flags for IRQs
**v17:** Remove SyncRst where not needed

**v18:** switch DDUfpga JTAG from SlwClk2 to SCLK, @INIT --> INIT for ROMs, tune BUSY/Sync priority
**r2:** add one SCLK delay to VME_PEN & VME_SEN, r3-8: test Broadcast
**v18r9:** ok, no Bcast.  v19r1-2: Bcast tests.  v19r3: Fixed Broadcast

**Mode 1 Switch Block, LED0 in rear:**
- 1: Mode Bit 0
- 2: Mode Bit 1 IRQ Response delay, Shuttle PC
- 3: Mode Bit 2 to end of first DTACK: 80-120 usec
- 4: Mode Bit 3 to end of second DTACK: 350-1150 usec
- 5: Mode Bit 4 00 for Standard Debug, 01 for VME-Serial
- 6: Mode Bit 5 10 for Flash RAM, 11 for VME-Parallel
- 7: Disable Auto Serial Load

**Set all LA bits HIGH ~FPGA version on LEDs**

**RST_1=Soft_Reset for FPGAs and ALL FIFOs**

**To Do:**
- Check DBR: throw Autoled
- Put GMR Pend into Flash BUS
- No logic for VMECtrl, VMEpar...

**Replace EmptyIN/FIFO_EMPTY PUs?**

**DDU WordCount (64-bit words) for "No Data" event: 0x006.**

**DDU WordCount for one DMB (only one CFEB): 0x19A = 410 dec.**

**DDU WC. 1 DMB with 2 CFEB: 0x32A = 810 dec.**

**DDU WC. 2 DMB with 1 CFEB (nCFEB=2): 0x32E = 814 dec.**

**DDU WC. 2 DMB with 2 CFEB (nCFEB=4): 0x64E = 1614 dec.**

**Ethernet ByteCount = 8*DDU WordCount (16 TS assumed)**

**Default Startup Order:**

- Release DLL (no wait)
- 4) DONE
- 5) En. Outputs
- 6) Release WE
SCLK: 10MHz = MIDCLK (max serial speed for FIFOs)
SLOWCLK: 2.5MHz (used for Serial ADC)
SLOWCLK2: 1.25MHz

CLK is in phase with MidClk, but they are not in phase with SlowClk

JTAG "Device" List
1: Output FIFO
dvc7
2: VME_Ctrl Prom
dvc1
3: DDU Ctl Prom 1 & 0
dvc6
4: InCtrl Prom 1 & 0
dvc4
5: DDU_Ctl FPGA
dvc8
6: InCtrl FPGA 0
dvc2
7: InCtrl FPGA 1
dvc3
8: SLINK JTAG
dvc5
9: VME Parallel (...not JTAG...)
N/A
10: VME Serial (...not JTAG...)
N/A
13: Serial ADC (...not JTAG...)
N/A
15: Emergency Load for VME_Ctrl Prom
N/A
The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz. The ISP does not work at 2.5MHz or faster.

Free LED Modes
LA0 free: 13   LA1 free: 12,13
LEDs Free: 13
TP 2-4 Used: 0,1
8-bit Opcode: Read Flash SRAM Status

Send Opcode MSb first, Read Data LSb first
VME, No Serial Dev

Check for These bits[7:0] in SRAM Status: Rdy, Comp, 0, 0, 1, 1, x, x

32-bit Opcodes: Program Flash SRAM Pages 1,4,5,7

Send Opcode MSb first, Read Data LSb first
VME, No Serial Dev

Check for These bits[7:0] in SRAM Status: Rdy, Comp, 0, 0, 1, 1, x, x

64-bit Opcodes: Readout Flash SRAM Pages 1,4,5,7

Send Opcode MSb first, Read Data LSb first
Auto, After MRST

Check for These bits[7:0] in SRAM Status: Rdy, Comp, 0, 0, 1, 1, x, x

Note 4-bit VME command (VMEadr[5:2])
Serial ADC (12-bit, MAX1270/1271) Interface clock: 1.25MHz (Divided SLOWCLOCK) is used. The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz.

REAL FMM 4-bit decode definitions:

- 0001: Warning/NearFULL (Grn ON, Yel BLINK)
- 0010: Lost Sync, need SyncReset (both BLINK)
- 0100: Ready {DDU Ready === !Busy} (Grn ON)
- 1100: Error, need HardReset (Yel BLINK)

Serial ADCs & FMM LED Logic
DDU VME Controller Logic
CMS CSC Electronics
Parallel Register Readout

Count how many CSC Reset bits are set:


Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write

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VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics

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VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics
Required for Test firmware:

CMD15 = "FMM Test Reg" FD16CE

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must set "FOE" FMM Override Enable

Dev9, CMD 0F/8Fh (R/W)
bits15-4: "FOEh"
bits3-0: FMM Bit state to Force

Special VME Parallel Dev 9 CMD 0,5,6

Dev9, CMD 00/80h (R/W)
bits2-0: GbE Prescale
bit3: Slink Wait Enable

Required for Test firmware:

Read Only, VME Par Dev 8:
writes with InReg0

Could be temporary

Dev9, CMD 05/85h (R/W)
bits2-0: Enable Fake L1A/Data Passthrough for each DDU FPGA
bit3: Not Used

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VME Communication Interface
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VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics
DDU VME Controller Logic JRG

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TITLE: VME Communication Interface
DDU VME Controller Logic
CMS CSC Electronics

DATE: 12-23-2005 10:50
PAGE: 2N

VME_DEV[15:0] = LA0[15:0]
VME_VMEACC[15:0] = BUFE16

DDU_SYNC[15:0] = LA0[15:0]
VME_DLL_ERR = BUFE4

DDU_BUSY[15:0] = LA0[15:0]
VME_VMEACC[15:0] = BUFE16

DDU_WARN[15:0] = LA0[15:0]
VME_VMEACC[15:0] = BUFE16

DDU.ERR[15:0] = BUFE16

INV = BUFE4

LED0 = BUFE16

LED2 = BUFE16

LED4 = BUFE16

LED6 = BUFE16

LED_OPT = BUFE16

LED7 = BUFE16

LED0 = BUFE4

LED2 = BUFE4

LED4 = BUFE4

LED6 = BUFE4

LED7 = BUFE4

INV = BUFE4

INV = BUFE4

INV = BUFE4

INV = BUFE4

INV = BUFE4

INV = BUFE4

Device: ADR[15:12] sets device ID


COMMAND[9:0]  ADR[7:2]=JTAG command

00  Read only Status Register[8-bit data]
01  Read Input Register0[16-bit data]
02  Read Input Register0-2[16-bit data]
03  Read Input Register0-2[16-bit data]
04  Read Input Register0-2[16-bit data]
05  Read Input Register0-2[16-bit data]
06  Read Input Register0-2[16-bit data]
07  Read Input Register0-2[16-bit data]

08  Input FIFOs 0-3

09  Serial ADC

VME-Serial Device code: "iadr" in scan.c

04  Flash SRAM (RdsStat or Program Page), NEEDS COMMAND

--> command required with device 4:

0x 00: Read Status Register[8-bit data]
0x 09: Program page 1 (Kill Ch.) [16-bit data]
0x xx: Program page 4 (DDR offsets) [32-bit data]
0x xx: Program page 5 (GBE offsets) [32-bit data]
0x 0D: Program page 7 (Board ID) [16-bit data]

0C  Load GBE Output FIFO (SEN=LD, set HI during MRST)

0D  Load DDU_Ctl FPGA (Kill Ch.)--N/A

0E  Load DDU_Ctl FPGA (Board ID)--N/A

0F  Load DDU_Ctl FPGA (Kill Ch.)--N/A

09  Emergency PROM Programming via VME

0A  User Code 11111110 1111001001

0B  User2 03C2h=1111000010

0C  User1 03C3h=1111000011

0D  Device Bypass

0E  User Code 11111111 1111100000

0F  User Code 11111110 1111001001

For bigger V2P's add 1's to the left

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VME-Read Command Decoder
DDU VME Controller Logic
CMS CSC Electronics
^added 3 clocks for Broadcast case^^^
^^^added 3 clocks for Broadcast^^^
CFEB JTAG commands:
00 || Shift data, no header, no tailer
01 || Shift data with header only
02 || Shift data with tailer only
03 || Shift data with header and tailer
04 ||
05 || Read TDO register
06 || Reset JTAG State machine
07 || Shift Instruction register with header and tailer
0C || Shift IR, no header, no tailer
0D || Shift IR with header only
0E || Shift IR with tailer only
0F || Shift Instruction register with header and tailer
DTACK for Load Instruction/Data Register command

was ~ADCENA1
Serial ADC Command Decoder:
00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
04 ||
05 ||
06 ||

CFEB JTAG command decode

Serial ADC Command Decoder:
- 00 || Write Control Byte to MAX1271's
- 01 || Read Data Back from 1271 Register
- 02 ||
- 04 ||
- 05 ||
- 06 ||