

this DDU:
add _BX Offset_ to Flash SRAM

VME5CTRL (file 0ddu_vme5ctrl) 4-20-2007_16:40
Version 19

CMS CSC DDU5, VME FPGA v1: Begin vme5ctrl from vme4ctrl v5, new DDU5 pinout
v3-8: All PROM JTAG lines now have 3-state drivers, fixed UCF FMM pins
v9-10: Add VME Serial ADC control (Device 8...13 in r2), debug on LEDmode14; tune DLL
v11-13: Modify FMM LEDs, add 3 IRQ pins, add VME Registers for GbE/SLINK_WAIT, Fake_L1A_Enable & DDU production testing
v14: Add Restore-Idle after SoftReset, add Busy/Warn history on VMEparDev6/5, tune RealFMM logic
v14r2-4: Tune Busy/Warn history
v15: Tune ToVME and AS timing, also VMEpar_Info Reg; sets IRQ1 on Error; add debug LEDmode12
v16: Tune 12-bit SADC, add verilog-Cascade bit_counter for CSC Sync/Err flags for IRQ
v17: Remove SyncRst where not needed
v18: switch DDUfpga JTAG from SlwClk2 to SCLK, @INIT-->INIT for ROMs, tune BUSY/Sync priority
r2: add one SCLK delay to VME_PEN & VME_SEN, r3-8: test Broadcast
v18r9: ok, no Bcast. v19r1-2: Bcast tests. v19r3: Fixed Broadcast

Set all Banks to 3.3V I/O

Indep Clocks: clk80, selk
Dependent Clocks: ck40=clk

Verilog Module Synth notes:

command line options: -bufg 0 -iob false -iobuf no VMECNTRL

PROGRAM takes < 55 ms (28ms this FPGA)

PART=XC2V500-5-FG456

PROM=XC18V04-VQ44 (PARALLEL)

ddu5_vme\VME5Ctrl\vme5ctrl

VME Broadcast Addresses:

- 24=OSU-TCB "Test Control Board"
- 25=DMB
- 26=TMB
- 27=Both DMB and TMB
- 28=DDU
- 22=DCC

Reset-to-DDU Ready time

- Sync: < 500ns
- Soft: < 20us
- Hard: < 62ms

VMEctrl-PROGRAM < 27.6ms
 DDUctrl-PROGRAM < 30.4ms
 INctrl-PROGRAM < 54.8ms

DDU Format Since DDUctrl v15:

H1: 0x/5T/NN.NNNN/XXX/1.H/VK
 H2: 0x/8000/0001/8000/HHHH
 H3: 0x/LLLL/0000/ZZZZ/GGMY

T-2: 0x/8000/FFFF/8000/8000
 T-1: 0x/SSSS.SSSS/QQQQ/PPPP
 TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
 DDU WordCount for one DMB (only one CFEB): 0x19A = 410 dec.
 DDU WC, 1 DMB with 2 CFEB: 0x32A = 810 dec.
 DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 0x32E = 814 dec.
 DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 0x64E = 1614 dec.
 DDU_WordCount = (6 + 25*Nts*nCFEB + 3*nDMB) <= 3005 (ignoring Trigger boards)
 Ethernet_ByteCount = 8*DDU_WordCount 16 TS assumed

Mode 1 Switch Block, LED0 in rear

1: Mode Bit 0
 2: Mode Bit 1
 3: Mode Bit 2
 4: Mode Bit 3
 5: Mode Bit 4
 6: Mode Bit 5
 7: Disable Auto Serial Load
 8: Set all LA bits HIGH, ~FPGA version on LEDs
 RST_1=Soft_Reset for FPGAs and ALL FIFOs

IRQ Response delay, Shuttle PC
 to end of first DTACK: 80-120 usec
 to end of second DTACK: 350-1150 usec

00 for Standard Debug, 01 for VME-Serial
 10 for Flash RAM, 11 for VME-Parallel

PromID: 05036093

ELECTRONICS LAB
 PHYSICS DEPARTMENT
 THE OHIO STATE UNIVERSITY
 174 WEST 18TH AVE
 COLUMBUS OHIO 43210

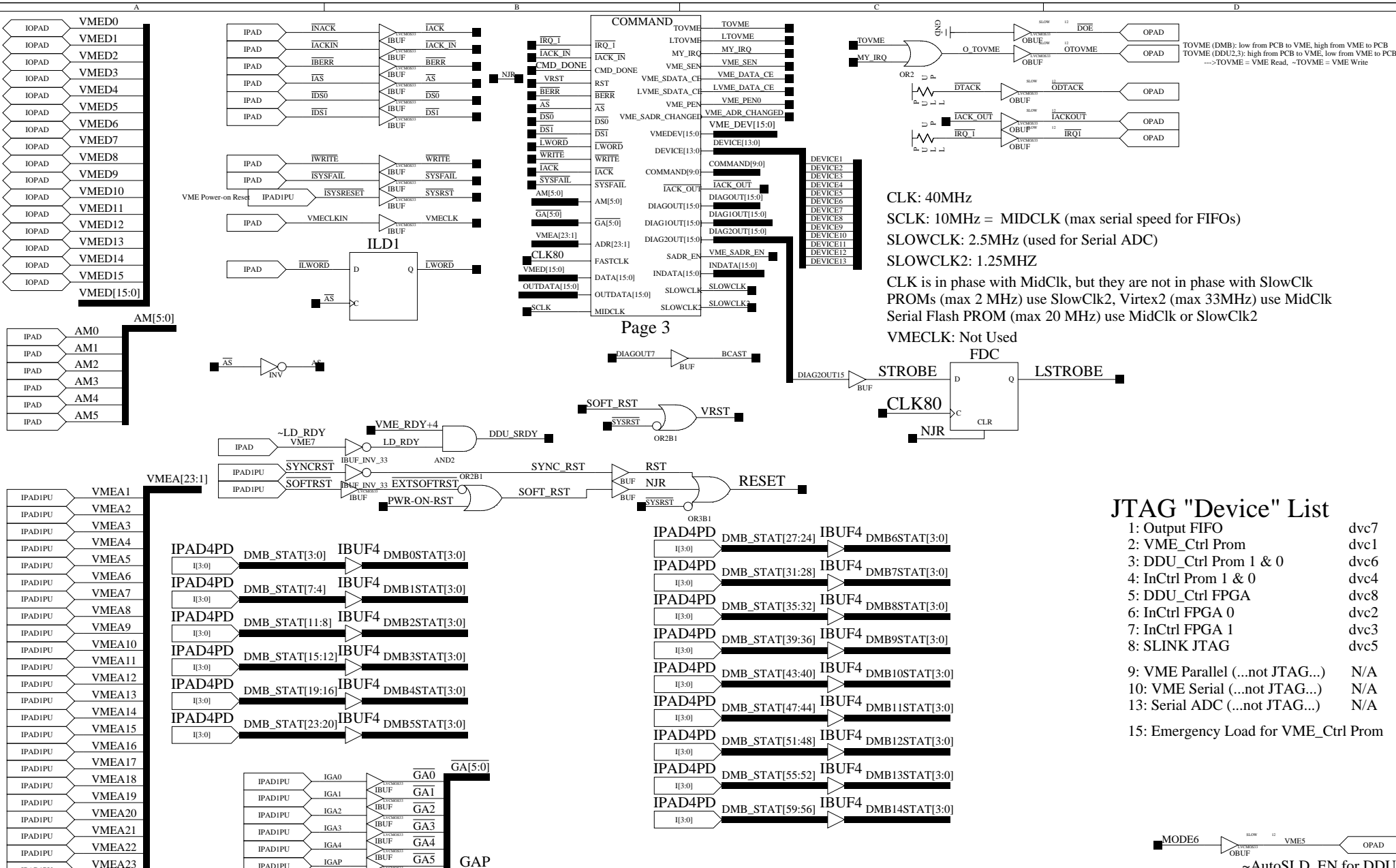
Replace EmptyIN/FIFO_EMPTY PUs?

To Do:

- Check GbE-thresh Autoload
- Put GbE Prescale into Flash RAM
- No logic for VMECLK, VMEA1...OK.

Default Startup Order:

- Release DLL (no wait)
- 4) DONE
- 5) En. Outputs
- 6) Release WE



Page 3

CLK: 40MHz
 SCLK: 10MHz = MIDCLK (max serial speed for FIFOs)
 SLOWCLK: 2.5MHz (used for Serial ADC)
 SLOWCLK2: 1.25MHZ
 CLK is in phase with MidClk, but they are not in phase with SlowClk
 PROMs (max 2 MHz) use SlowClk2, Virtex2 (max 33MHz) use MidClk
 Serial Flash PROM (max 20 MHz) use MidClk or SlowClk2
 VMECLK: Not Used

JTAG "Device" List

- 1: Output FIFO dvc7
- 2: VME_Ctrl Prom dvc1
- 3: DDU_Ctrl Prom 1 & 0 dvc6
- 4: InCtrl Prom 1 & 0 dvc4
- 5: DDU_Ctrl FPGA dvc8
- 6: InCtrl FPGA 0 dvc2
- 7: InCtrl FPGA 1 dvc3
- 8: SLINK JTAG dvc5
- 9: VME Parallel (...not JTAG...) N/A
- 10: VME Serial (...not JTAG...) N/A
- 13: Serial ADC (...not JTAG...) N/A
- 15: Emergency Load for VME_Ctrl Prom



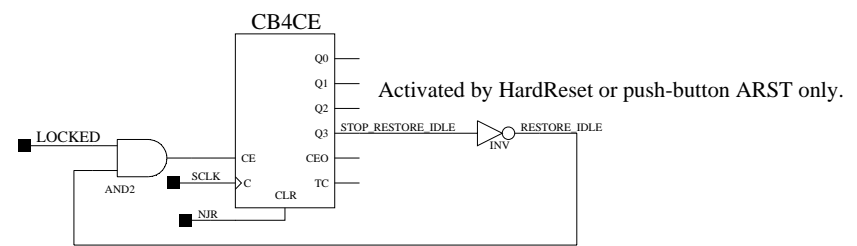
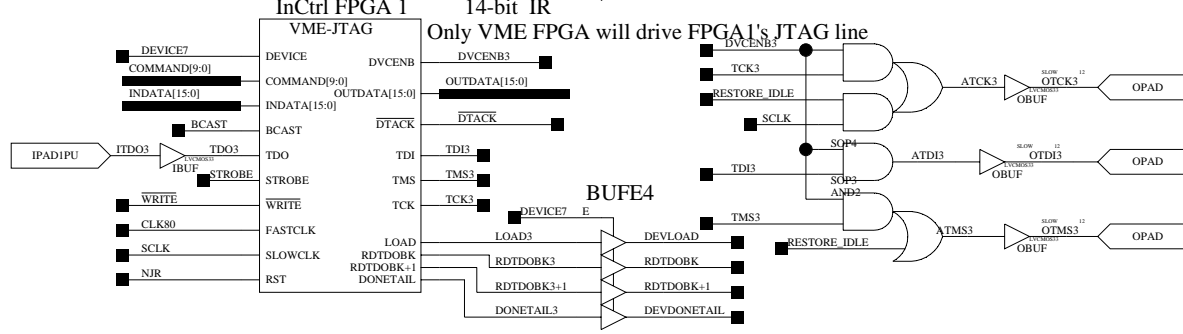
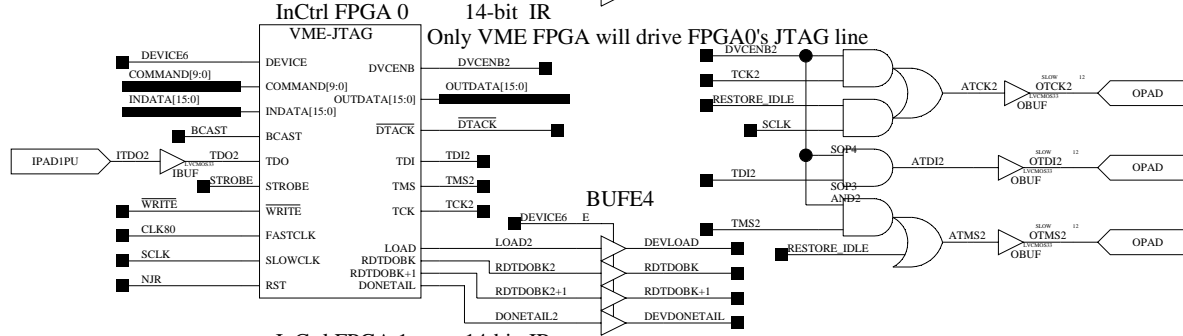
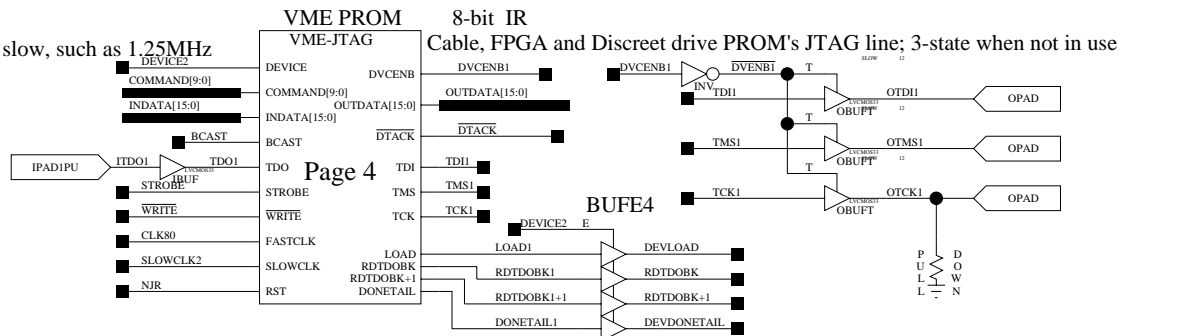
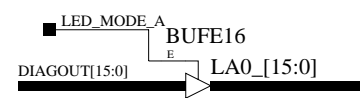
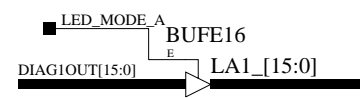
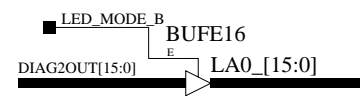
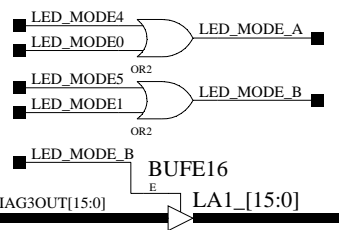
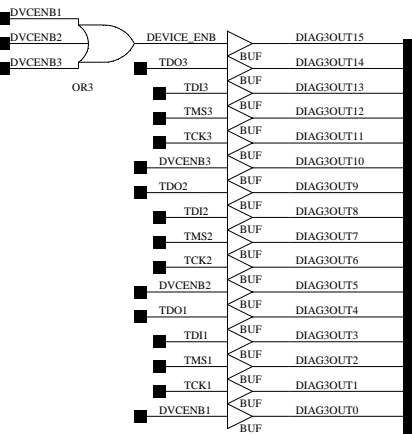
~AutoSLD_EN for DDU_Ctrl

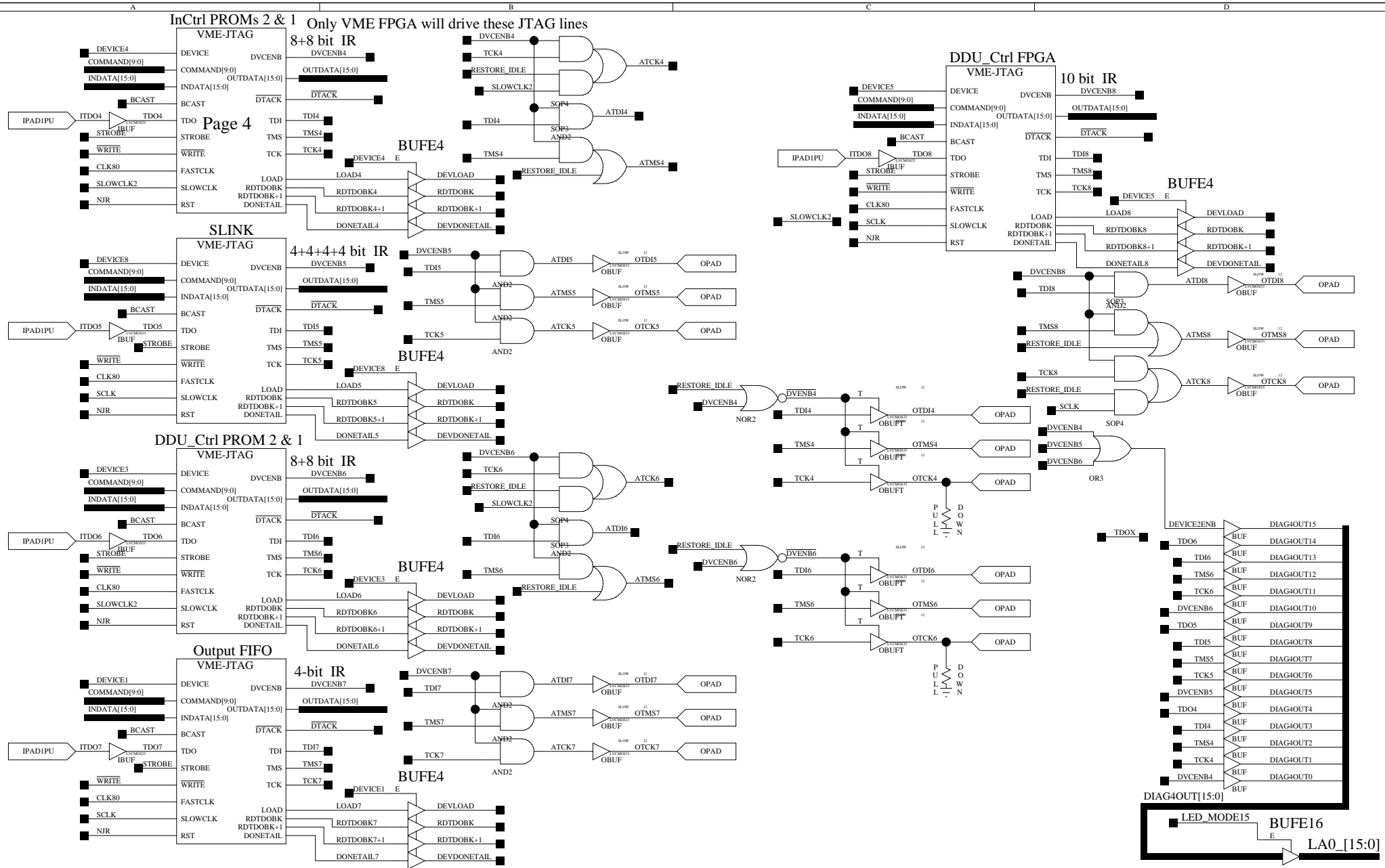
DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK

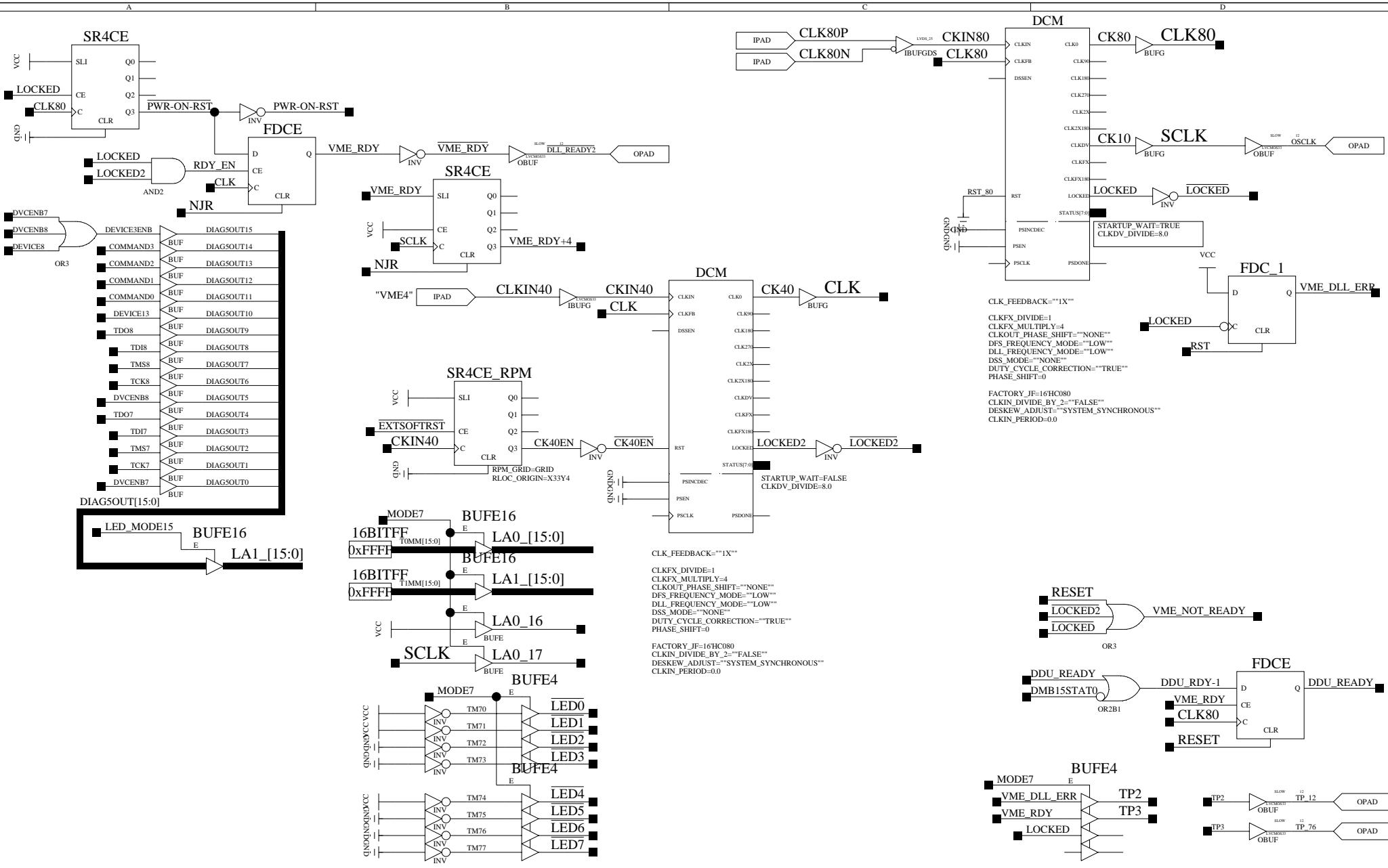
The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz
 The ISP does not work at 2.5MHz or faster

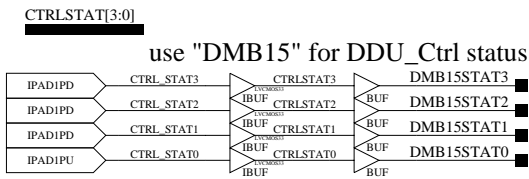
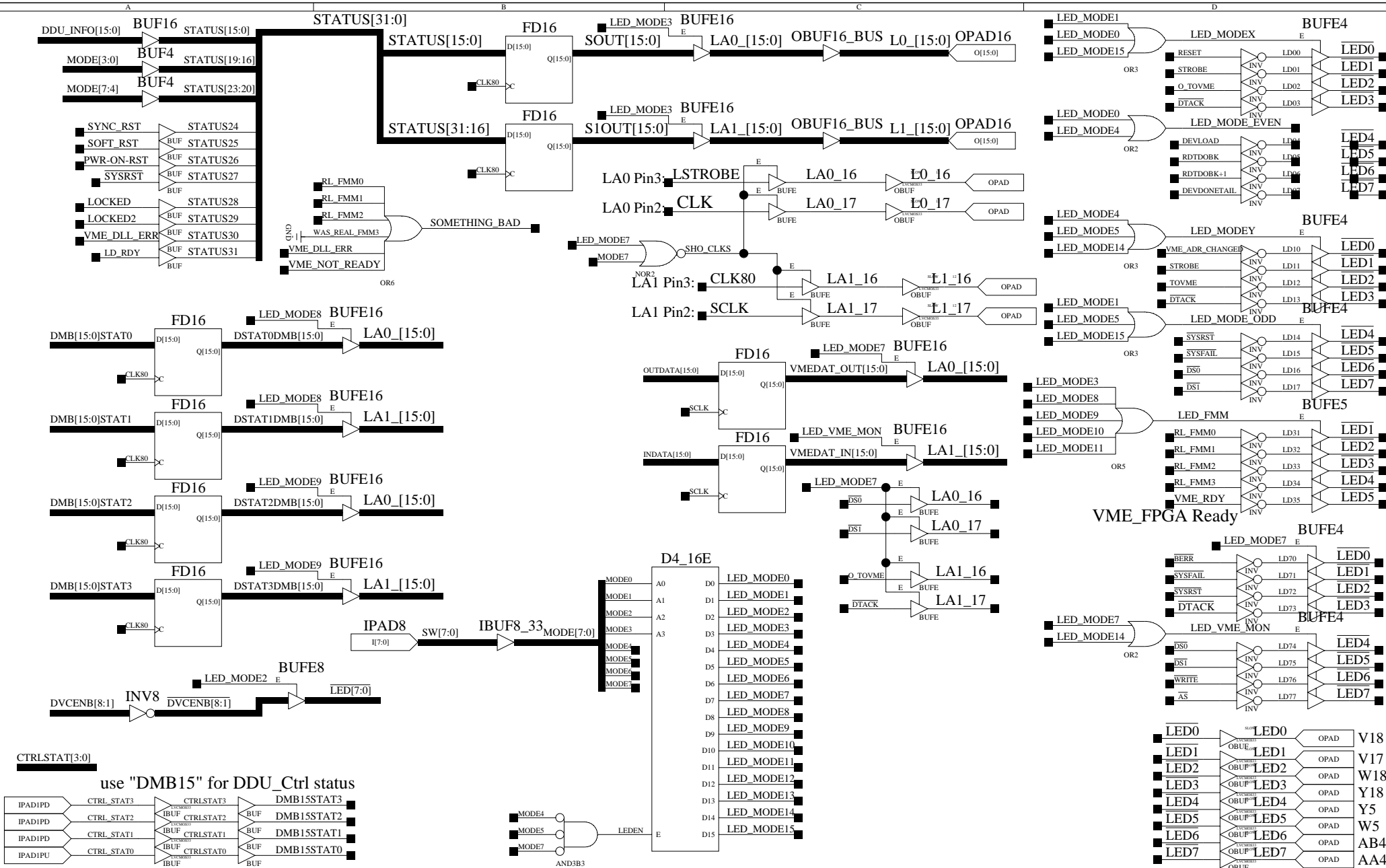
Free LED_Modes

LA0 free: 13 LA1 free: 12,13
 LEDs Free: 13
 TP 2-4 Used: 0,1

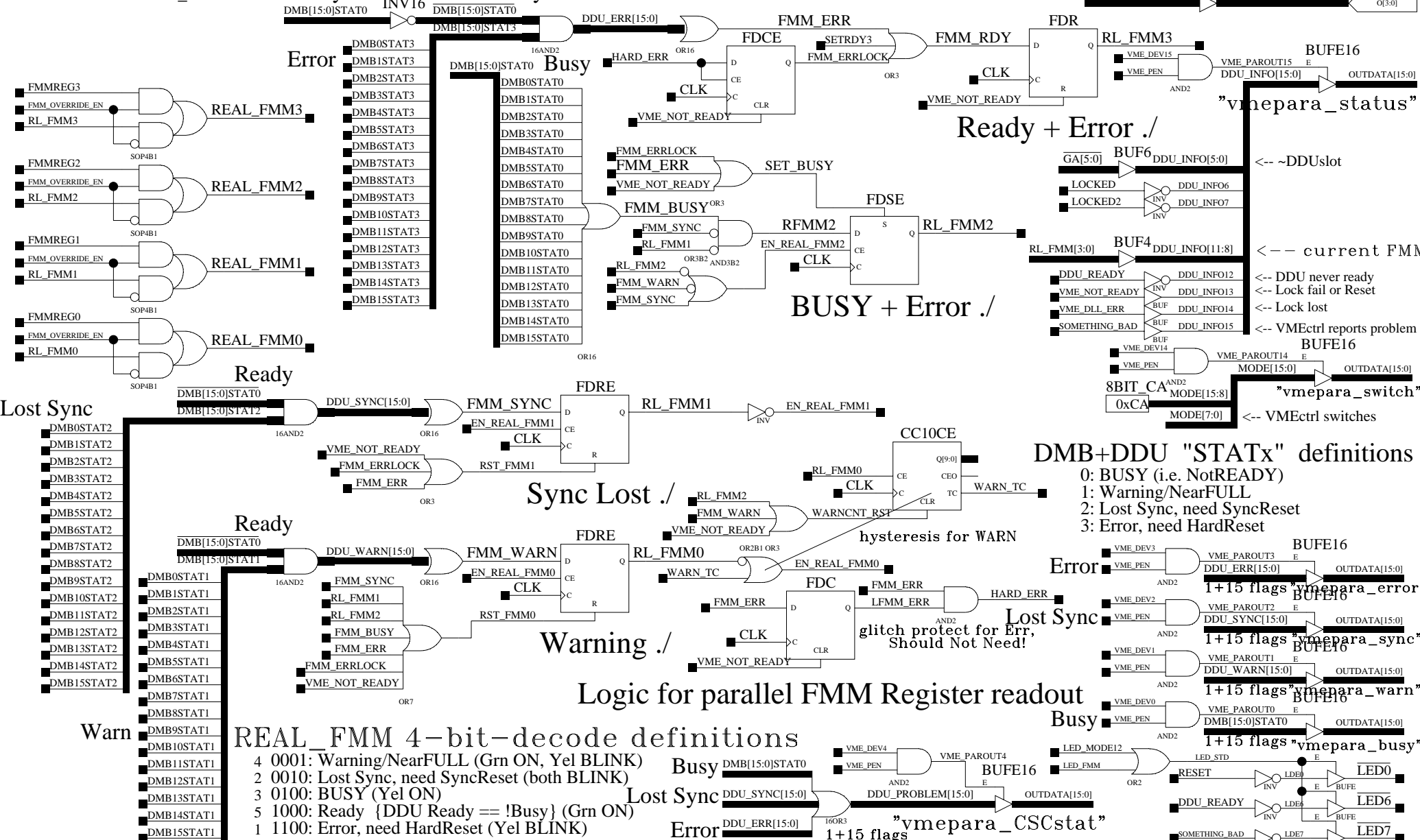








use "DMB15" for DDU_Ctrl status



Lost Sync

Warn

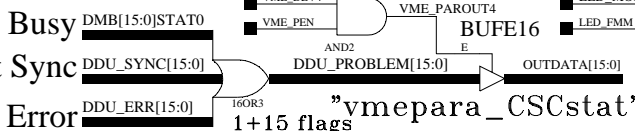
REAL_FMM 4-bit-decode definitions

- 4 0001: Warning/NearFULL (Grn ON, Yel BLINK)
- 2 0010: Lost Sync, need SyncReset (both BLINK)
- 3 0100: BUSY (Yel ON)
- 5 1000: Ready {DDU Ready == !Busy} (Grn ON)
- 1 1100: Error, need HardReset (Yel BLINK)

DMB+DDU "STATx" definitions

- 0: BUSY (i.e. NotREADY)
- 1: Warning/NearFULL
- 2: Lost Sync, need SyncReset
- 3: Error, need HardReset

Logic for parallel FMM Register readout



Serial Device List

(12 device functions, SEN = Serial Load)

9 VME Reads, 4 VME Writes, 7 Auto commands

- 0x 00: Read InFIFO 0
- 01: Read InFIFO 1
- 02: Read InFIFO 2
- 03: Read InFIFO 3
- 04: R/W Flash SRAM
- 0x 08: W Load DDR InFIFO 0
- 09: W Load DDR InFIFO 1
- 0A: W Load DDR InFIFO 2
- 0B: W Load DDR InFIFO 3
- VME_SDEV>=8 or ==4 are Writeable; others are Read Only.
- 0C: W Load GBE Output FIFO (SEN=LD, set HI during MRST) --test?
- 0D: W Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.) --test?
- 0E: W Load DDU_Ctrl FPGA (Board ID) --test?
- 0F: W Load all 4 DDR InFIFOs

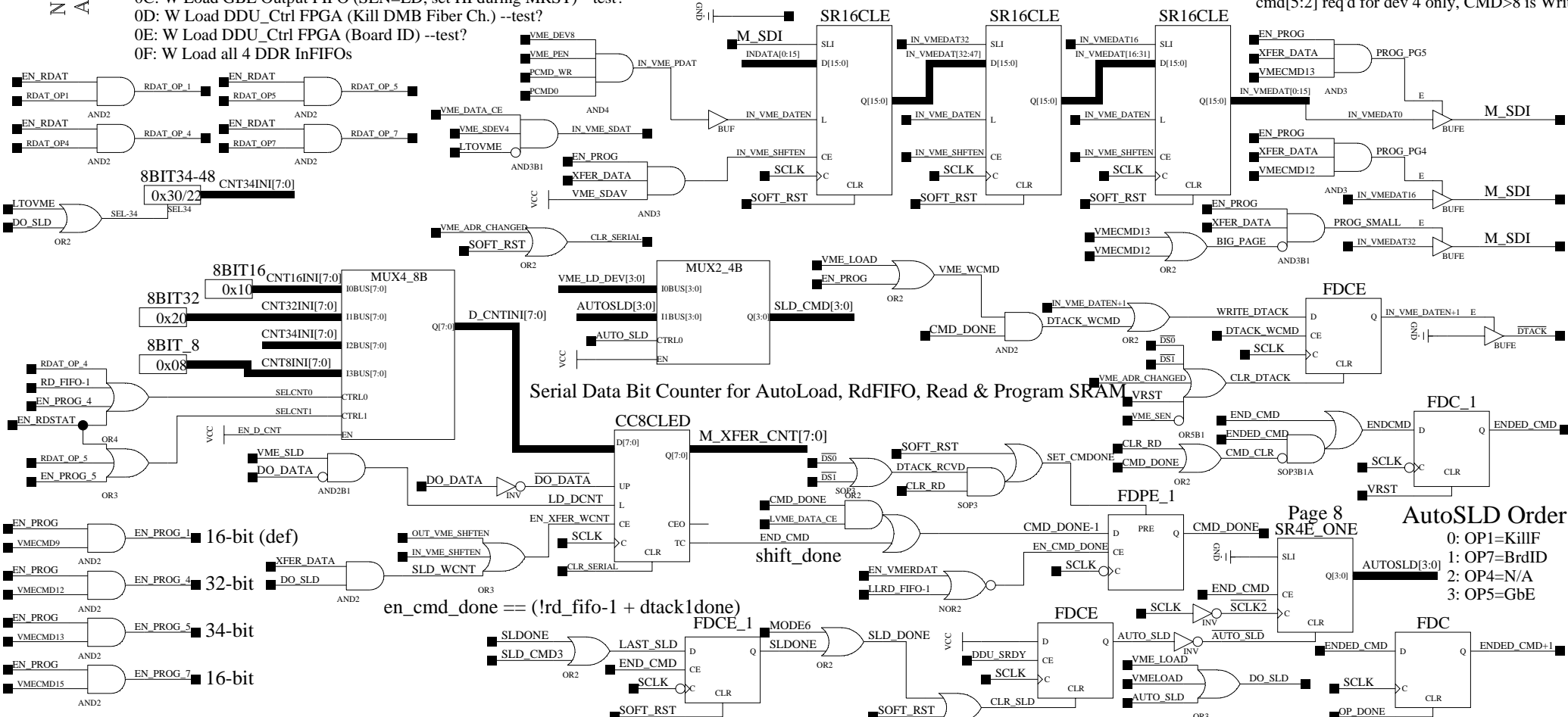
Non-VME!!
Auto Load
Only

Flash Memory Access

- CMD<9 is Read Only. CMD>=9 is Write Only.
- 0x 00: Read Status Register
- 01: Read page 1 (Kill Ch.) to DDU_Ctrl
- 04: Read page 4 (DDR offsets) to In DDR FIFO
- 05: Read page 5 (GBE offsets) to GBE Out FIFO
- 07: Read page 7 (Board ID) to DDU_Ctrl
- 0x 09: W Program page 1 (Kill Ch.) [16 bit data]
- 0C: W Program page 4 (DDR offsets) [32 bit data]
- 0D: W Program page 5 (GBE offsets) [34 bit data]
- 0F: W Program page 7 (Board ID) [16 bit data]

Serial VME_ADR: slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]

cmd[5:2] req'd for dev 4 only, CMD>8 is Write

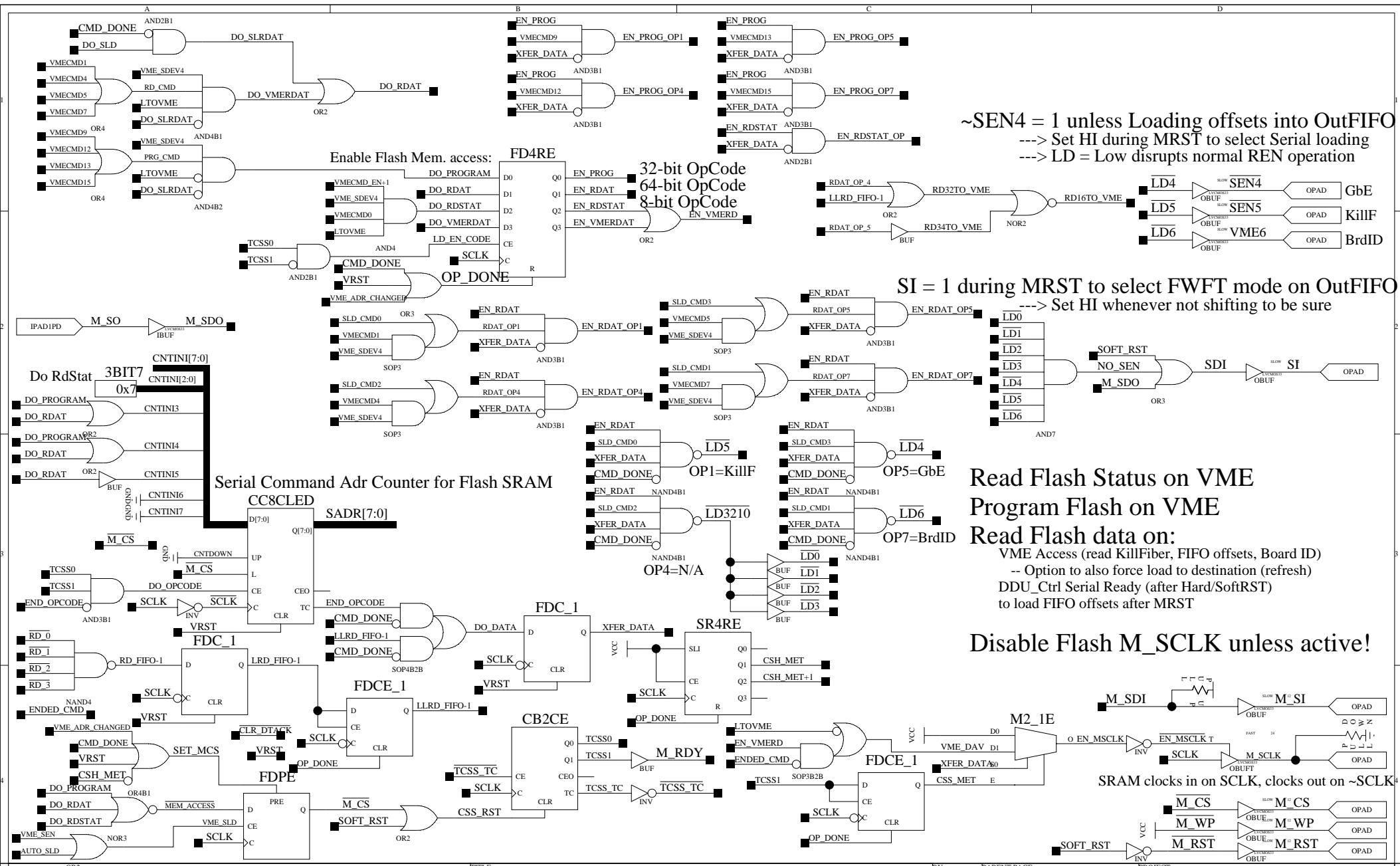


Serial Data Bit Counter for AutoLoad, RdFIFO, Read & Program SRAM

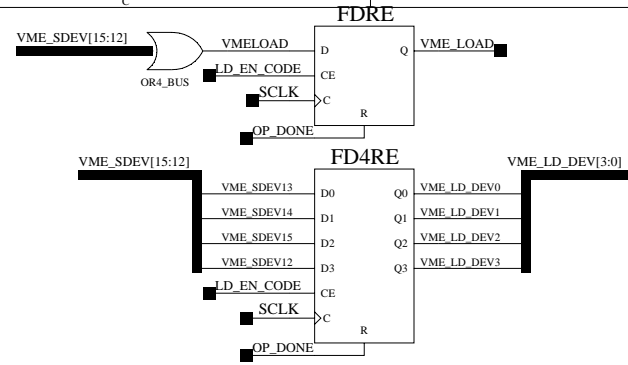
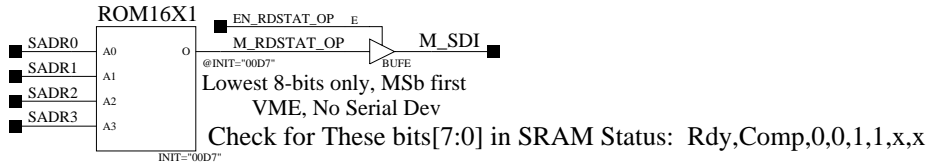
Page 8 AutoSLD Order

- 0: OP1=KillF
- 1: OP7=BrdID
- 2: OP4=N/A
- 3: OP5=GbE

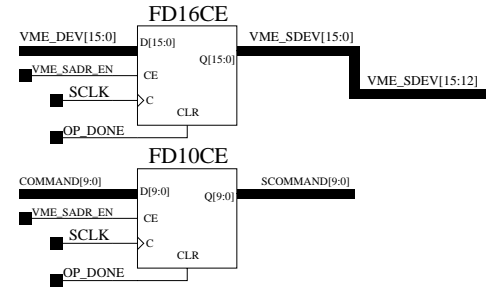
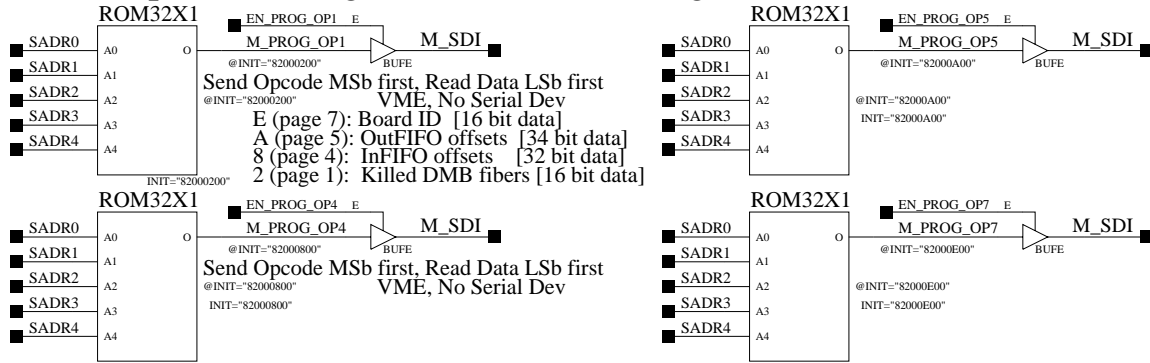
en_cmd_done == (!rd_fifo-1 + dtack1done)



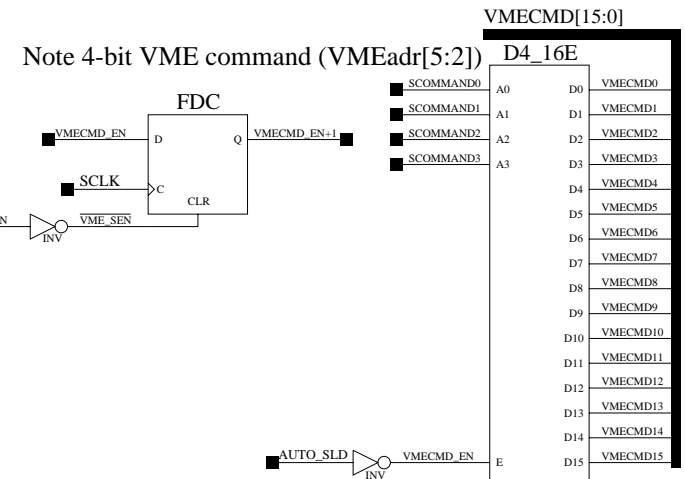
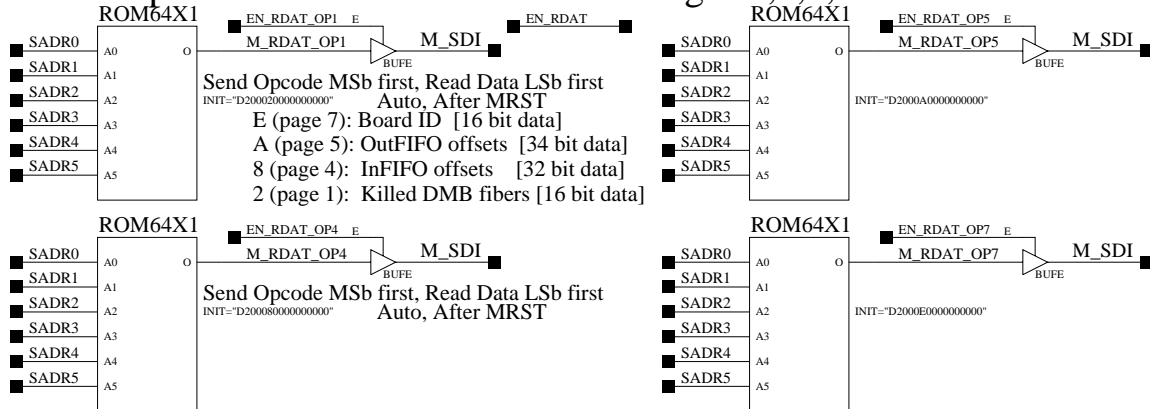
8-bit Opcode: Read Flash SRAM Status



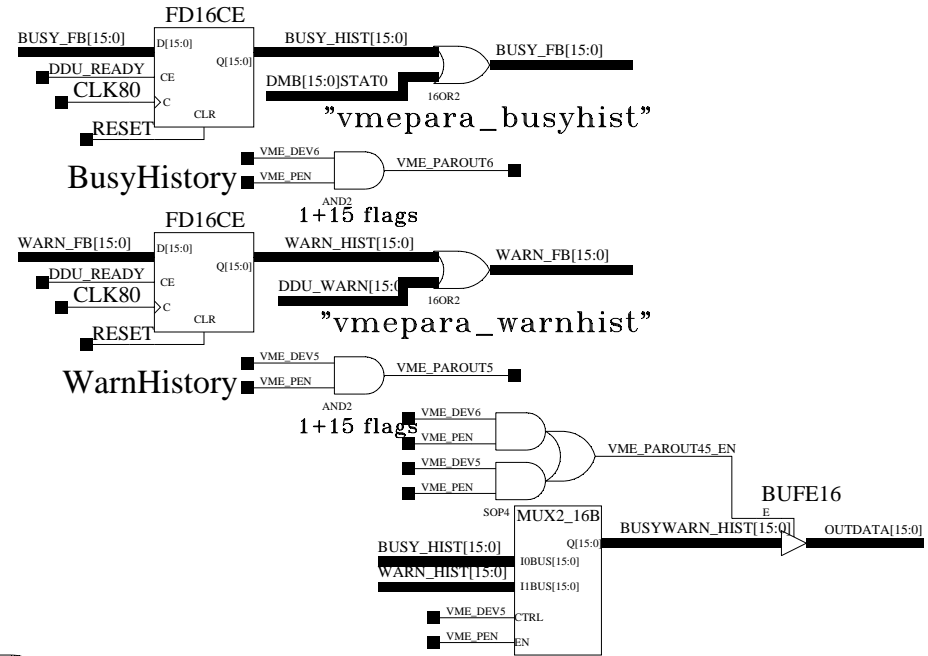
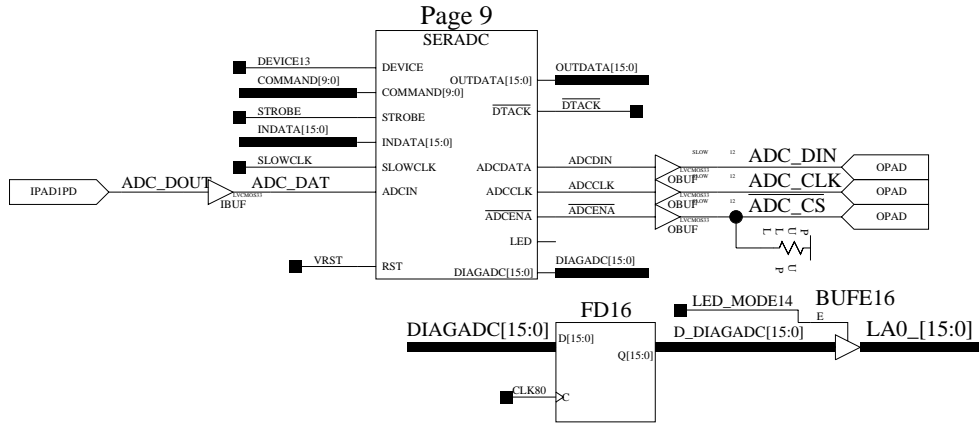
32-bit Opcodes: Program Flash SRAM Pages 1,4,5,7



64-bit Opcodes: Readout Flash SRAM Pages 1,4,5,7

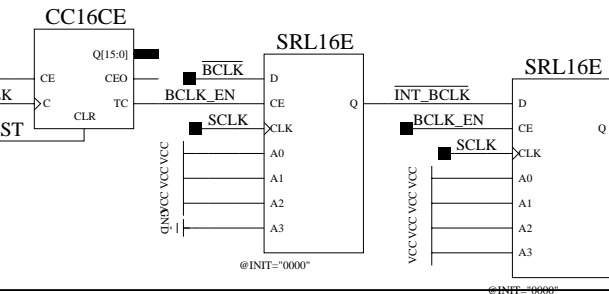
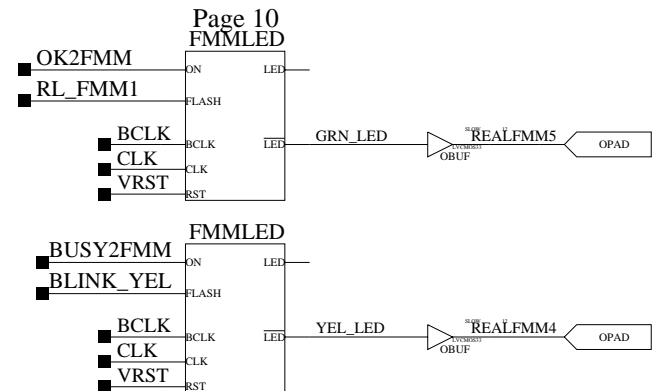
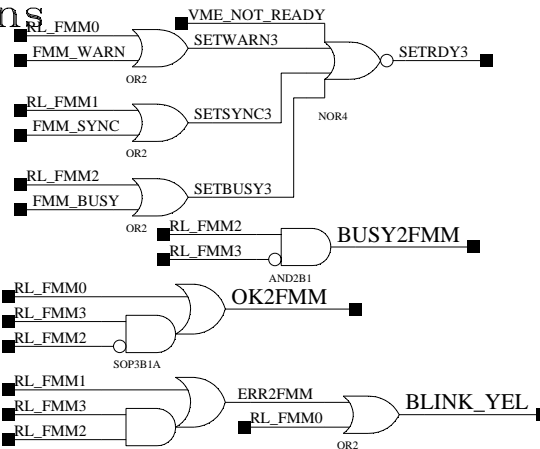


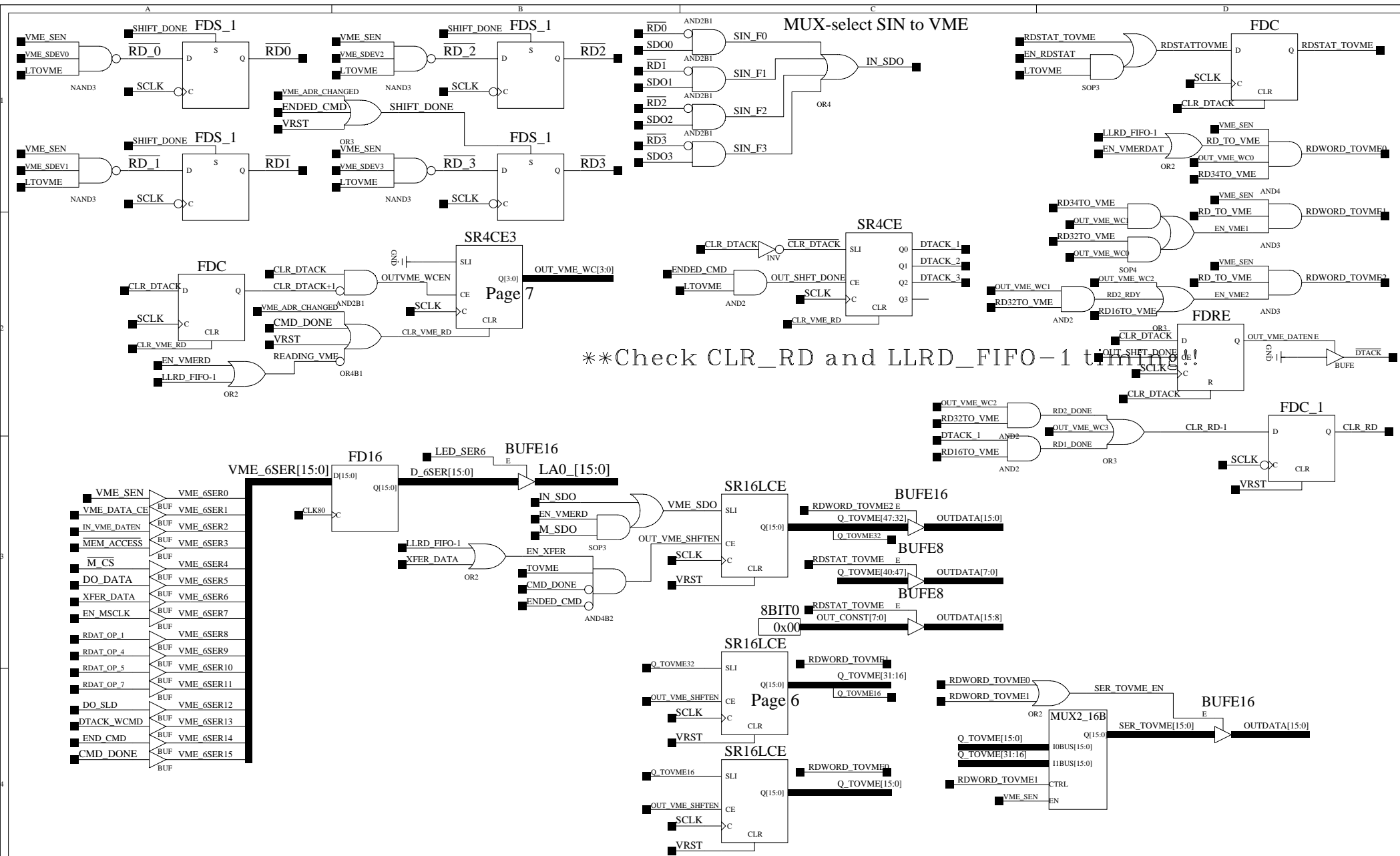
Serial ADC (12-bit, MAX1270/1271) Interface clock: 1.25MHz (Divided SLOWCLOCK) is used
 The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz



REAL_FMM 4-bit-decode definitions

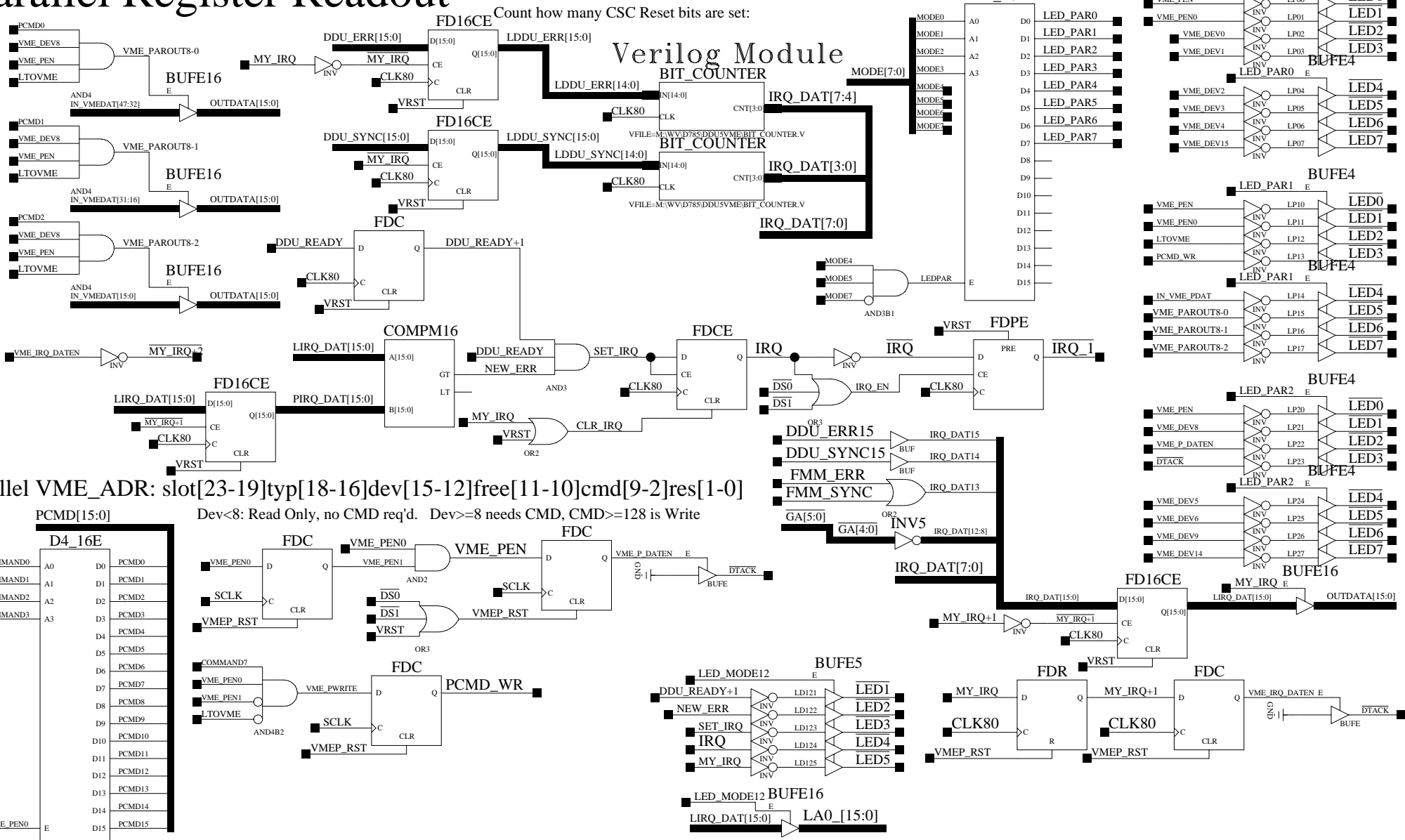
- 0001: Warning/NearFULL (Grn ON, Yel BLINK)
- 0010: Lost Sync, need SyncReset (both BLINK)
- 0100: BUSY (Yel ON)
- 1000: Ready {DDU Ready == !Busy} (Grn ON)
- 1100: Error, need HardReset (Yel BLINK)





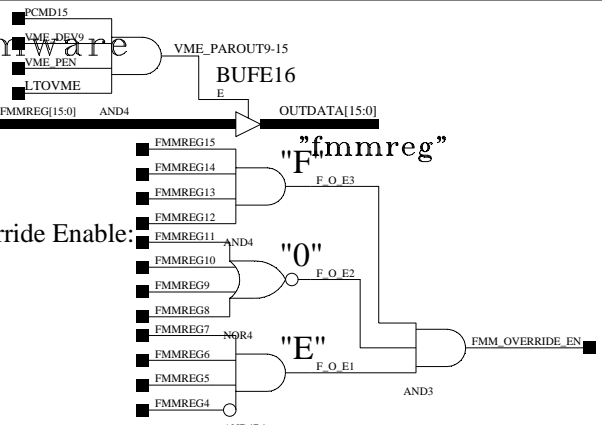
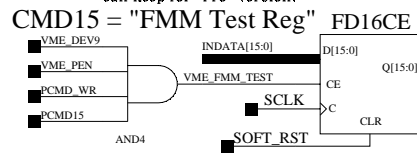
**Check CLR_RD and LLRD_FIFO-1 timing

Parallel Register Readout



Parallel Register Read/Write

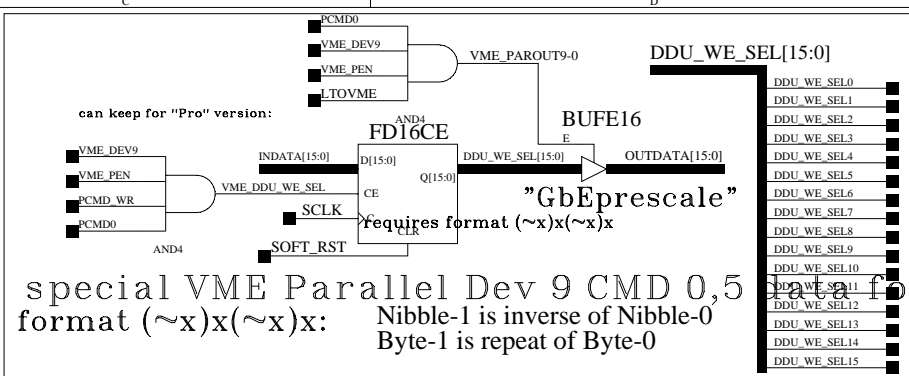
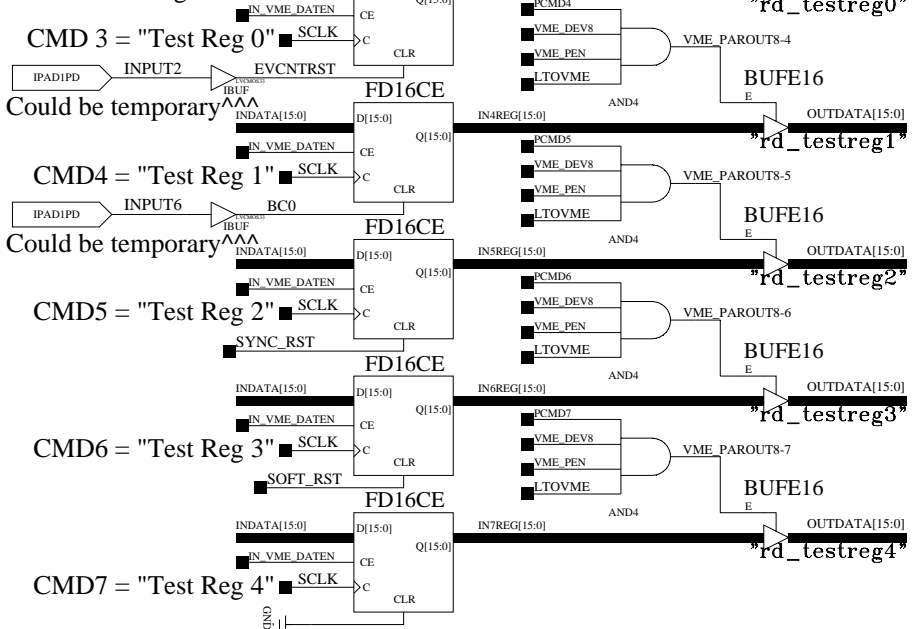
Required for Test firmware



must set "FOE" FMM Override Enable:
 Dev9, CMD 0F/8Fh (R/W)
 bits15-4: "FOEh"
 bits3-0: FMM Bit state to Force

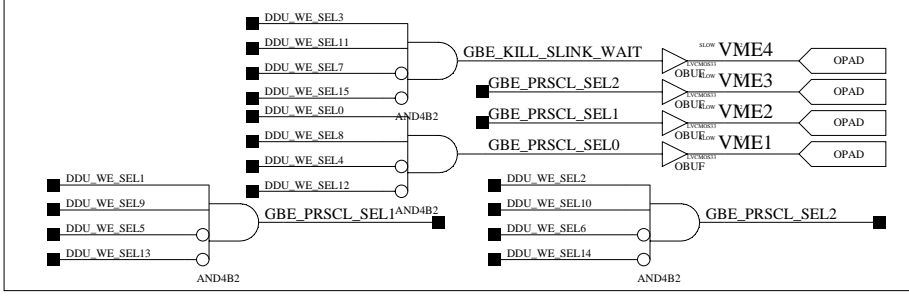
Required for Test firmware

can keep for "Pro" version
 Read Only, VME Par Dev 8:
 writes with InReg0



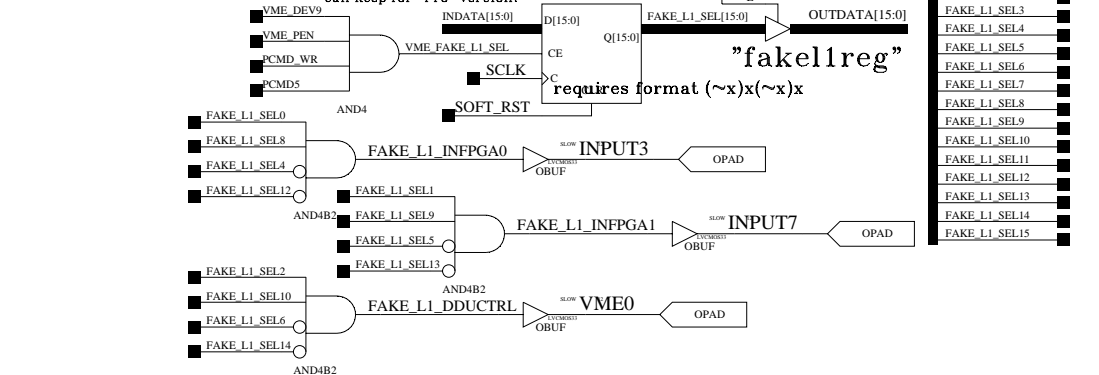
special VME Parallel Dev 9 CMD 0,5
 format (~x)x(~x)x: Nibble-1 is inverse of Nibble-0
 Byte-1 is repeat of Byte-0

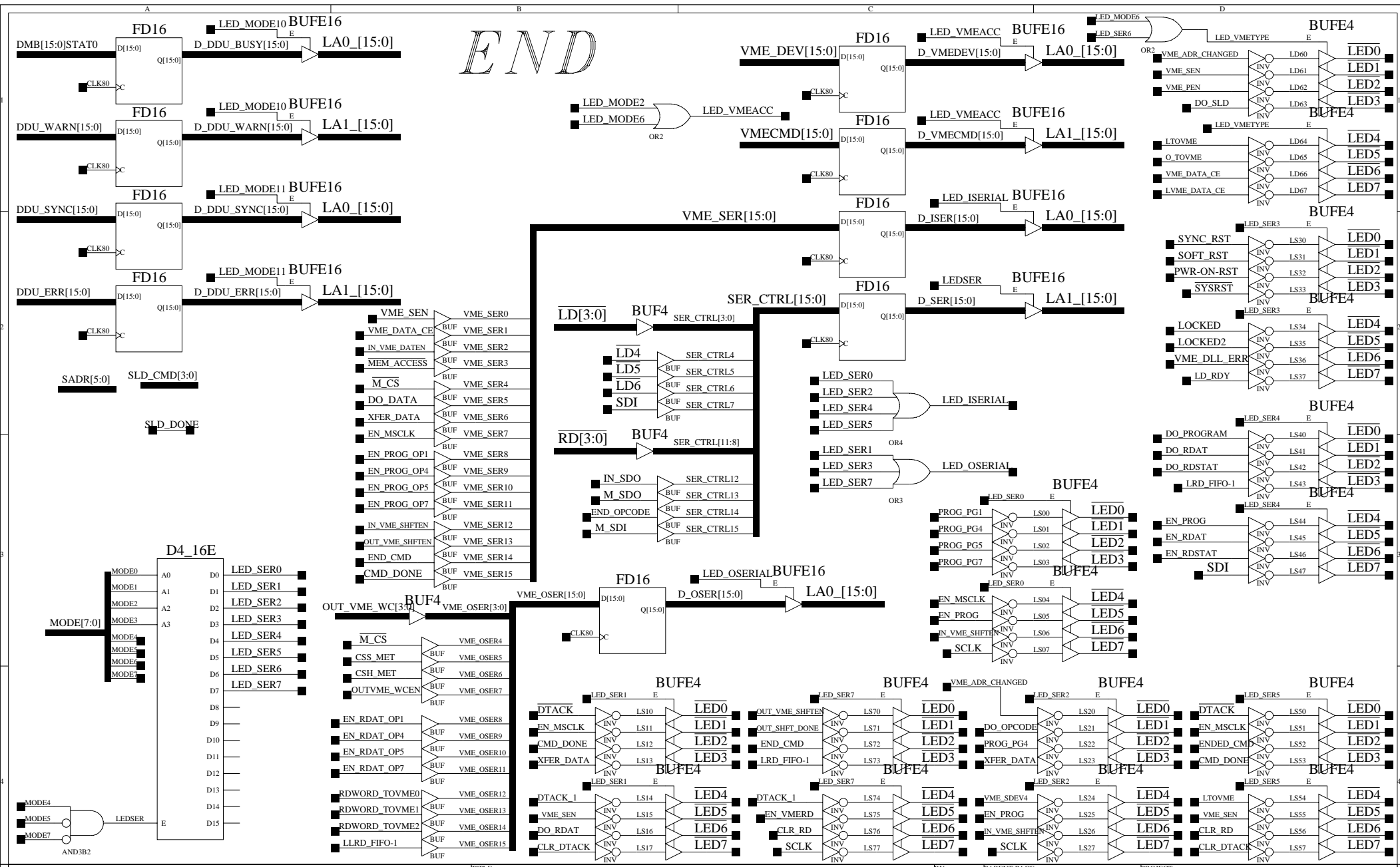
Dev9, CMD 00/80h (R/W)
 bits2-0: GbE Prescale
 bit3: Slink Wait Enable



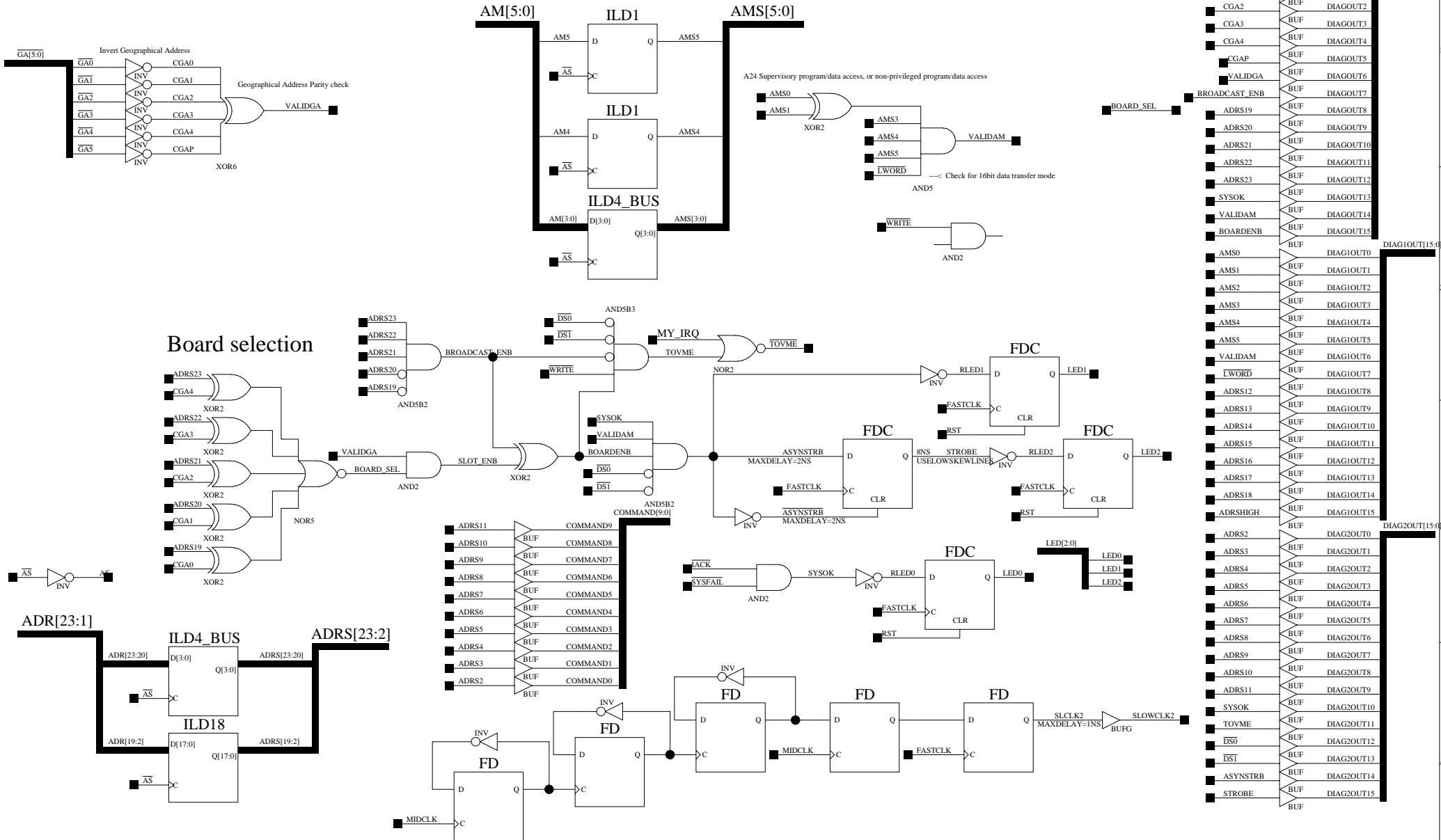
Dev9, CMD 05/85h (R/W)

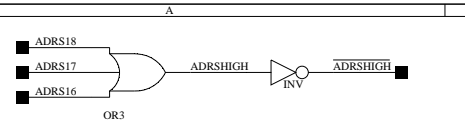
bits2-0: Enable Fake L1A/Data Passthrough
 for each DDU FPGA
 bit3: Not Used





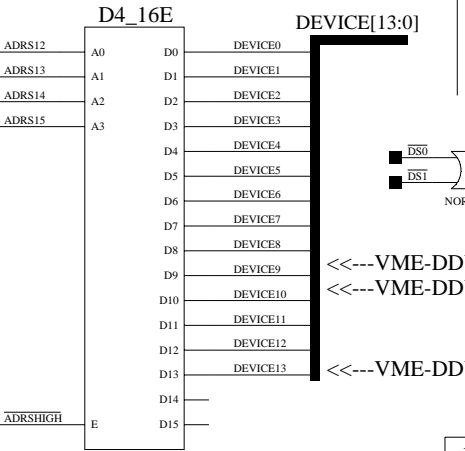
DDU Broadcast Address = 28 = 0x1C = 11100b





VME-JTAG Device code: Path IR bit length

00			
01		Output FIFO **FIX**	4
02		VME_Ctrl PROM (all PROMs=XC18V04)	8
03		DDU_Ctrl PROMs 1 & 0	8+8
04		InCtrl PROMs 1 & 0	8+8
05		DDU_Ctrl FPGA (V2P7)	10
06		InCtrl FPGA 0 (V2P20)	14
07		InCtrl FPGA 1 (V2P20)	14
08		Input FIFOs 0-3	4+4+4+4
09		Serial ADC (...not JTAG...)	N/A
0F		Emergency PROM Programming via VME	8

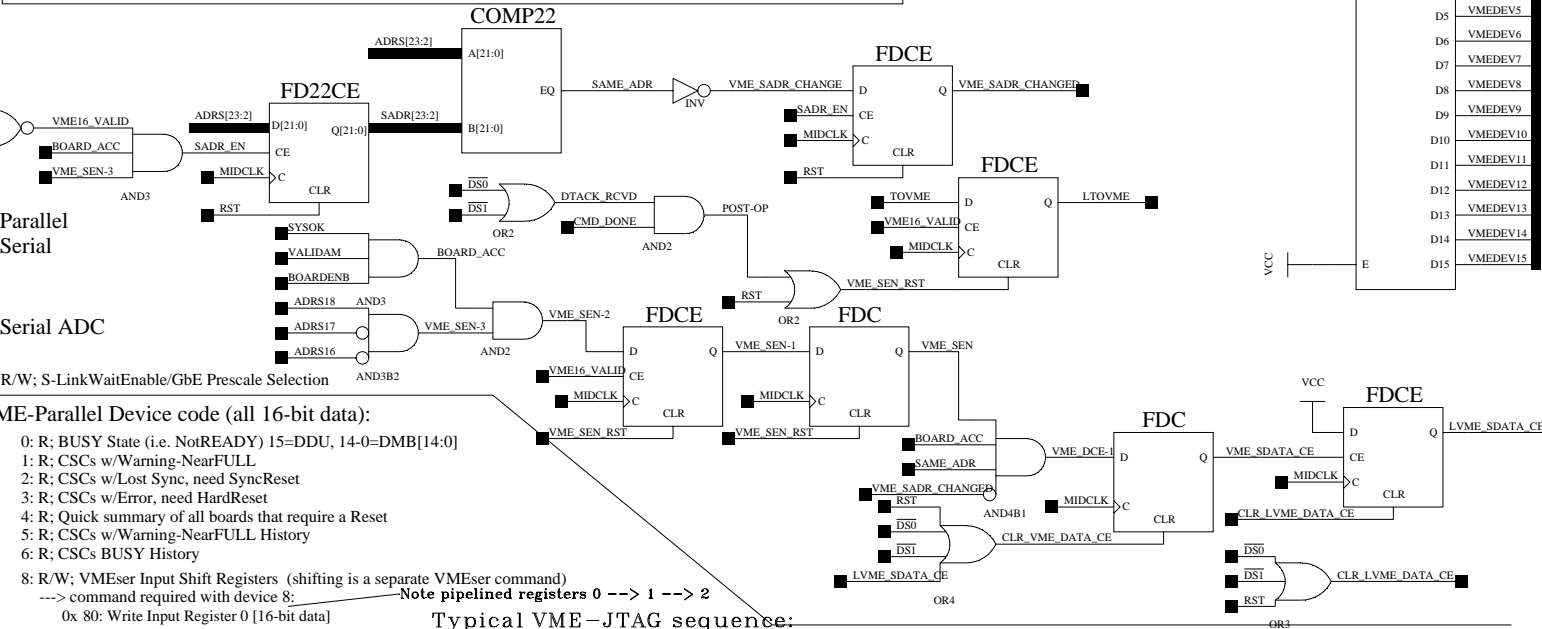


Slot Selection: ADR[23:19] ADR[1:0]=Not Used
 Device: ADR[15:12] sets device ID
 Type: ADR[18:16]=000b for VME-JTAG
 COMMAND[9:0] { ADR[11:8]=bit count
 ADR[7:2]=JTAG command
 slot[23-19]typ[18-16]dev[15-12]bitcnt[11-8]cmd[7-2]res[1-0]
 ADR[18:16]=100b for VME-Serial
 COMMAND[9:0] { ADR[11:6]=Not Used
 ADR[5:2]=serial command (req'd for dev 4 only)
 slot[23-19]typ[18-16]dev[15-12]free[11-6]cmd[5-2]res[1-0]
 Dev>=8: Write Only. Dev=4 needs CMD, CMD>=9 is Write. Otherwise Read
 ADR[18:16]=011b for VME-Parallel
 Dev<8: Read Only, no CMD req'd. Dev>=8 needs CMD, CMD>=128 is Write
 slot[23-19]typ[18-16]dev[15-12]free[11-10]cmd[9-2]res[1-0]

VME-Serial Device code: "iadr" in scan.c

04 || Flash SRAM (RdStat or Program Page), NEEDS COMMAND
 ---> command required with device 4:
 0x 00: Read Status Register [8-bit data]
 09: Program page 1 (Kill Ch.) [16 bit data]
 xx 0C: Program page 4 (DDR offsets) [32 bit data] xx
 0D: Program page 5 (GBE offsets) [34 bit data]
 0F: Program page 7 (Board ID) [16 bit data]

0C || Load GBE Output FIFO (SEN=L.D, set HI during MRST)--N/A
 0D || Load DDU_Ctrl FPGA (Kill DMB Fiber Ch.)--N/A
 0E || Load DDU_Ctrl FPGA (Board ID)--N/A



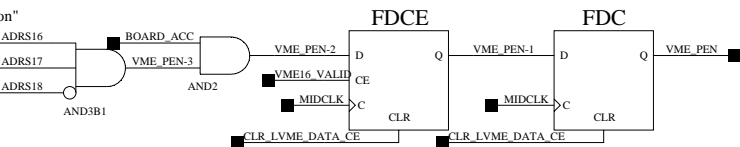
VME-Parallel Device code (all 16-bit data):

0: R; BUSY State (i.e. NotREADY) 15=DDU, 14-0=DMB[14:0]
 1: R; CSCs w/Warning-NearFULL
 2: R; CSCs w/Lost Sync, need SyncReset
 3: R; CSCs w/Error, need HardReset
 4: R; Quick summary of all boards that require a Reset
 5: R; CSCs w/Warning-NearFULL History
 6: R; CSCs BUSY History
 8: R/W; VMEser Input Shift Registers (shifting is a separate VMEser command)
 ---> command required with device 8: Note pipelined registers 0 ---> 1 ---> 2
 0x 80: Write Input Register 0 [16-bit data]
 00-02: Read Input Register 0-2 [16-bit data]
 03-07: Read Only RstTestReg 0-4 [16-bit data]
 9: R/W; command required to specify register
 0x 00/80: R/W S-LinkWaitEnable & GbE Prescale [16-bit data]
 05/85: R/W Fake L1 Register (Data Passthrough) [16-bit data]
 0F/8F: R/W FMM Test Register [16-bit data]

14: R; bits 15-8="CAh", 7-0=ModeSwitch[7:0]
 15: R; VMEfpga Status bits (VMErdy, FMM, Geog/Slot Adr)

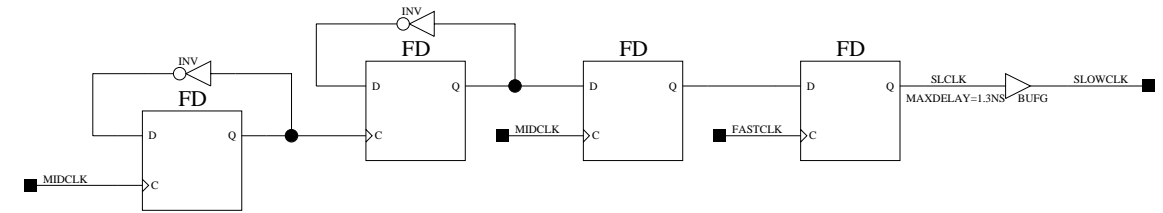
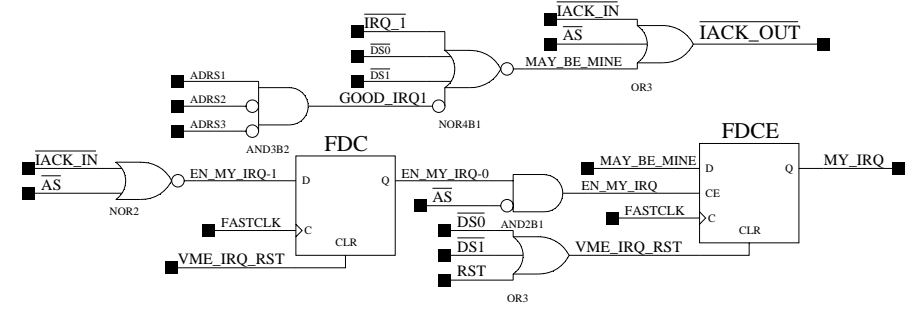
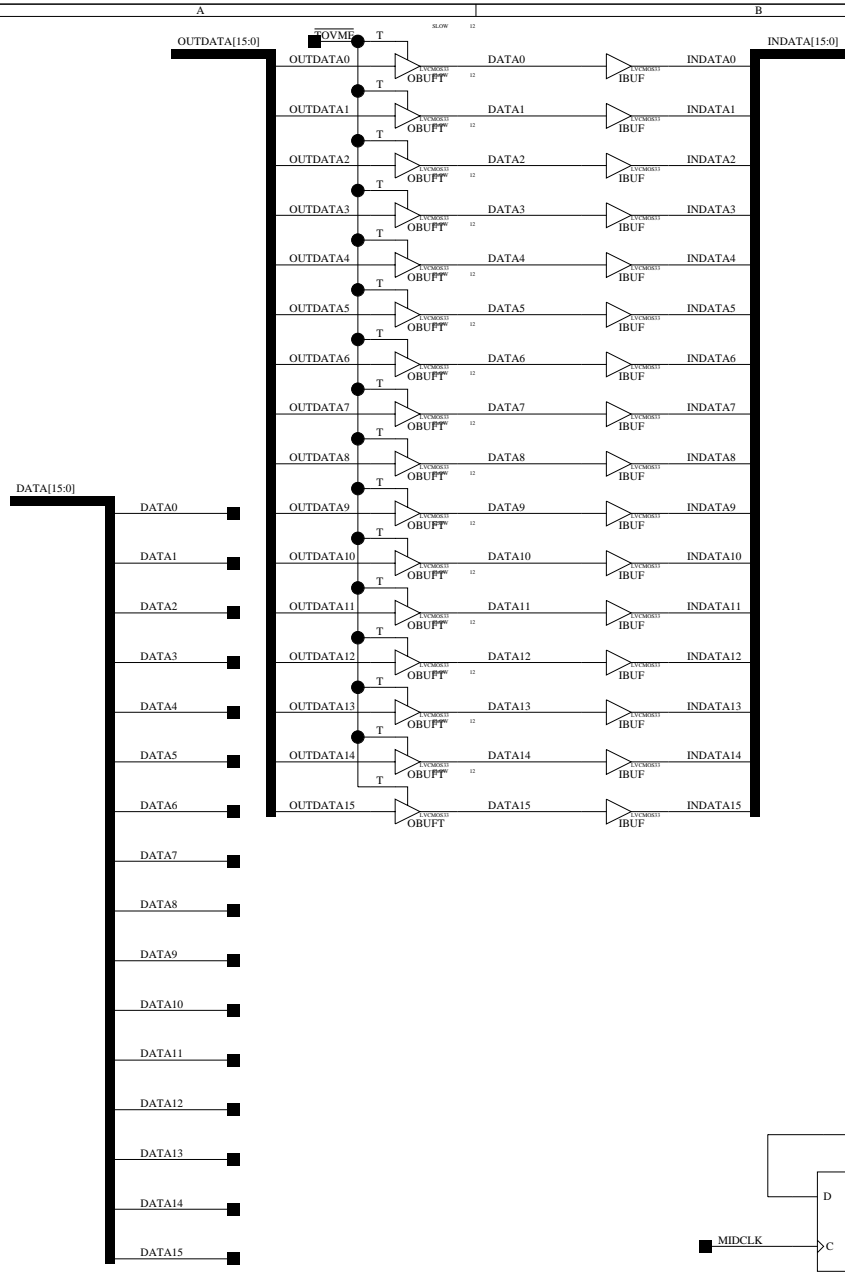
Typical VME-JTAG sequence:

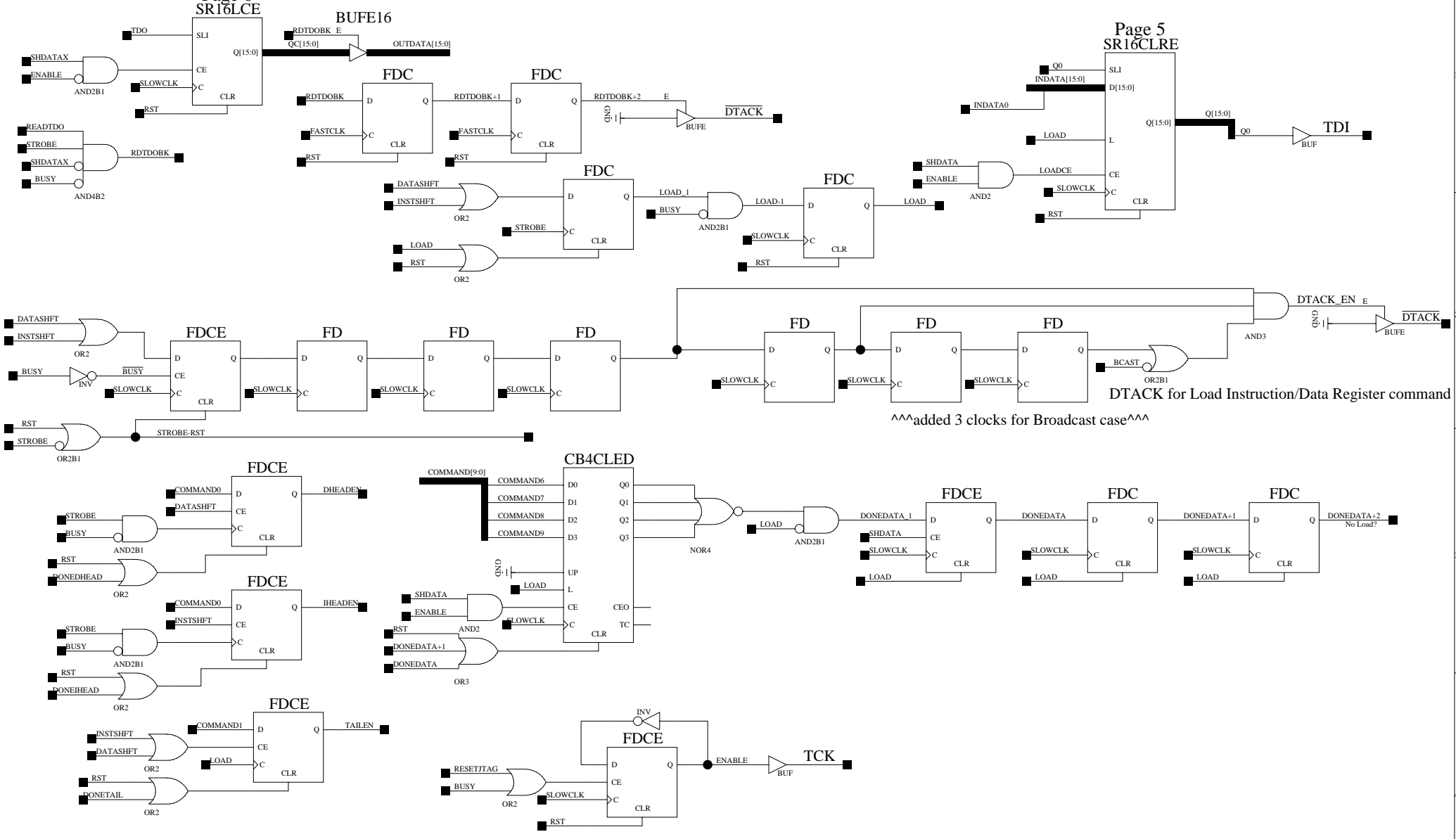
- 1st VME Data: send IR (10-bit) "User1"
- 2nd VME Data: set User1 DR (8-bit) "Select Function"
- 3rd VME Data: send IR (10-bit) "User2"
- 4th VME Data: send User2 DR (16-bit)
- 5th VME Data: send IR (10-bit) "User1"
- 6th VME Data: set User1 DR (8-bit) "No-Op"
- 7th VME Data: send IR (10-bit) "Bypass"

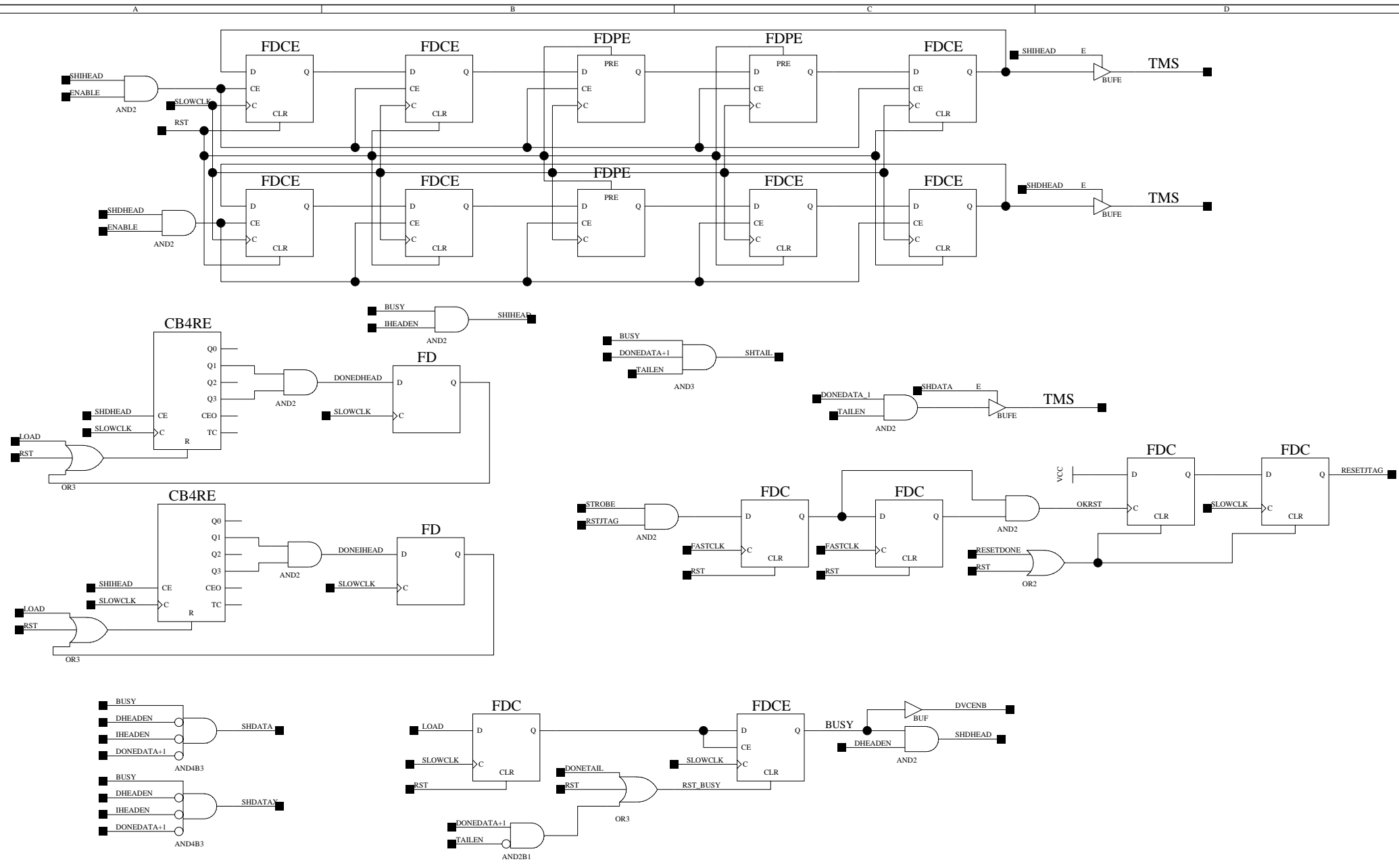


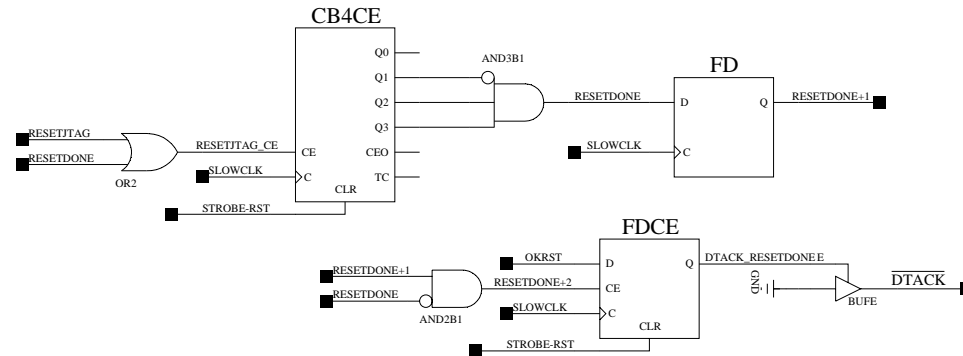
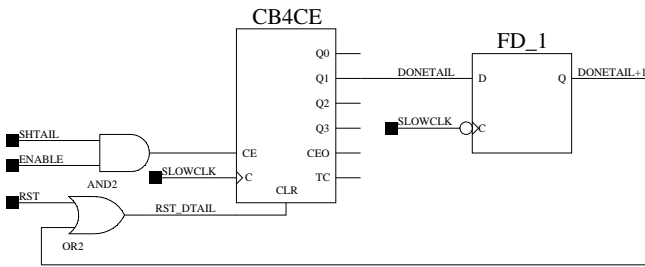
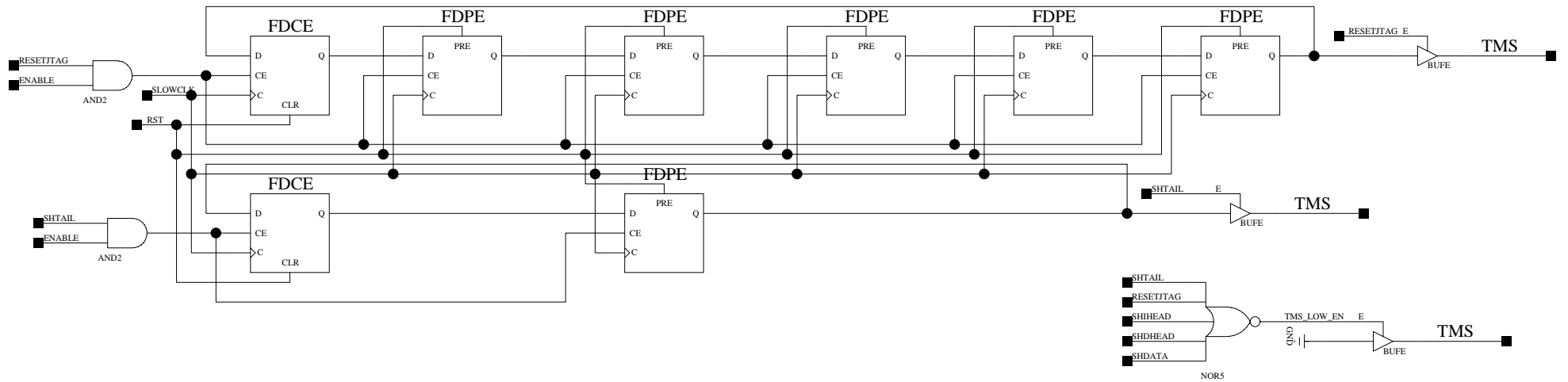
Boundary Scan IR Codes	PROM XC18V04 8-bit IR	FPGA Virtex2Pro 10-bit IR
Device Bypass	11111111	1111111111
User Code	11111101	1111001000
ID Code	11111110	1111001001
User1	N/A	03C2h=1111000010
User2	N/A	03C3h=1111000011

For bigger V2P's add 1's to the left



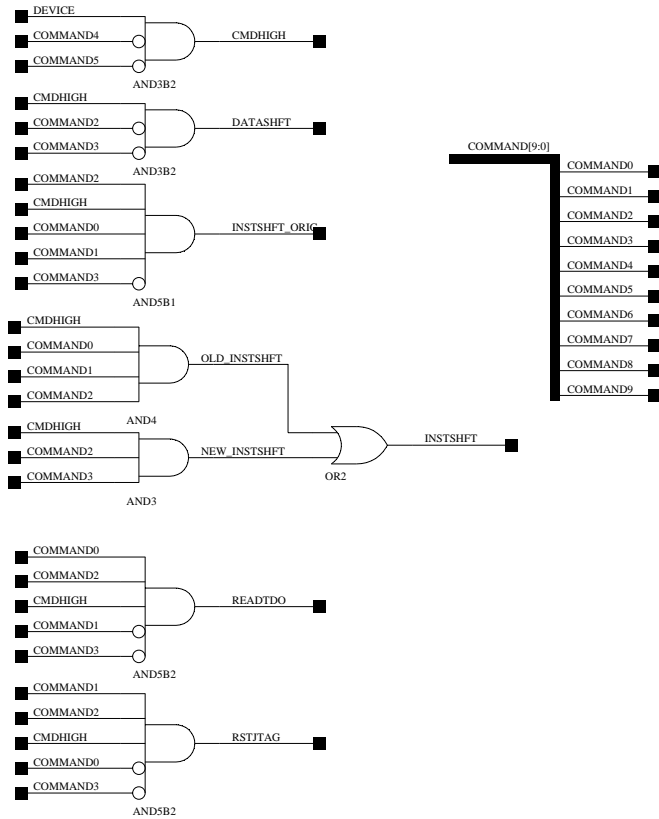






^^^added 3 clocks for Broadcast^^^

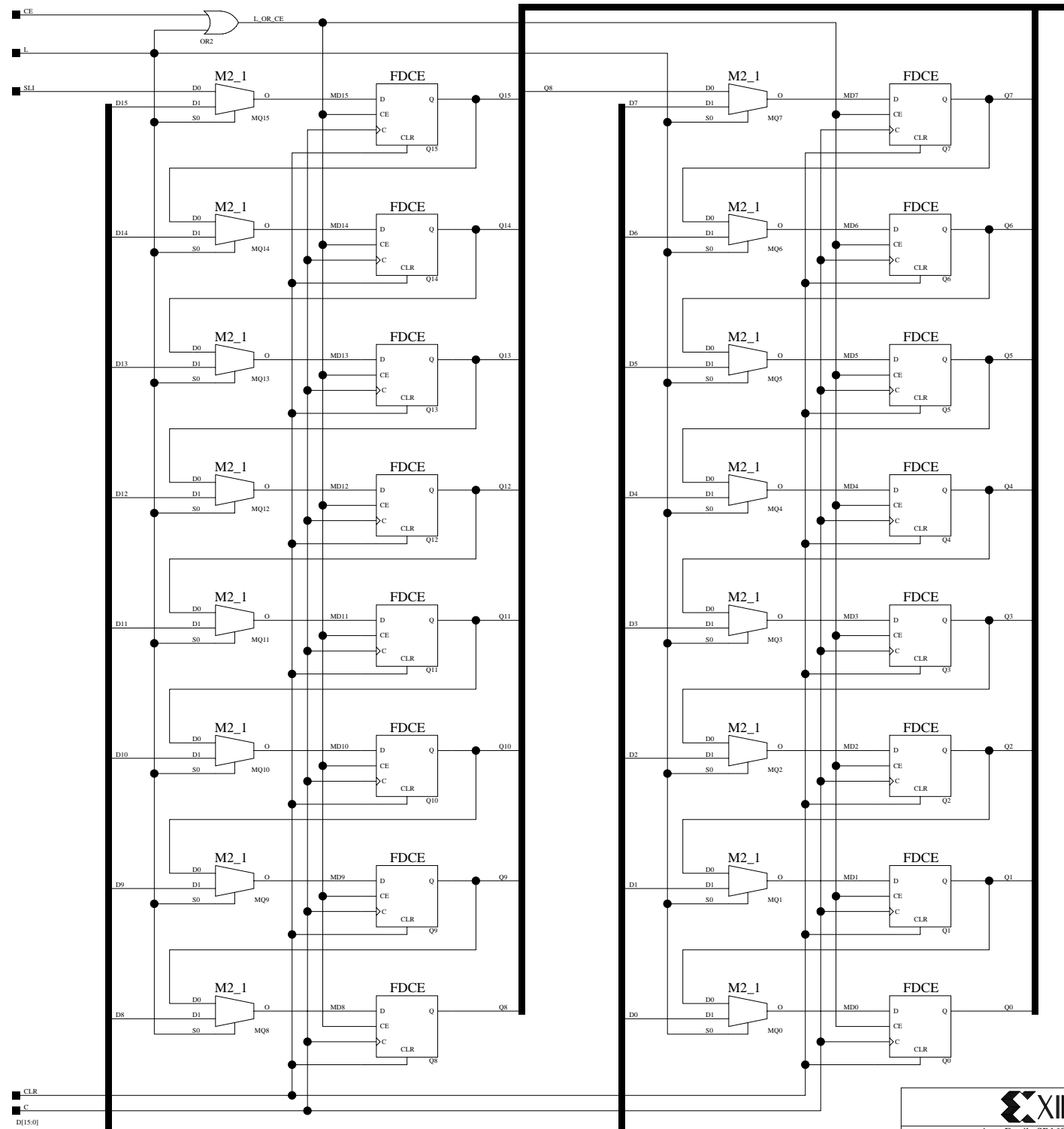
CFEB JTAG command decode



CFEB JTAG commands:

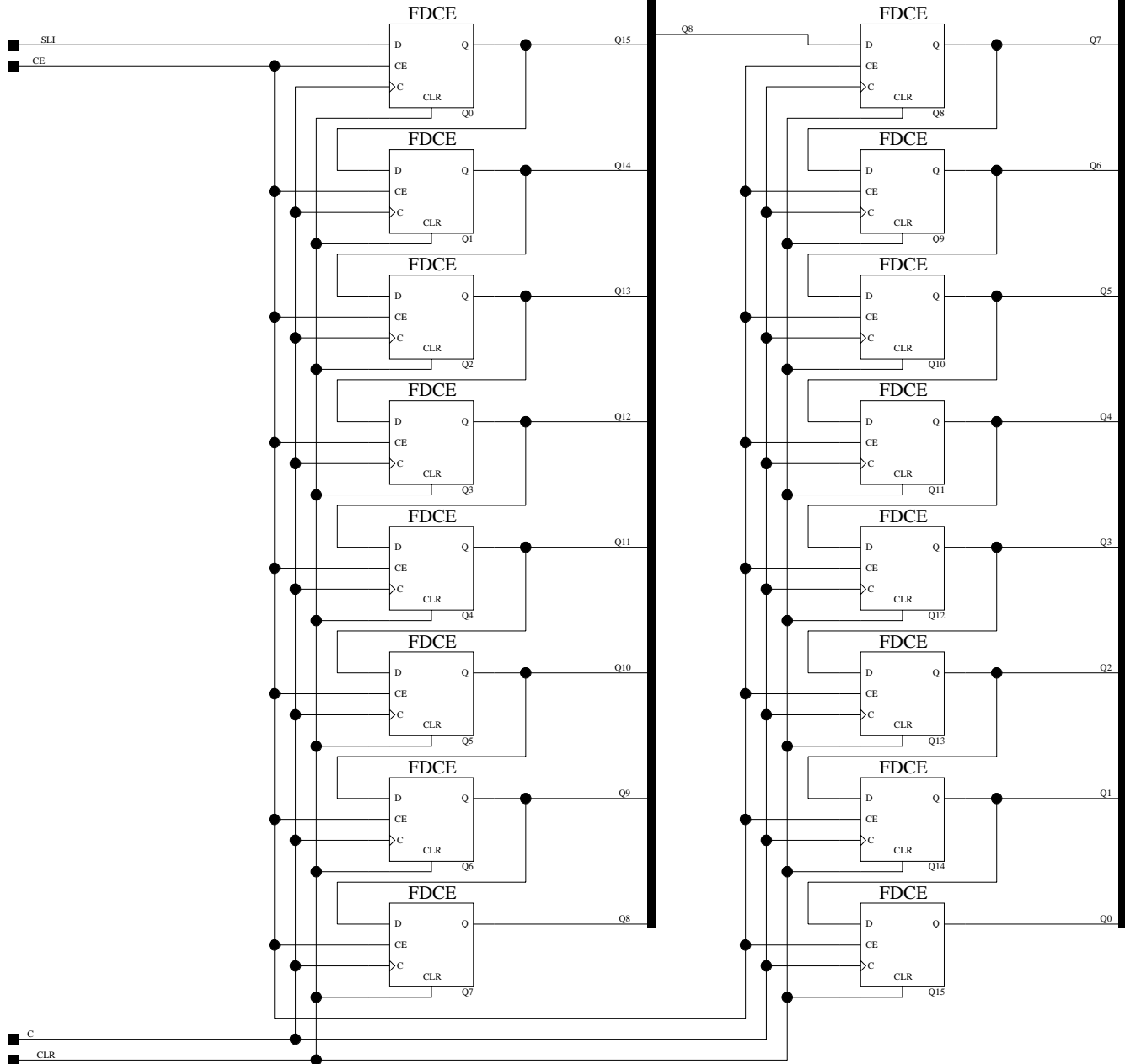
- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register with header and tailer

- 0C || Shift IR, no header, no tailer
- 0D || Shift IR with header only
- 0E || Shift IR with tailer only
- 0F || Shift Instruction register with header and tailer



CLR
 C
 D[15:0]

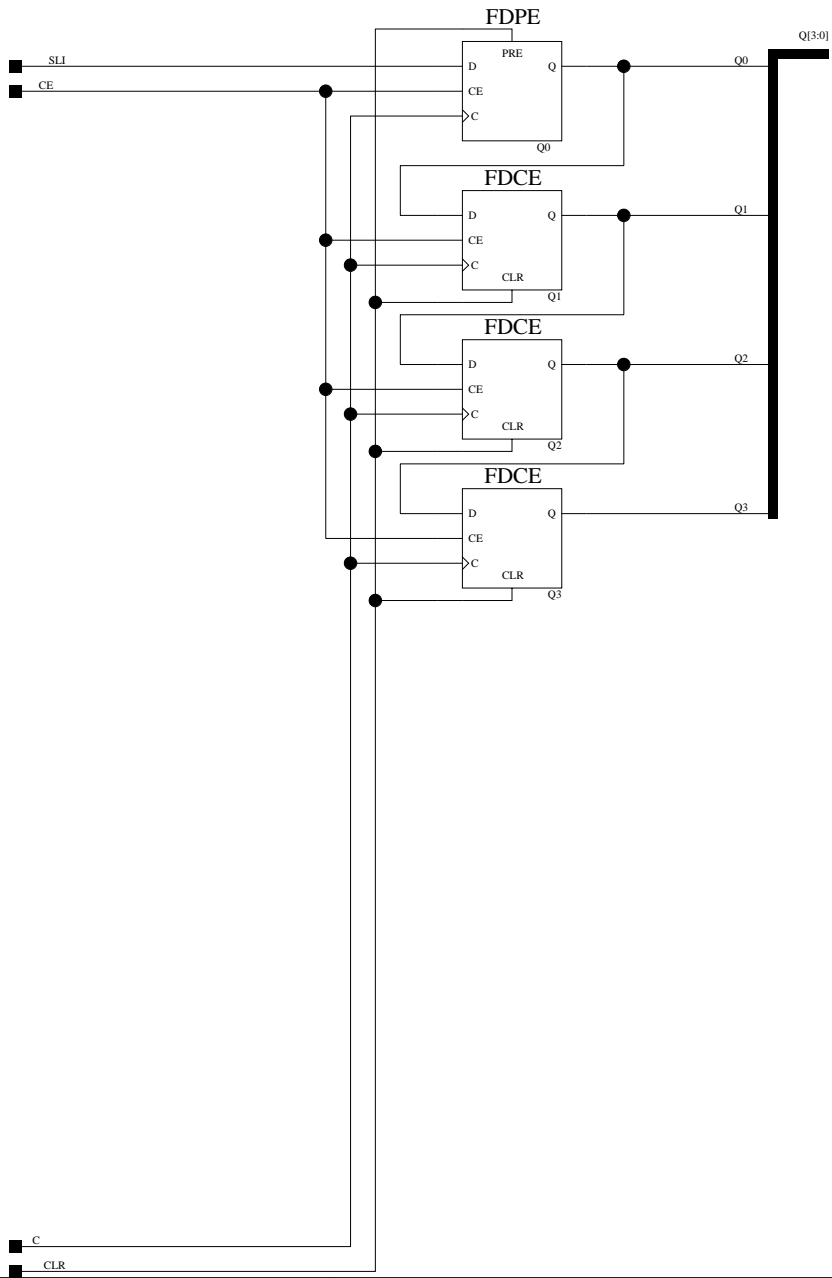
XILINX		J. Gu
Title: virtex Family SR16CLRE Macro, Right Shift		
Comments: 16-Bit Loadable Set/Para-In, right shift Para-Out Shift Reg w/ Enable & Async Clr		
Date: 13th January 1993	Ver: 1, Modified from XILINX, SR16CLE	
Sheet Size: C	Rev: A	



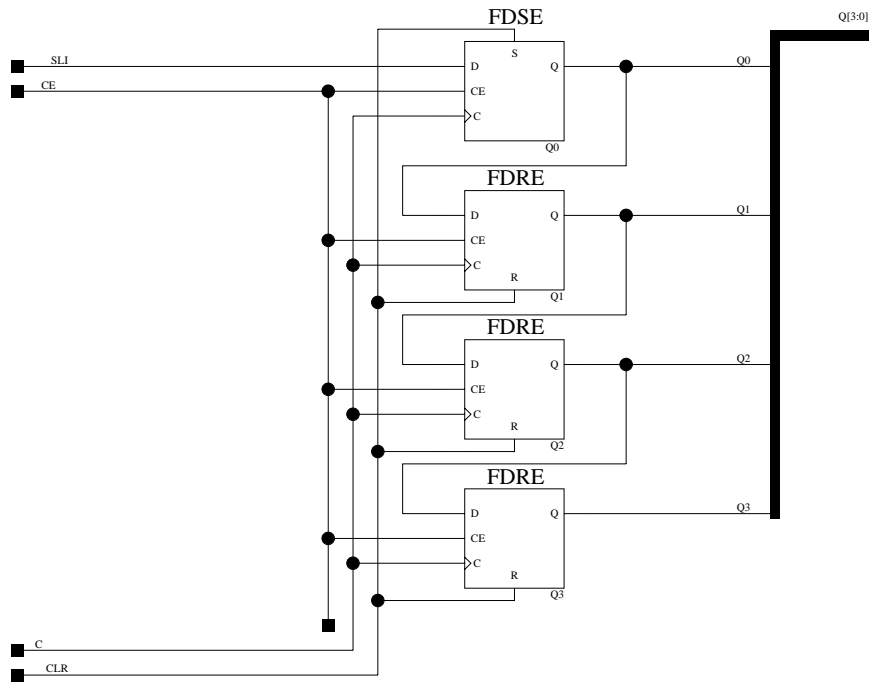
J. Gu

Title:	virtex Family SR16LCE Macro		
Comments:	Modified from XILINX Library SR16CE, shift right	16-bit Serial-In Parallel-Out	Shift Register w/ Enable and Async Clr
Date:	11th May 2001	Ver:	1
Sheet Size: B		Rev:	

drawn by KS
Copyright (c) 1993, Xilinx Inc.



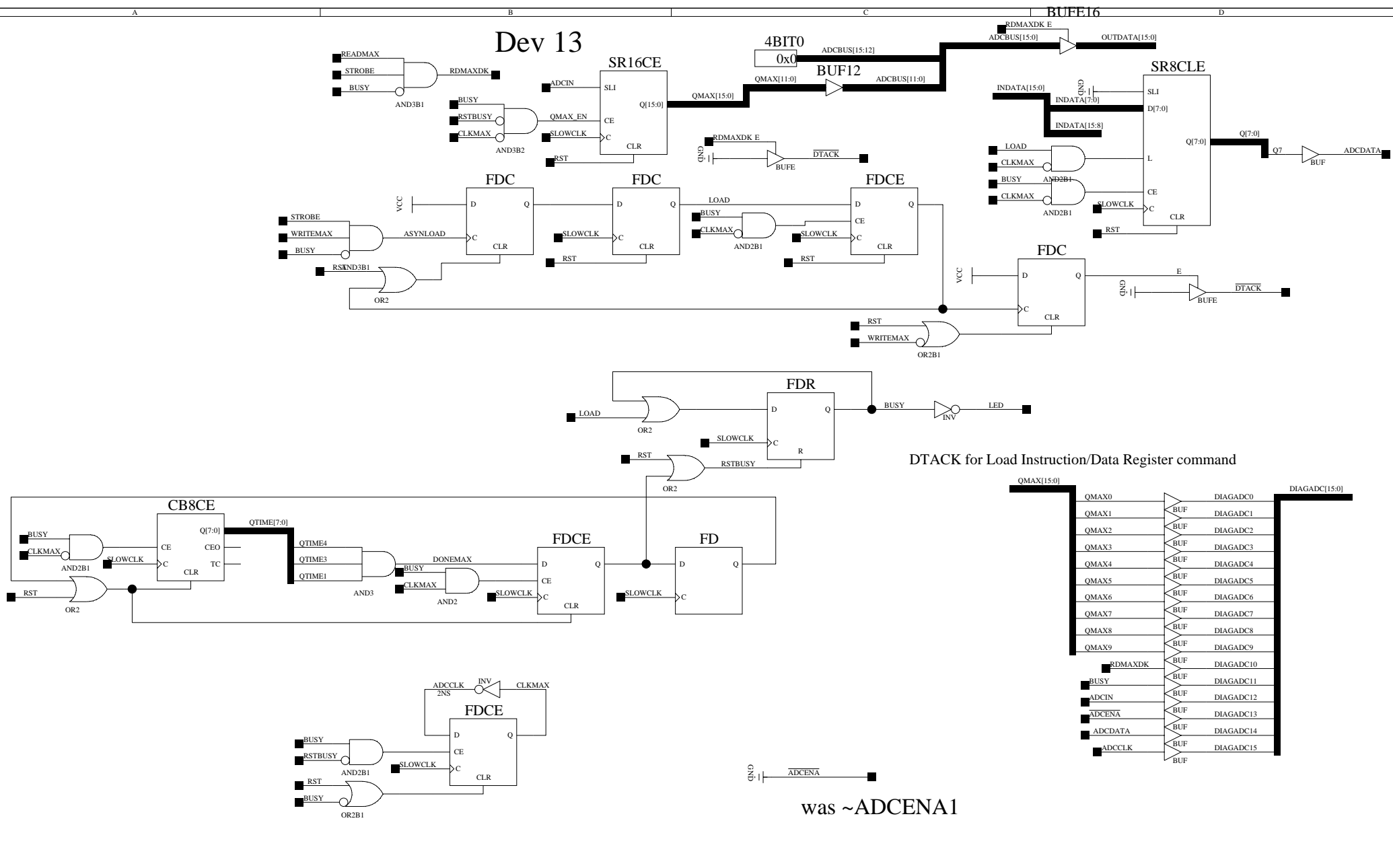
Title:	VIRTEX Family SR4CE3 Macro (Set 1, Clear 3)	JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/Enable, 1 Preset & 3 Async Clr	
Date:	13th October 2003	Ver: 1
Sheet Size: B		Rev: A



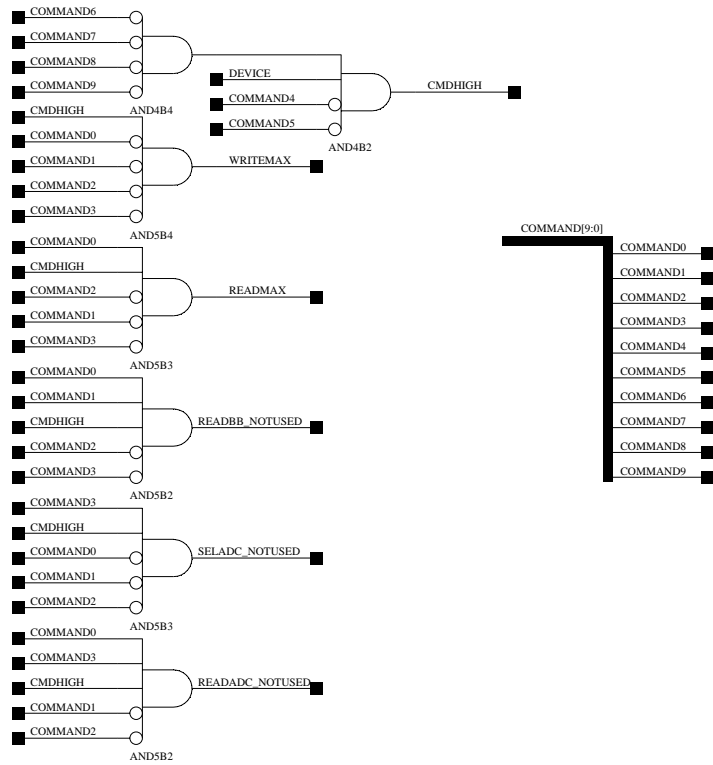
drawn by KS
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Title: VIRTEX Family SR4RE Macro (SR4E_ONE)		JRG
Comments: 4-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single "one" on Sync Reset		
Date: 7th August 2001	Ver: 1	
Sheet Size: B	Rev: A	

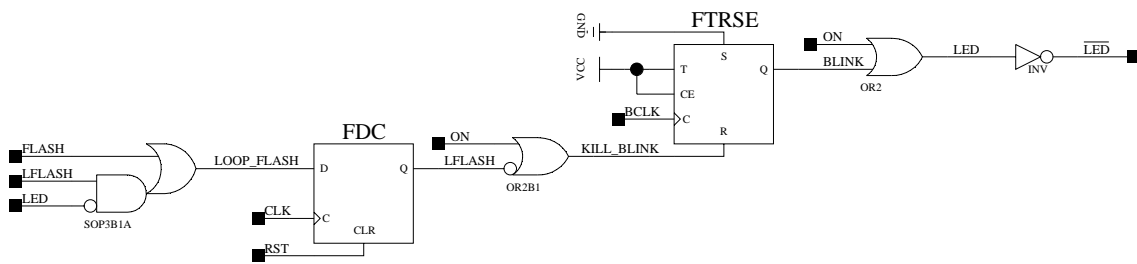


CFEB JTAG command decode



Serial ADC Command Decoder:

- 00 || Write Control Byte to MAX1271's
- 01 || Read Data Back from 1271 Register
- 02 ||
- 04 ||
- 05 ||
- 06 ||



JRG

Title:	FMMLED	
Comments:	Custom LED Slow-Blink Control for FMM Outputs	
Date:	27th January 2004	Ver: 1
Sheet Size: B		Rev: A