this DDU:
RXER words are skipped, FILLER added as needed
- Use code "C" with FILL flag set (b34 & b16)
  -- could use code "8" instead...
- Should we Reset RxErr Monitor?  How?
PART=XC2VP20-6-FG676
AVOID=Y21, E23, C22, E21
(INIT, BUSY, WRITE, CS)
NC_XCV400_FG676=B13, AF13
NC_XCV400E_FG676=D13, Y13
VME Broadcast Addresses:
24=OSU-TCB "Test Control Board"
25=DMB
26=TMB
27=Both DMB and TMB
28=DDU
22=DCC

DDU Format Since DDUctrl v15:

**Mode 1 Switch Block**
1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
7: Set Fake_L1A (data passthrough)
8: Show STAT31-0 on LAs, ~FPGA version on LEDs

**DDU WordCount**

DDU WordCount (64-bit words) for "No Data" event: 0x0006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 2 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 3 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes

**To Do:**
- COMPARE LUNK & INK (DMB/TMB (conf))
  add INK offset compatible to INIT?
- use DDU-DLL fiber to VD0 DMB on FULL check
- fix for TMB buffer overflows
- No logic for TUNN, CUNN, TMB/L, Model/4...GL.
- add Instruct Check for DME Tuneout & cali SMB Reset?

**Special Startup Order:**
1) Release WE
2) Release DLL
3) En. Outputs
6) DONE
Mask DMBs with critical error until they're Reset. 

For now just use FIFO. 

---Not useful, comes 3 words too late to stop data. 

---Real PAF @N-7! 

This event is garbage! Set error bit in SLINK... 

SINGLE WARNING 

This reset Required!!! Tell FMM... 

Tell TTS to slow down...
FILL Logic for 2-4 word alignment

Do we really want RXDV to override a FILL?  YES

1.5-logic-step delay
LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data

*Assume 4 E-Codes at DMB End are sequential with no gaps*

- Normal event sync:
  - Lost 1 word OR 3 extra: $X X E E E$
  - Lost 2 words OR 2 extra: $X X E E E$
  - Lost 3 words OR 1 extra: $X X E E E$

- Normal, but lose 1st E-Word:
  - (or lose last E-Word)
    - $X X E E E$

- Normal, but lose 2nd E-Word:
  - (or lose 3rd E-Word)
    - $X X E E E$

- Normal, but BAD 1st E-Code:
  - $X X E E E$

- Normal, but BAD 2nd E-Code:
  - $X X E E E$

BAD 3rd or 4th E-Code is no problem

---

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Input Unit
DDU Input Controller Logic
CMS CSC Electronics

JRG 174 WEST 18TH AVE, COLUMBUS OH 43210
11-15-2006 15:50
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11-15-2006 15:50
PAGE 2

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11-15-2006 15:50
PAGE 2
Don't use COMMA as RxDV indicator!

Kill WEN & MemReq on Mem Error?
gets 1st mem after HardRST (startup)

Send 2 Idle bytes: K28.5(10111100), D16.2(01010000) = 0x1BC, 0x050 (time-ordered) = 0x50BC (in parallel)
LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data

*Assume 4 E-Codes at DMB End are sequential with no gaps*

Lost 1 word OR 3 extra: X X X X
Lost 2 words OR 2 extra: X X E X
Lost 3 words OR 1 extra: E X E X

Normal event sync:

---

Normal, but lose 1st E-Word:

Normal, but lose 2nd E-Word:

Normal, but lose 3rd E-Word:

Normal, but BAD 1st E-Code:

Normal, but BAD 2nd E-Code:

BAD 3rd or 4th E-Code is no problem

Set LAST Flag for Bad 2nd E-Code case

---

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TITLE: Input Unit
DDU Input Controller Logic
CMS CSC Electronics

JRG 11-15-2006_15:51 2D 174 PAGE 4B

DEPARTMENT: 17
IN_UNIT_B: 3
PAGE: 4B
Custom Logic for DDU
similar to AND12B10 with OR2 (allows ON to override)
Send 2 Idle bytes:
K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050 (time-ordered)
= 0xBC50 (in parallel)
Search "corner fifo_busy" radr for free FIFO.

Which Fibers need a new FIFO?

Corner 0 FIFO usage

Search corner "c0" FIFO availability for use by any fiber. Up-search for "corner Fiber f0", down-search otherwise.

Write "0" into adr "oldmem" to mark FIFO available.

FIFO Release Control

2-bit encoding of active OLDENB

OLDCTRL[1:0]

D2 4E OLDENB[3:0]

Search corner "c0" FIFO availability for use by any fiber.

Up-search for "corner Fiber f0", down-search otherwise.

Write "0" into adr "oldmem" to mark FIFO available.
Corner 1 FIFO usage

Search "corner fifo busy" register for free FIFO

write "0" into addr "oldmem" to mark FIFO available

Up-search for "corner Fiber f3", down-search otherwise.

Assign Fiber to FIFO & Assign FIFO to Fiber

How many of 22 FIFOs are free?

set for WARN at <= 3

COMP4
Write Control

MemIn-MemOut Mapping:
- DO35  Dout35
- DO34  Dout17
- DO33-26  Dout34-27
- DO25-18  Dout16-9
- DO17  Dout26
- DO16  Dout8
- DO15-8  Dout25-18
- Din7-0  Dout7-0

First Word Fall Through logic:
- Not Used: REN = OE * RD_EN
Write Control

FNEXT, FWEN & FxDIN come from the 4 InUnits.
ASF & ASF_ADR come from MemCtrl.
FAD is the fixed FIFO location reference.
 MemIn-MemOut Mapping:

<table>
<thead>
<tr>
<th>Din35</th>
<th>Din35</th>
</tr>
</thead>
<tbody>
<tr>
<td>Din34-27</td>
<td>Din33-26</td>
</tr>
<tr>
<td>Din26</td>
<td>Din17</td>
</tr>
<tr>
<td>Din25-18</td>
<td>15-8</td>
</tr>
<tr>
<td>Din17</td>
<td>Din34</td>
</tr>
<tr>
<td>Din16-9</td>
<td>Din25-18</td>
</tr>
<tr>
<td>Din8</td>
<td>Din16</td>
</tr>
<tr>
<td>Din7-0</td>
<td>Din7-0</td>
</tr>
</tbody>
</table>

but 4 input logic should optimize to 1 LUT=4.5 step delay.

4.5-logic-step delay (WEN)

need to write one more after FULL-3 to make it EVEN

only 120 writes from FULL, 95%
4th September 2003

11-Bit Cascadable Binary Counter

VIRTEX Family CC11CE Macro

with Clk Enable & Async Clr (using MUXCY_L).

RPM_GRID coords X0Y0.

Comments:

Date:

Title:

Ver:

Rev:

Sheet Size: D
UP = Increment 1
UP.DOWN = Decrement 1
DOWN = Decrement 2
Assume that CE includes DOWN+UP
IN16/34 == FILL
IN17/35 == LAST

prompt on OEFOK

IN35 == EVEN_OUT

Null data on OUT[35:0]

At LOUT/DOUT == Timing near EOE

1st E-code: GoldDat, FDone, set DOUT19,39 Flags
2nd E-code: DoneData, low GoldDat, hi ~OWEN, kill DOUT19,39

~OWEN must be set LOW when data is at SELOUT
sync'd to REN/LREN for FW
sync'd to GoldDat for LW

~OWEN must be set LOW when data is at SELOUT
3 more words to FIFO after FF is set; use LEXT FIFO PAF to stop REN/OWEN!

Note that DONE means Last FIFO_REN is done!

Use as POP for FWFT FIFO?

Hold off this Reset until EndOfEvent

Indicates current REN'd Fiber memory synched with DoFW+1 synched to REN LREN[3:0]

The first GoodData comes at least 3 clocks AFTER the last DoHdr
Check for DMB Error Word and consistency:

Check consistency of the four "Special Word" bits:

2-logic-step delay synched w/GoodDat

Voted bits are not for FirstWord use

3 more words to FIFO after FF is set; use PAF to stop!

A FIFO ends at 1st false "LFIFO_EMPTY" after "LGoodLW"

"FDONE" indicates "LGoodLW" was received: waiting for the final NotEmpty word from FIFO

------> Switch FIFOs after next good word!

------> "RENOE-0" holds REN enabled until "FDONE" goes false

------> FIFODONE means the LastWord/LREN is on OUT[35:0], NextFiber is set

synched w/GoodDat+1 synched w/GoodDat+1 synched w/GoodDat+1 synched w/GoodDat+1

Page 21

Page 20

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Page 18
Permanent accumulation of valid DMB-path-Xmit errors

Watch for multiple XMIT errors on same path

FIFO Done Timeout: count to 10752, 132 usec=10625 is the worst case possible per FIFO?

12.5ns clock period here

Set to 18945 (~236 usec) for now

FirstWord bit15 Low or A,B,C,D,E,F code
Status Monitor

Pick 8 Status signals, include in DAQ HDR/TR
-create logic for OEHDR/TR and their format
Also set 4 FMM bits for each input channel

#Bits useful at EOE (for Used Memories in event? 22 bits)

12b HDR0TR[11:0] [EVT_CNT[11:0] BUF12 HDR0TR[11:0]]
12b HDR0TR[29:18] [EVT_CNT[23:12] BUF12 HDR0TR[29:18]]
4b HDR1TR[3:0] [DMBDAY
4b HDR1TR[6:4] [DMBCNT[2:0] BUF3 HDR1TR[6:4]]

1=alive, 0=killed

Killed Channels

HDR1TR[21:18] [DMBCNT[1:0] HDR1TR[21:18]]
4b HDR1TR[22:20] [DMBCNT[2:0] HDR1TR[22:20]]

Live Channels

HDR1TR[8:6] [DMBCNT[2:0] HDR1TR[8:6]]

SyncErr AND ~MemErr == Mult1Err

Including DLError, RxError, SpwdError

In Hdr/TR, removed from data---DDUctrl can detect...

"Hard Error"

Removed from Hdr/TR...DDUctrl detects easily...

"SCA_OVFL"

1-3-2007_14:23 RD_CTRL 5
hdr1tr[29:22] "C-Code-Stat"

Bring These Out

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1-3-2007_14:23 RD_CTRL 5

---DDUctrl detects easily...

"SCA_OVFL"

In Hdr/TR, removed from data---DDUctrl can detect...

"Hard Error"

removed from Hdr/TR...

synced to LLLLREN/OE_TR1, inc CritDataErr

Includes DLError, RxError, SpwdError

In Hdr/TR, removed from data---DDUctrl detects easily...

"Hard Error"

"Hard Error"...DDUctrl detects easily...

"SCA_OVFL"

SyncErr AND ~MemErr == Mult1Err

Includes DLError, RxError, SpwdError

In Hdr/TR, removed from data---DDUctrl detects easily...

"Gran Error"

removed from Hdr/TR...

synced to LLLLREN/OE_TR1, inc CritDataErr
H1: 0x/5T/NN,NNN/XXX/I.II/VK

H2: 0x/8000/0001/8000/HHHH

H3: 0x/LLLL/0000/ZZZZ/GGMY

T-2: 0x/8000/FFFF/8000/8000

T-1: 0x/SSSS,SSSS/QQQQ/PPPP

TR: 0x/A/WWW,WWW/RRRR/UUMK
Event START timeout 3.2usec: 128=1000/0000=0x80.
Calibration START timeout 6.4usec: 256=0x0100.
25ns clock period here

Page 22

set AF at Full-512 = 7680 events:
set FULL at 8192 events

SPS BXN cycle from 0 to 923: CLR after 923=0x39B.
Implement look-ahead logic: (like OEFIFO+1)

CB2RE

START_D

START_E

SKP_STF_THR

NEXT FIBER

LOOKAHEAD_RST

Next Fiber to READ

M32E5BUS

FD4CE

2.1-logic-step delay for NEXT_FIBER

FD32CE

1.4-logic-step delay

WRNEXT_Fx: Fiber is writing to next memory

FDCE

REN_Fx used to POP Fiber memory record

SR4CLE

2.4-logic-step delay

2.1-logic-step delay for OEFIFOx

OE's the correct memory for READ synched to FOE_REN

实施前瞻逻辑：（类似于 OEFIFO+1）

CB2RE

START_D

START_E

SKP_STF_THR

NEXT FIBER

LOOKAHEAD_RST

Next Fiber to READ

M32E5BUS

FD4CE

2.1-logic-step delay for NEXT_FIBER

FD32CE

1.4-logic-step delay

WRNEXT_Fx: Fiber is writing to next memory

FDCE

REN_Fx used to POP Fiber memory record

SR4CLE

2.4-logic-step delay

2.1-logic-step delay for OEFIFOx

OE's the correct memory for READ synched to FOE_REN
Access FIBEROK from JTAG as a fiber check.

---+ RESET required after fiber status change for now...

Change in FIBEROK is BAD! Set error code.

...notify FMM and maybe set STATUS bit, but...
data is OK until FIFO read time-out occurs.

...but how to know WHEN the bad-data comes out?

---+ timeout will probably occur for that event
DDU Input Controller Logic

Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits.

INT0

INT1

INT2

INT3

INT4

INT5

2ORMORE

2ORMORE
DDU Input Controller Logic

CMS CSC Electronics

Check for ALL bits set, ANY bits set and NOTALL bits set
O = NEXT_FIBER

X = ~WAIT

DODATA

FIFO

FOE

REN

TOGGLE

DMBDAY

[3:0]

DMBDAX

[3:0]

A

[3:0]

B

[3:0]

O

1234

115th October 2003

JRG
Custom Fast, Complex Logic for DDU, use 2 MUXCY as AND similar to: OR4 AND SOP4B2b

14th September 2004
DOWN = Decrement 1

Assume that CE includes DOWN+UP
the D byte goes out last (on \(C\) rising edge)
the F byte goes out first (on \(C\) falling edge)
the D byte goes out last (on C rising edge)
the F byte goes out first (on C falling edge)
Implements as a DPRAM (8 slices)
decode first 32 OpCodes (5 bits)

Glitch Protection for JRST function: must do NOOP after RESET!
10-bit JTAG Register Read out (on DVCENB)
12-bit JTAG Register Read out (on DVCENB)
16-bit JTAG Register Read out (on DVCENB)
DDU 24-bit JTAG Register Readout

DDU Input Controller Logic

CMS CSC Electronics
Check Status LOGIC (F3), shift test (F2)
FOK LED
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED
--LIT == Active Data Xmit
--OFF == No data to Xmit
VIRTEX Family Decode 32E Macro

5-bit to 32-bit Decoder
4-Bit Data Register w/ Clock Enable & Sync Reset, RPM coords X0Y0.

VIRTEX Family FD4RE Macro

RLOC=X0Y0

D0 CE C R
Q0

D1 CE C R
Q1

D2 CE C R
Q2

D3 CE C R
Q3

Title: VIRTEX Family FD4RE Macro
Comments: 4-Bit Data Register w/ Clock Enable & Sync Reset, RPM coords X0Y0.
Date: 4th November 2003
Rev: 1
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
4-to-1 Multiplexer with Enable

VIRTEX Family M4_1E_RPM Macro

Title:

Date: 31st October 2003

Ver: 1

Rev: B

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
Title: 9-bit MUX for 2 9-bit Inputs, w/Enable. RLOC=GRID

DDU Input Controller Logic

CMS CSC Electronics
18-bit MUX *DIAGONAL* for 4 18-bit Inputs, w/Enable

Virtex MUX logic

CMS CSC Electronics

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Q[17:9]

MUX4_9B_GV

Q[17:0]

CTRL1

CTRL0

I0BUS[8:0]

I1BUS[8:0]

I2BUS[8:0]

I3BUS[8:0]

Q[8:0]
9-bit MUX for 4 9-bit Inputs, w/Enable. RPM_GRID, Vertical.
Virtex MUX logic
CMS CSC Electronics
Shift Register w/ Enable and Async Clr

Q[0:3]

1234

drawn by KS

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VIRTEX Family SR4CE_R Macro

JRG

4-bit Serial-In Parallel-Out, REVERSED-ORDER on OUTPUT BUS!

Shift Register w/ Tiedie and Async Clr

3rd October 2003

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