In5Ctrl (file 0ddu_in) 1-3-2007_14:28

CMS CSC DDU5, Input Control FPGAs DF025A02 Version 25

Process Rocket I/O Data from DMB, format output to DDU FIFOs

v20: fix DMBfull-to-JTAG monitor logic
v21: add 2*32 bit Fiber Memory diagnostic (F30,31)
v22: replace F_OK with LFOK for InUnits;
r2, use FDP for LFOK; r3, use FOK to control GT PwrDn;
v23, RxErr sets SingleWarn, but LRxErr goes on Stat11, Lfilled on Stat30, LDLLerr on STAT31
v24: Tune RdBusy logic, extend RHL to 1200ns; r2: add Search/Free Errordetection to FMM & L1m2b7
r3: add REN-while-StackMT error to FMM & L1m2b7; r4: new LA signals on 2H
r5: try OEF_F/REN_F fix in RdCtrl.9, allows Fiber/NextMem bookeeping when FIFO Empty at EOE
r6: add mode 8-F options for LAs & LEDs; r7: add RstEOE to OEM_fctrl counter, bring BadFW to L0mA4
v25: RdCtrl.9 disable LnxtFIFO until NextFiber+6, prevents Previous fiber moving Current Read pointer
r2: Now SCAovfl (DMBerr) does Not set SingleError at InFPGA

this DDU:
RXER words are skipped, FILLER added as needed
- Use code "C" with FILL flag set (b34 & b16)
-- could use code "8" instead...
- Should we Reset RxErr Monitor? How?

PART=XC2VP20-6-FG676
AVOID=Y21, E23, C22, E21
(INIT, BUSY, WRITE, CS)
NC_XCV400_FG676=B13, AF13
NC_XCV400E_FG676=D13, Y13

All I/O is 3.3V

INCNTRL

Mode 1 Switch Block
1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
7: Set Fake_L1A (data passthrough)
8: Show STAT31-0 on LAs, ~FPGA version on LEDs

PROM=2*XC18V04-VQ44 (PARALLEL)
DDU5in\In5Ctrl\in5ctrl

* af_clb_5x31rpm has Core EDN file
PROGRAM takes < 55ms

VME Broadcast Addresses:
24=OSU-TCB "Test Control Board"
25=DMB
26=TMB
27=Both DMB and TMB
28=DDU
22=DCC

PromID: 05026093h
FPGAid: 31266093h

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174 WEST 18TH AVE
COLUMBUS OHIO 43210

To Do:
- COMPARE L1NUM & BXN (DMB/TMB too)
add BX_offset constants to SRAM?
- use DDU-DMB fiber to STOP DMB on FULL, check
- Watch for TRG buff overflows
- No logic for TXEN, TXDIN, PAE0/1, Mode5/4...OK.
- Add InUnit Check for DMB Timeouts & set FMM Error?

Special Startup Order:
2) Release WE
3) Release DLL
5) En. Outputs
6) DONE

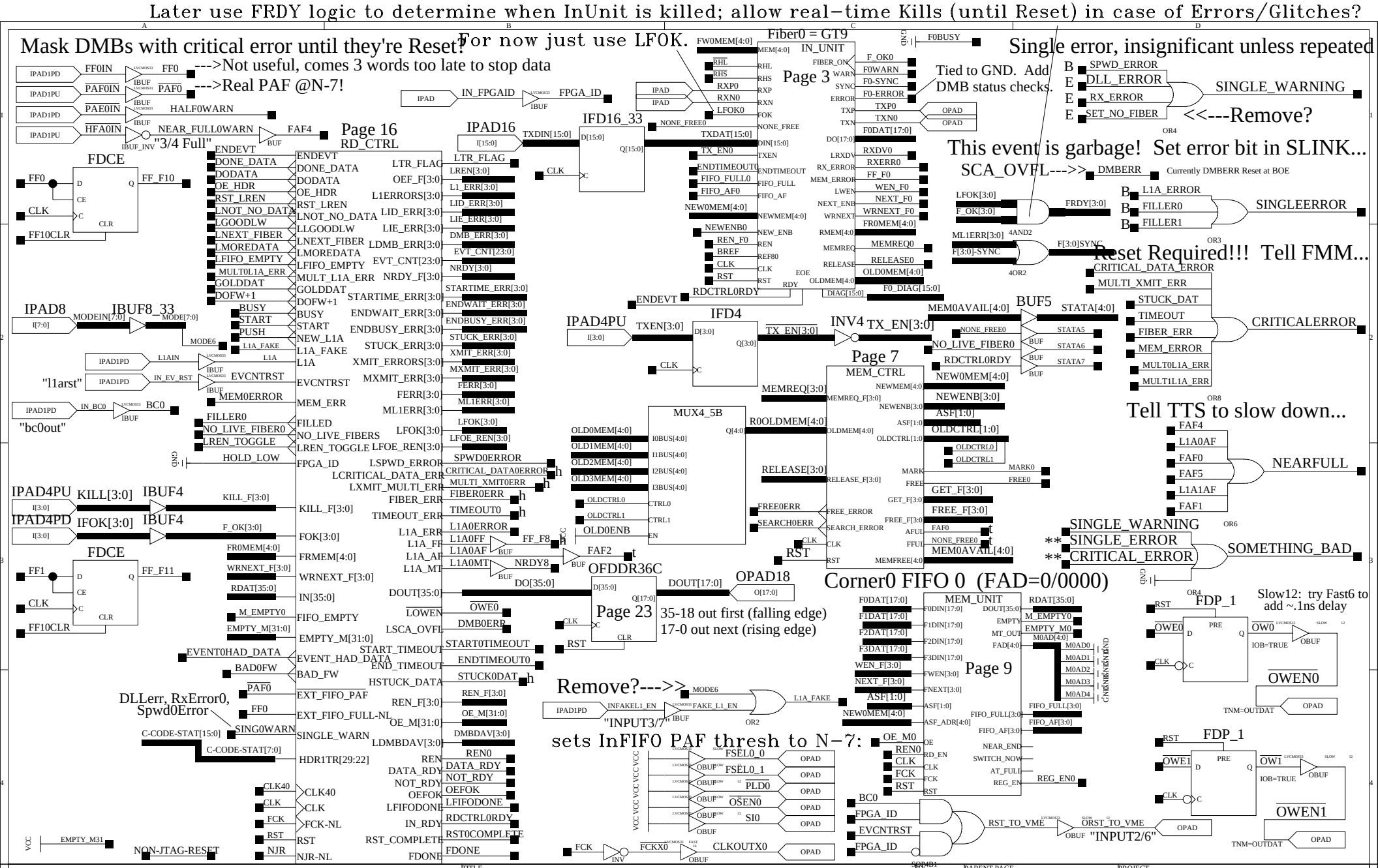
DDU Format Since DDUctrl v15:
H1: 0x/5T/NN.NNNN/XXX/I.II/VK (BOE1 type, L1A Number, BXN, ID, FOV, K-Status)
H2: 0x/8000/0001/8000/HHHH (49-bit ~unique constant, DMBfull(15))
H3: 0x/LLLL/oooo/ZZZZ/GGMY (LiveDMB(15), Ostat, DMB-DAV(15), BOEstat, DMBcnt)
T-2: 0x/8000/FFFF/8000/8000 (64-bit unique constant)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP (DDU EOE Status, DMBerr, DMBwarn(15))
TR: 0x/A/?/WW.WWWW/RRRR/UUMK (EOE, WordCount, CRCword, EOEstat, K-Status)

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount 8 TS assumed

mojo

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes

DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes


Later use FRDY logic to determine when InUnit is killed; allow real-time Kills (until Reset) in case of Errors/Glitches?
Mask DMBs with critical error until they're Reset?
For now just use LFOK.
Single error, insignificant unless repeated
Fiber0 = GT9
Page 3
Page 16
RD_CTRL
Page 7
Page 9
Page 23
Corner0 FIFO 0 (FAD=0/0000)
This event is garbage! Set error bit in SLINK...
Reset Required!!! Tell FMM...
Tell TTS to slow down...
Remove?--->>
sets InFIFO PAF thresh to N-7:
35-18 out first (falling edge)
17-0 out next (rising edge)
---->Not useful, comes 3 words too late to stop data
---->Real PAF @N-7!
"3/4 Full"
Tied to GND. Add DMB status checks.
<<---Remove?
SCA_OVFL--->>
Currently DMBERR Reset at BOE
"l1arst"
"bc0out"
DLLerr, RxError0, Spwd0Error
"INPUT3/7"
"INPUT2/6"
Slow12: try Fast6 to add ~.1ns delay
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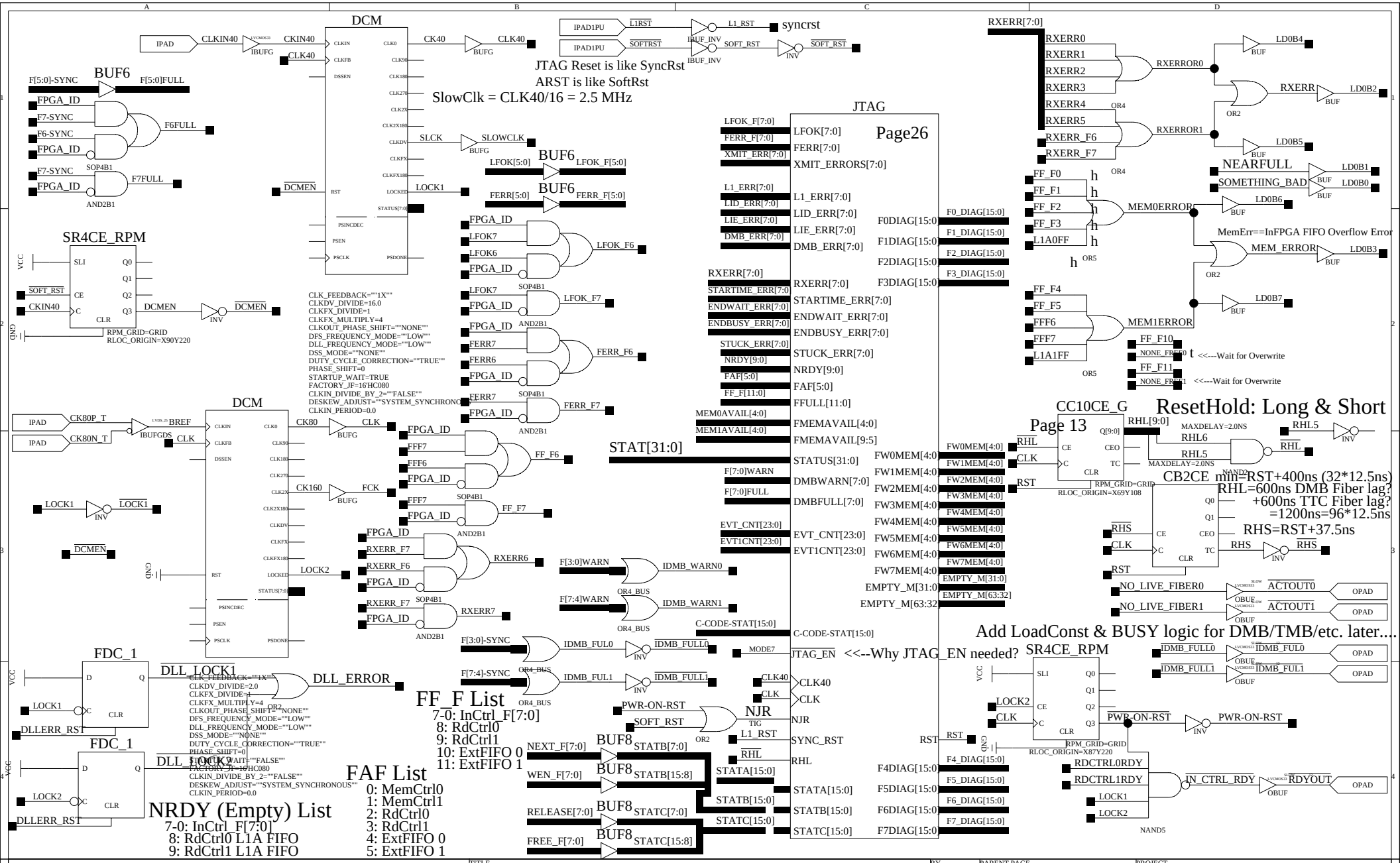
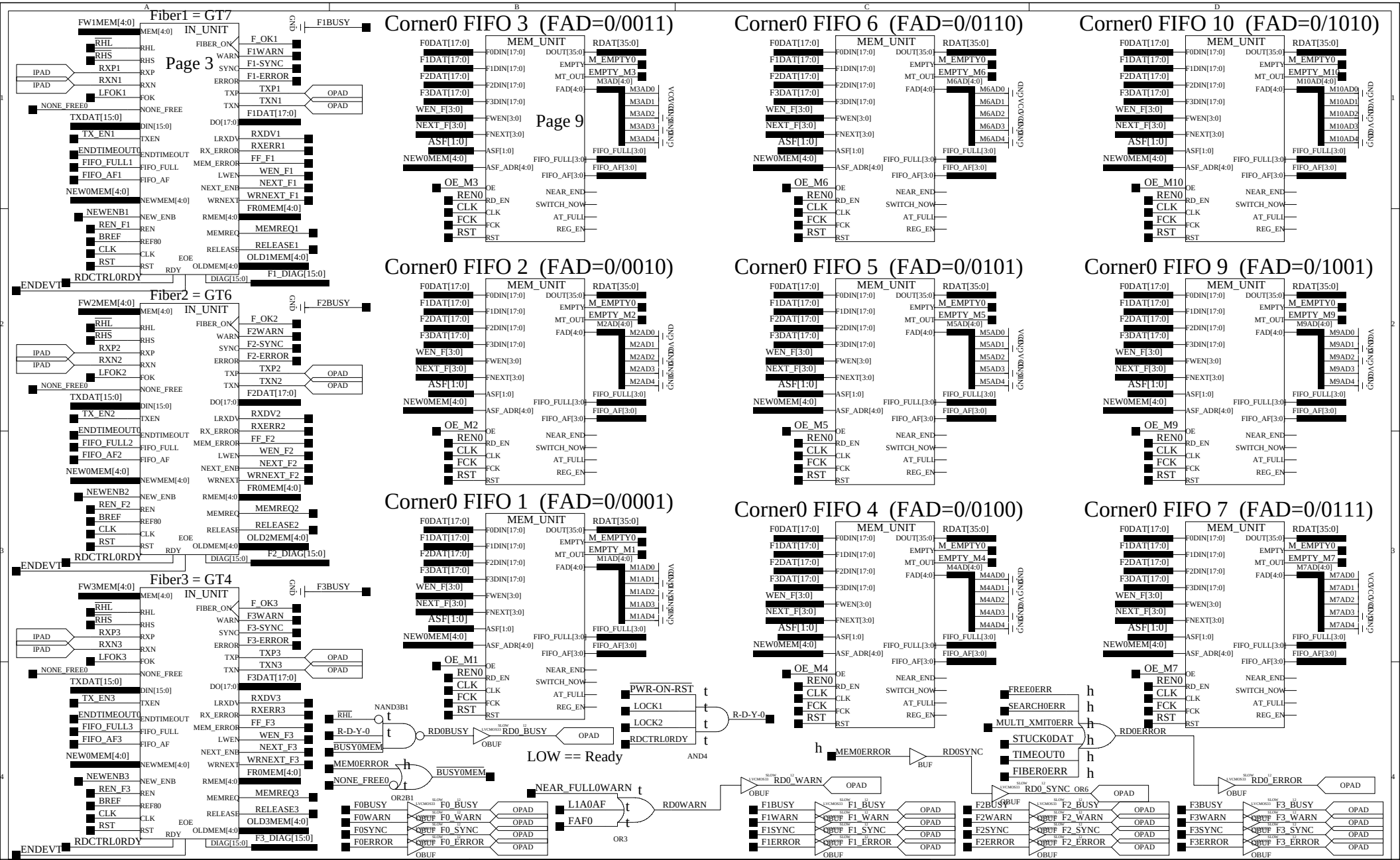
174 WEST 18TH AVE, COLUMBUS OH 43210
Input Control
DDU Input Controller Logic
CMS CSC Electronics
JRG
1-3-2007_14:25
D785D
INCNTRL . 1
2

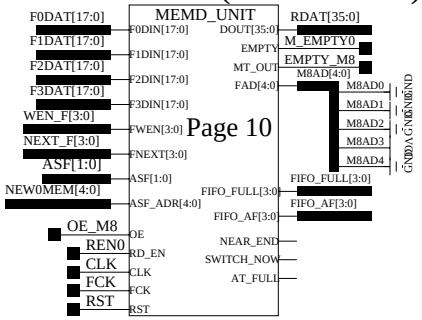


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 11-20-2006_17:24	PARENT PAGE: 1 FILE: INCNTRL . 2	PROJECT: D785D PAGE: 2A

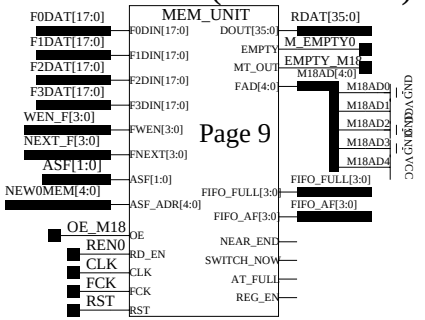


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Input Control DDU Input Controller Logic CMS CSC Electronics	BY JRG DATE 11-15-2006_15:57	PARENT PAGE 1 FILE INCNTRL . 3
		PROJECT D785D	PAGE 2B

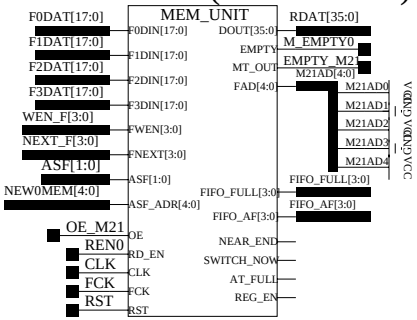
Corner0 FIFO 8* (FAD=0/1000)



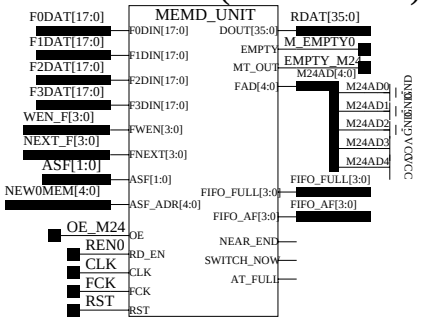
Corner1 FIFO 2 (FAD=1/0010)



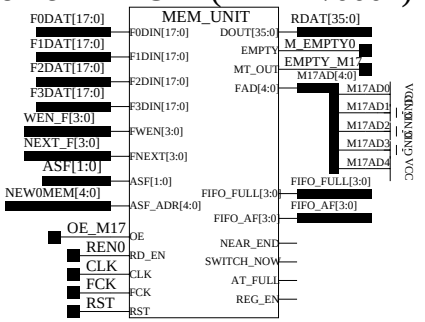
Corner1 FIFO 5 (FAD=1/0101)



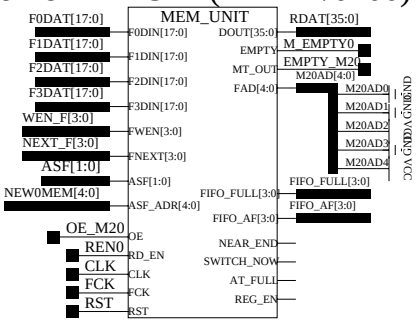
Corner1 FIFO 8* (FAD=1/1000)



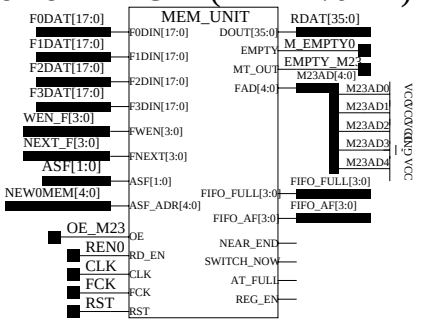
Corner1 FIFO 1 (FAD=1/0001)



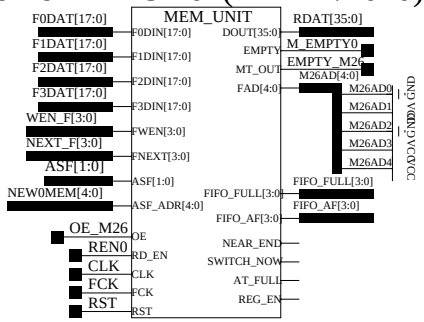
Corner1 FIFO 4 (FAD=1/0100)



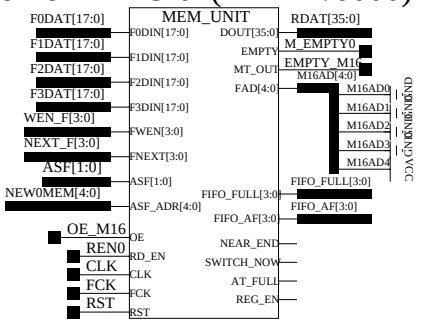
Corner1 FIFO 7 (FAD=1/0111)



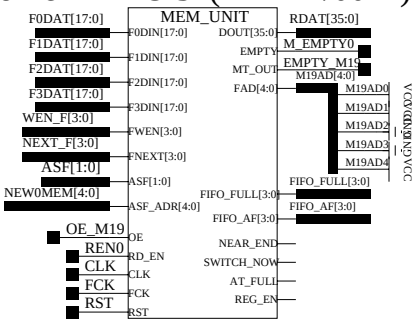
Corner1 FIFO 10 (FAD=1/1010)



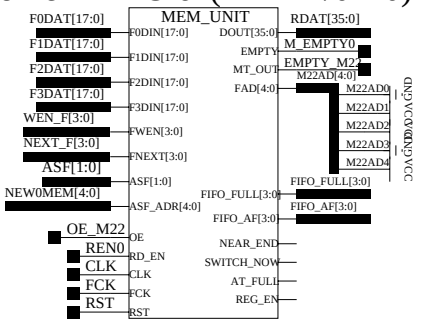
Corner1 FIFO 0 (FAD=1/0000)



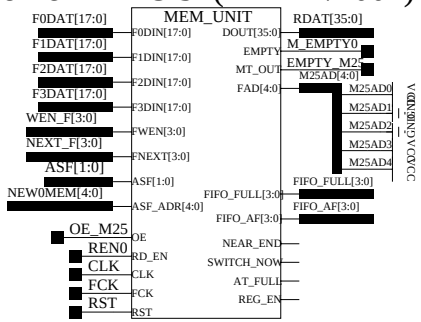
Corner1 FIFO 3 (FAD=1/0011)



Corner1 FIFO 6 (FAD=1/0110)



Corner1 FIFO 9 (FAD=1/1001)



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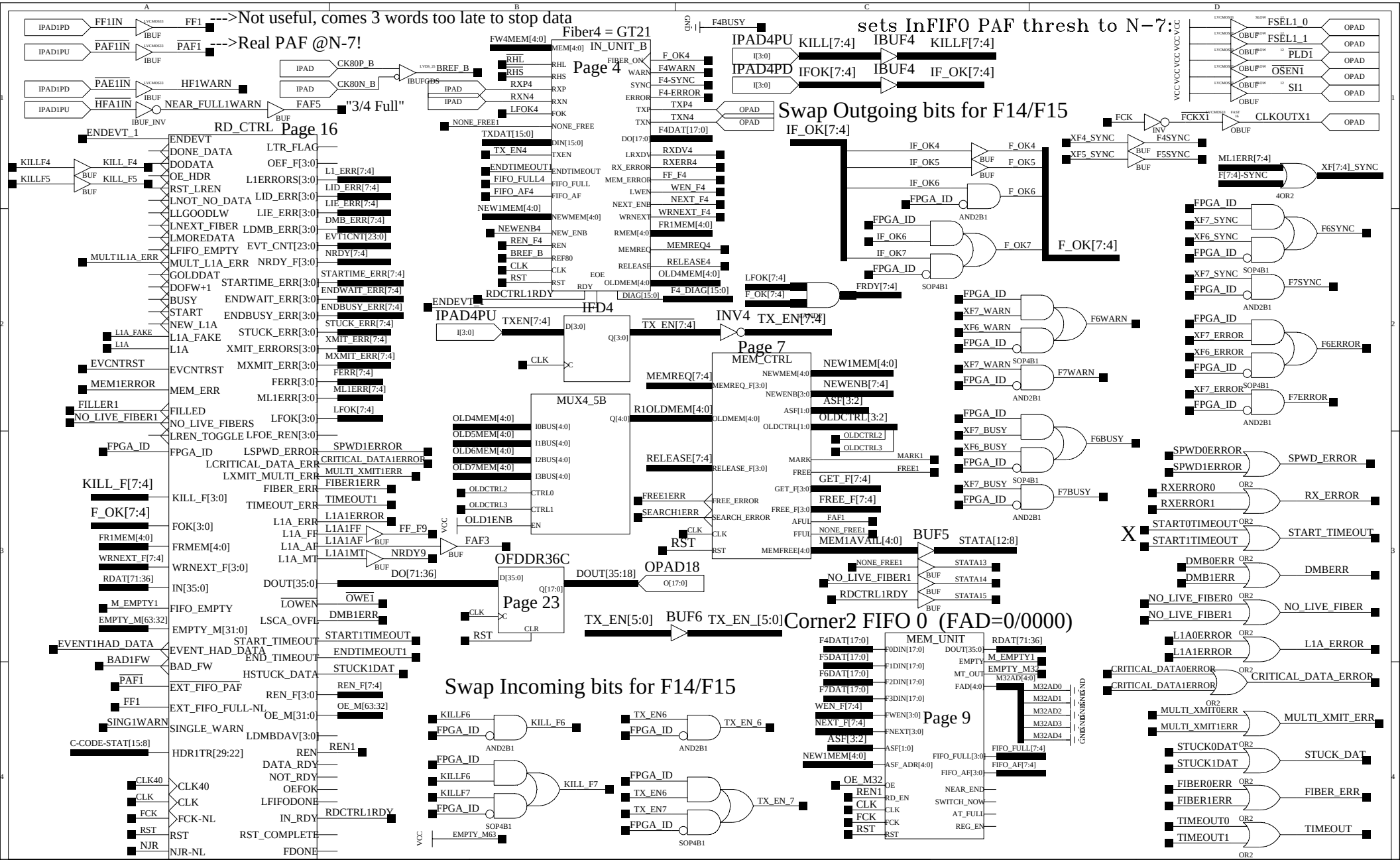
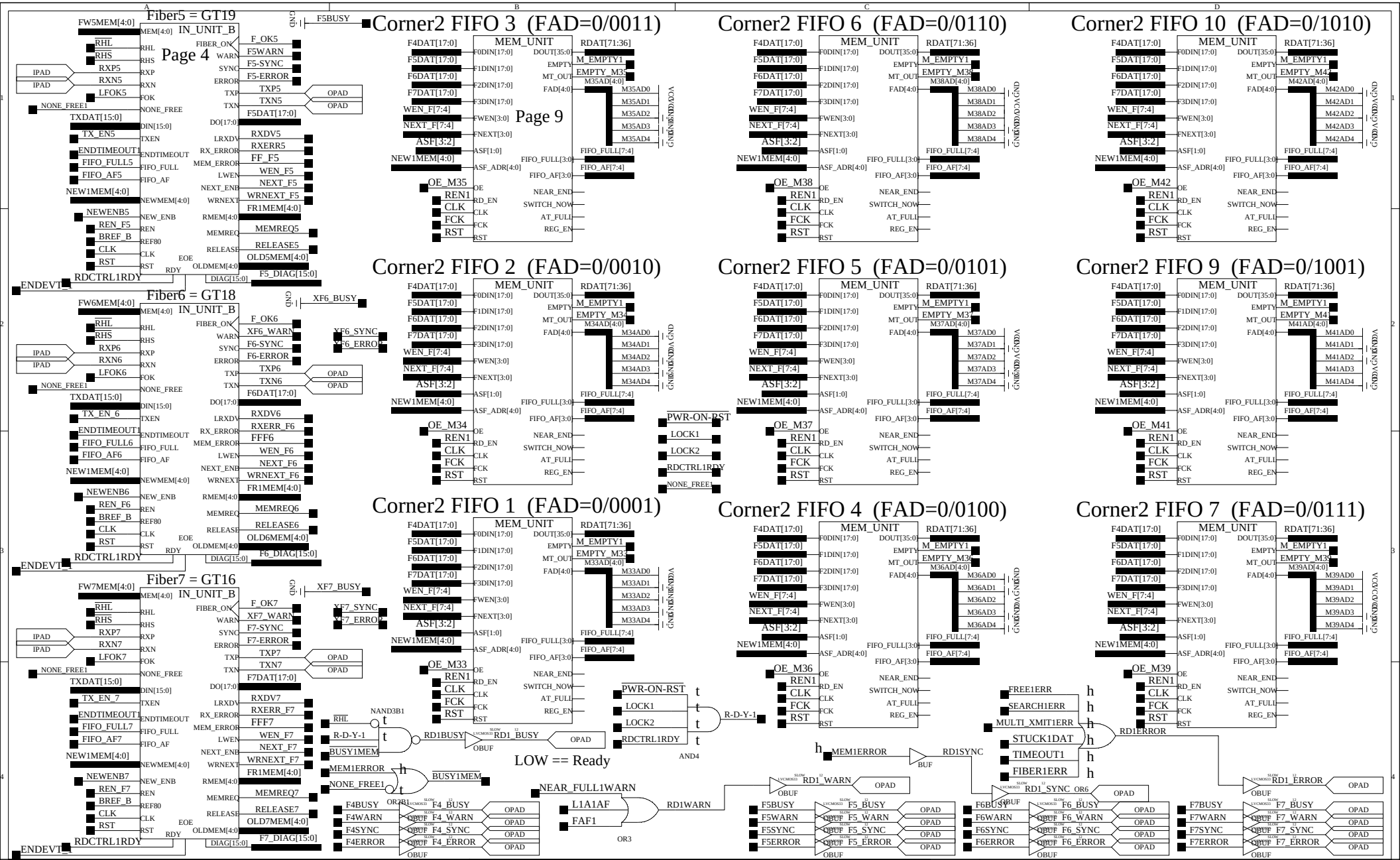
TITLE: Input Control
DDU Input Controller Logic
CMS CSC Electronics

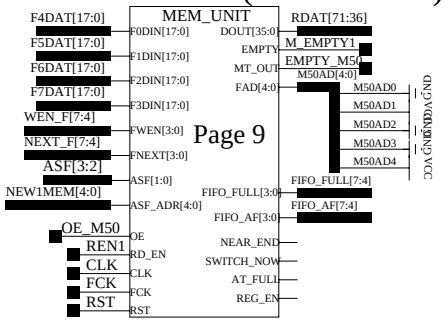
BY	PARENT PAGE	PROJECT
JRG	1	D785D
DATE	FILE	PAGE
7-18-2005_14:34	INCNTRL . 4	2C


--->Not useful, comes 3 words too late to stop data
--->Real PAF @N-7!
sets InFIFO PAF thresh to N-7:
Fiber4 = GT21
Page 4
Swap Outgoing bits for F14/15
RD_CTRL
Page 16
"3/4 Full"
IFD4
INV4
Page 7
MEM_CTRL
MUX4_5B
OFDDR36C
Page 23
Corner2 FIFO 0 (FAD=0/0000)
MEM_UNIT
Page 9
Swap Incoming bits for F14/15
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
Input Control
DDU Input Controller Logic
CMS CSC Electronics
JRG
1
D785D
11-22-2006_15:48
INCNTRL . 5
2D

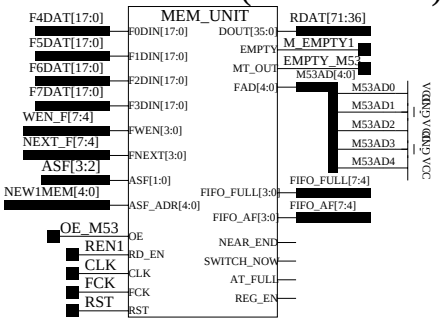


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Input Control DDU Input Controller Logic CMS CSC Electronics	BY JRG DATE 11-15-2006_15:57	PARENT PAGE 1 FILE INCNTRL . 6
		PROJECT D785D PAGE 2E	

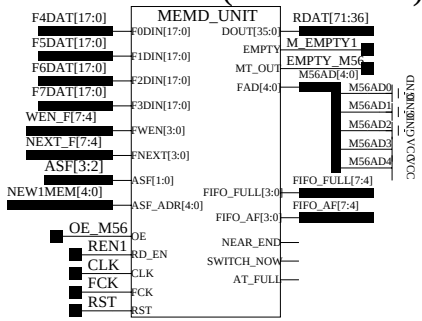
Corner3 FIFO 2 (FAD=1/0010)



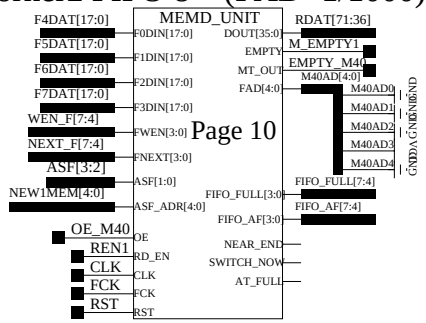
Corner3 FIFO 5 (FAD=1/0101)



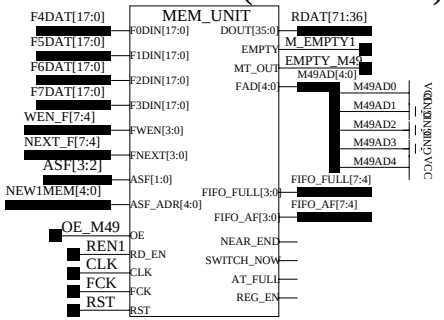
Corner3 FIFO 8* (FAD=1/1000)



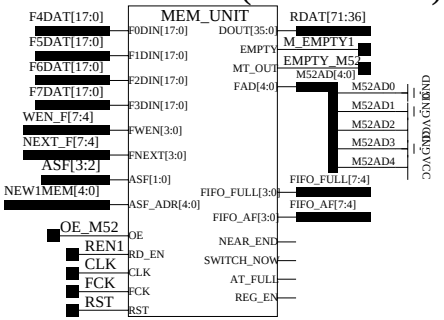
Corner2 FIFO 8* (FAD=1/1000)



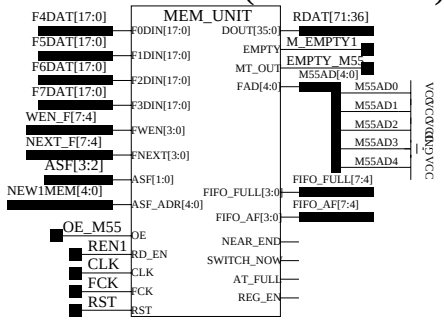
Corner3 FIFO 1 (FAD=1/0001)



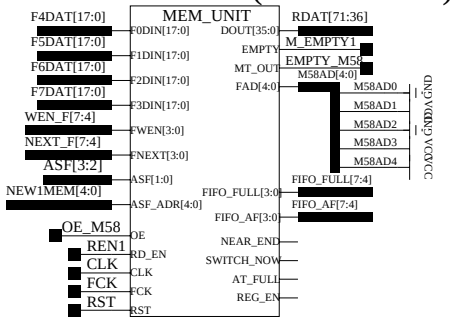
Corner3 FIFO 4 (FAD=1/0100)



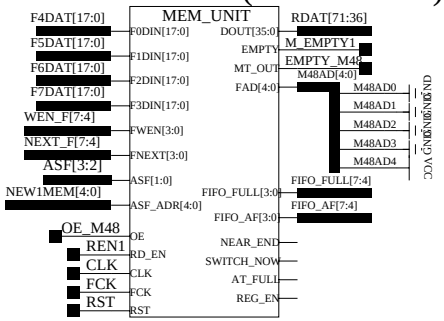
Corner3 FIFO 7 (FAD=1/0111)



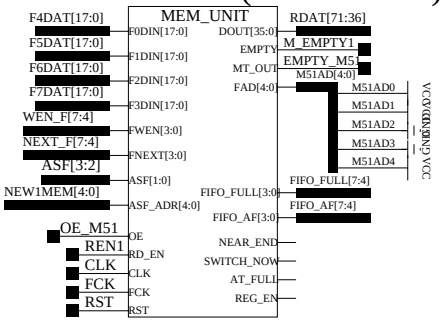
Corner3 FIFO 10 (FAD=1/1010)



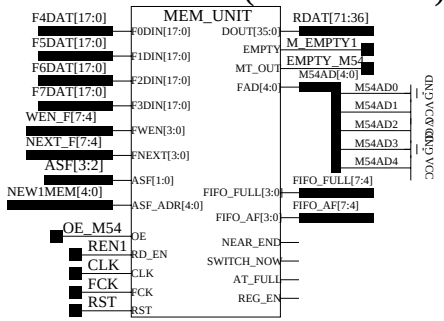
Corner3 FIFO 0 (FAD=1/0000)



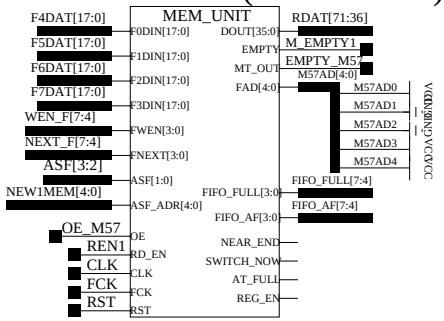
Corner3 FIFO 3 (FAD=1/0011)



Corner3 FIFO 6 (FAD=1/0110)



Corner3 FIFO 9 (FAD=1/1001)



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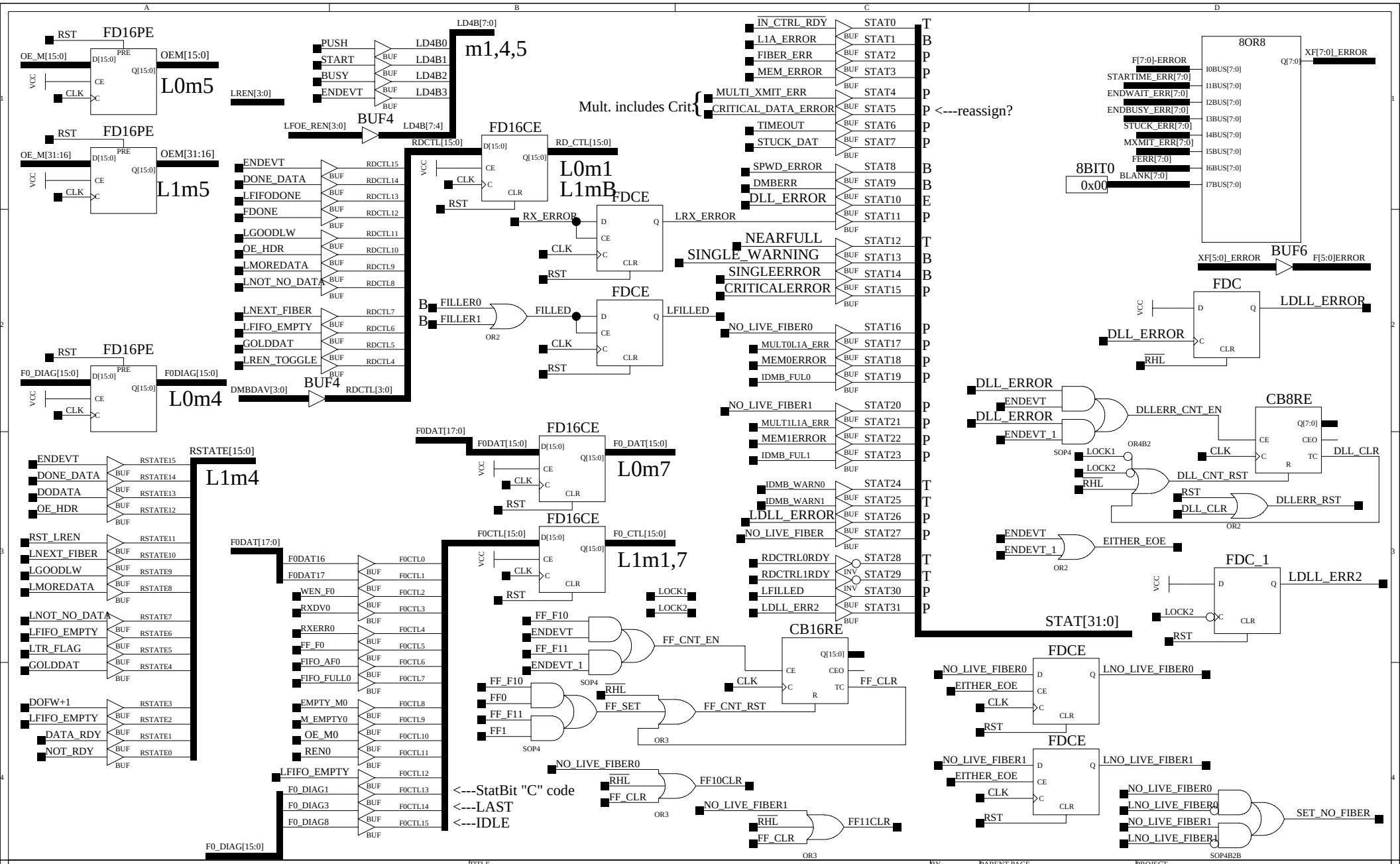
TITLE: Input Control
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	1	D785D
DATE	FILE	PAGE
7-18-2005_14:39	INCNTRL . 7	2F



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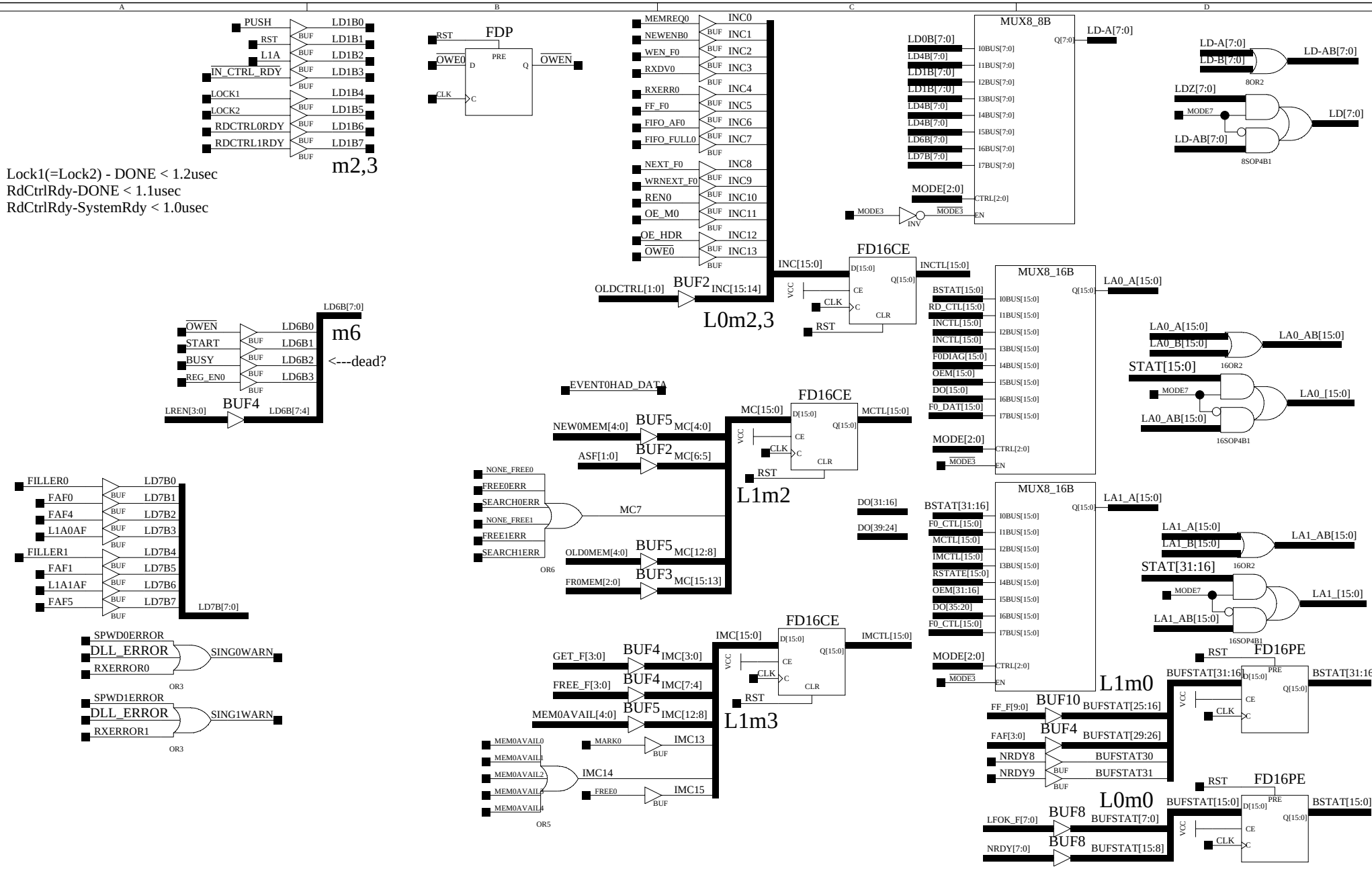
		DATE: 11-20-2006_15:38	FILE: INCNTRL . 8	PAGE: 2G



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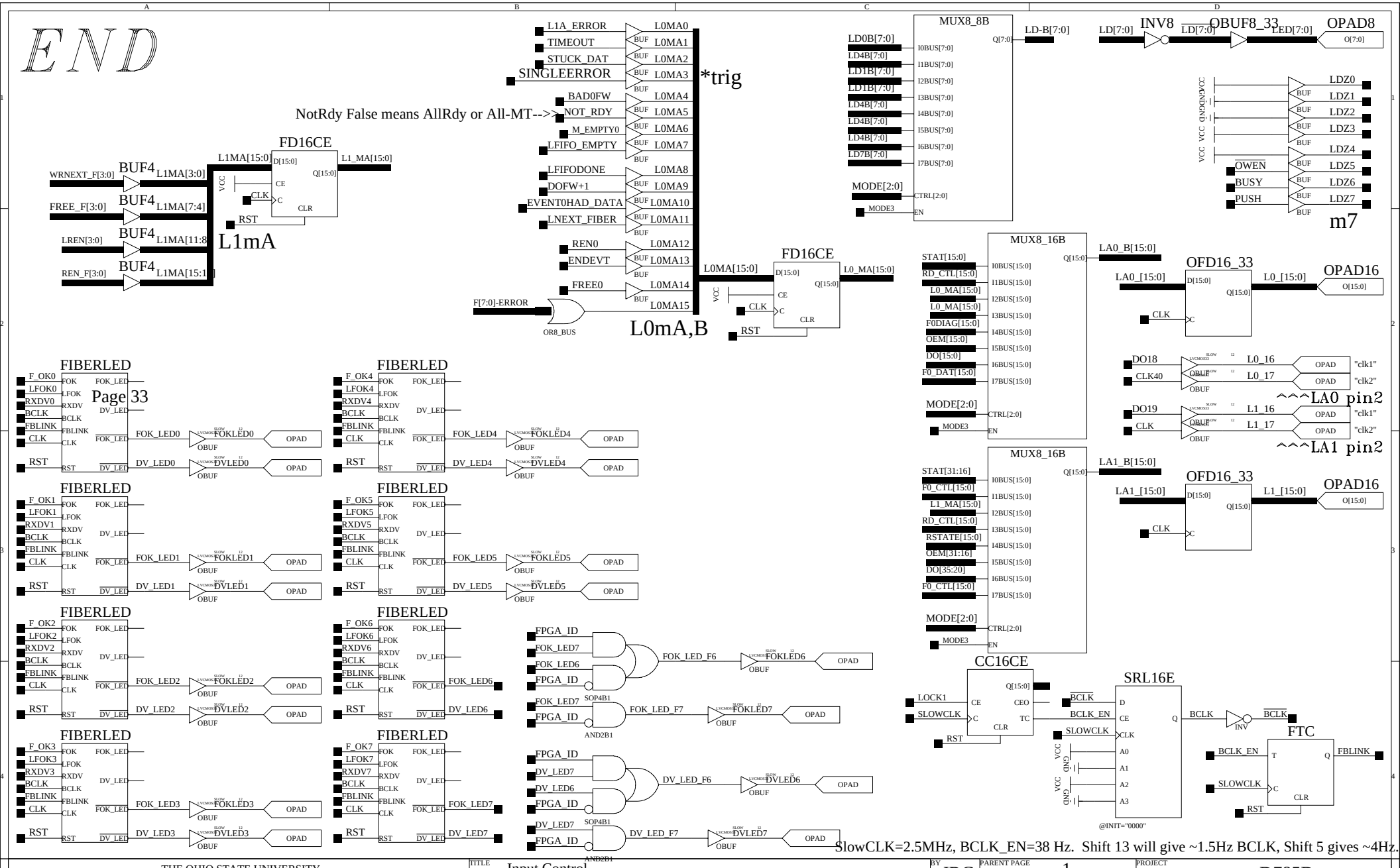
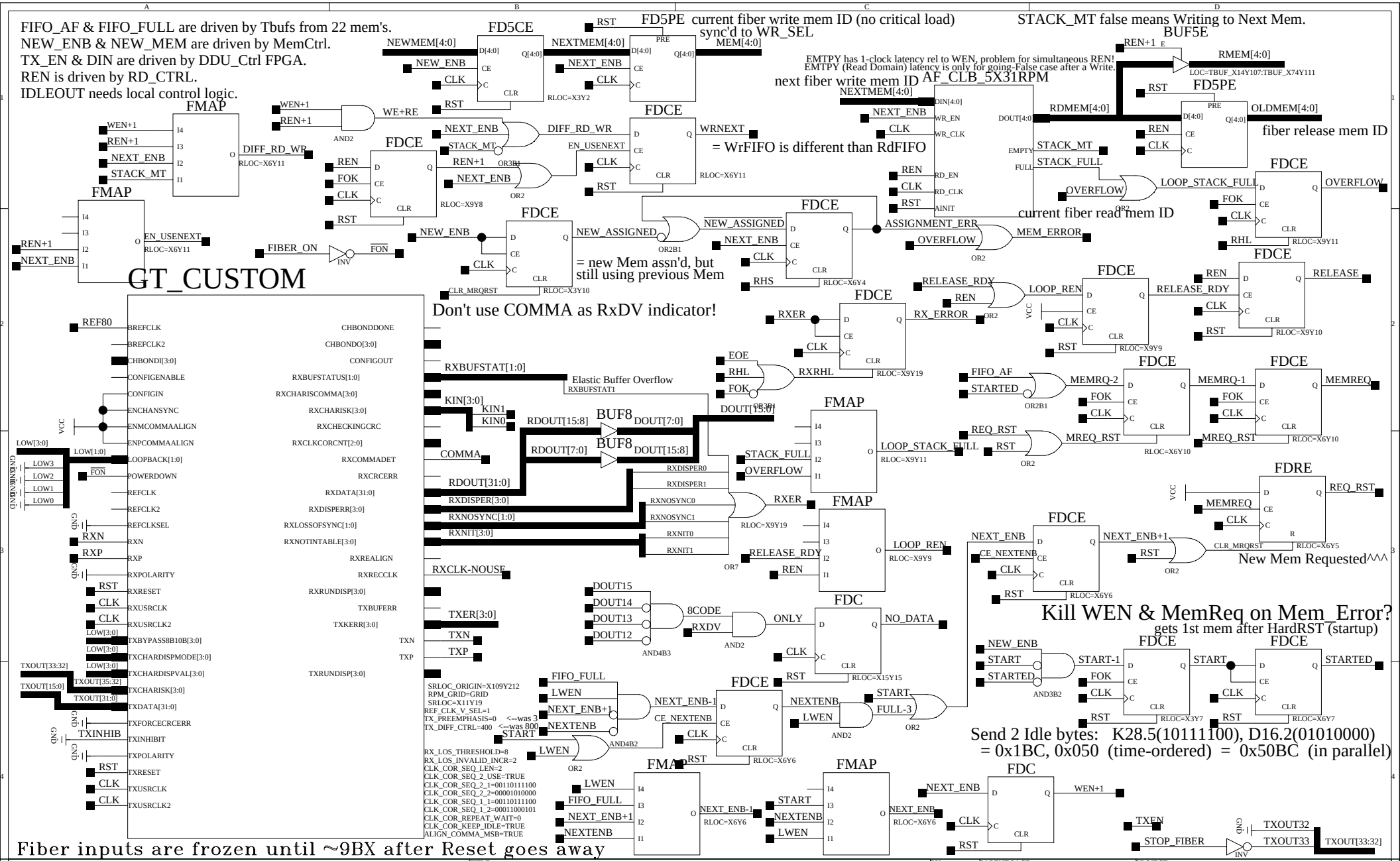
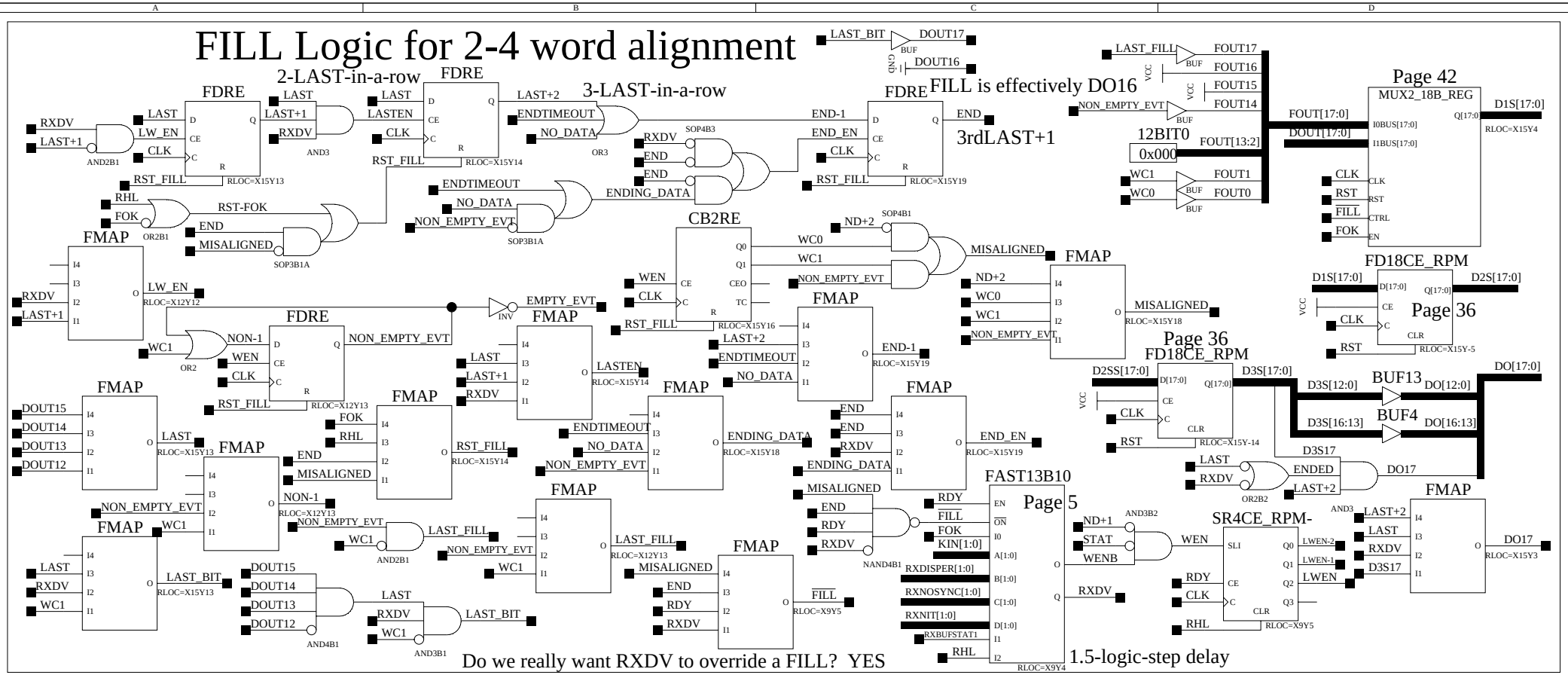
		DATE 11-22-2006_15:48	FILE INCNTRL . 9	PAGE 2H

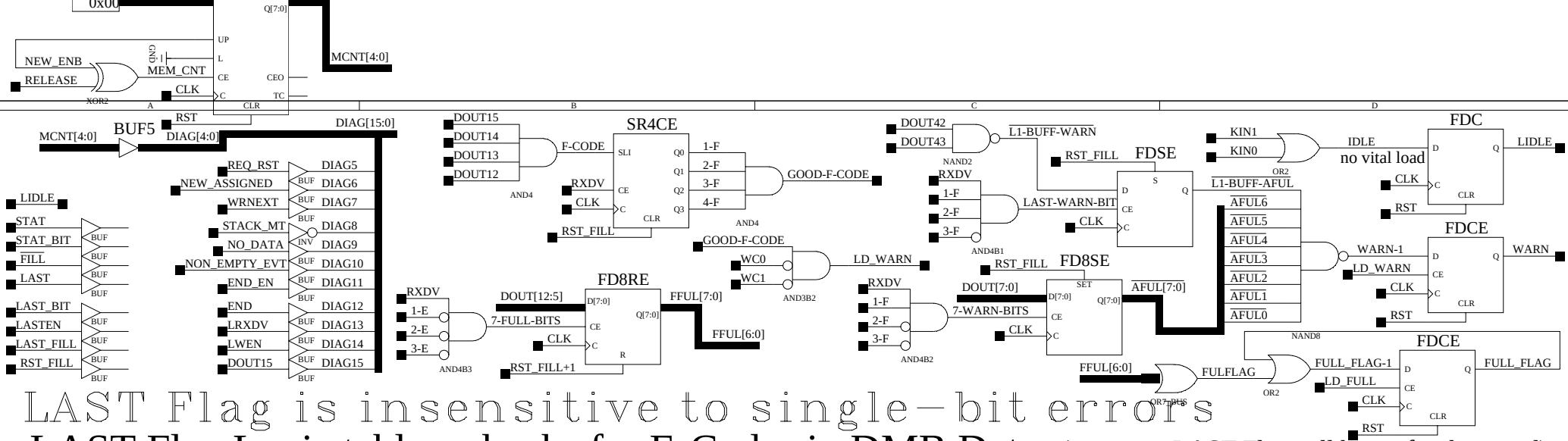

END
NotRdy False means AllRdy or All-MT-->>
FD16CE
L1mA
L1MA[15:0]
L1MA[3:0]
L1MA[7:4]
L1MA[11:8]
L1MA[15:12]
WRNEXT_F[3:0]
FREE_F[3:0]
LREN[3:0]
REN_F[3:0]
BUF4
L1_MA[15:0]
L1A_ERROR
TIMEOUT
STUCK_DAT
SINGLEERROR
BAD0FW
NOT_RDY
M_EMPTY0
LFIFO_EMPTY
LFIFODONE
DOFW+1
EVENT0HAD_DATA
LNEXT_FIBER
REN0
ENDEVT
FREE0
F[7:0]-ERROR
OR8_BUS
L0MA0
L0MA1
L0MA2
L0MA3
L0MA4
L0MA5
L0MA6
L0MA7
L0MA8
L0MA9
L0MA10
L0MA11
L0MA12
L0MA13
L0MA14
L0MA15
*trig
L0mA,B
L0MA[15:0]
L0_MA[15:0]
MUX8_8B
LD0B[7:0]
LD4B[7:0]
LD1B[7:0]
LD7B[7:0]
MODE[2:0]
LD-B[7:0]
LD[7:0]
INV8
OBUF8_33
OPAD8
LED[7:0]
LDZ0
LDZ1
LDZ2
LDZ3
LDZ4
LDZ5
LDZ6
LDZ7
OWEN
BUSY
PUSH
m7
MUX8_16B
STAT[15:0]
RD_CTL[15:0]
F0DIAG[15:0]
OEM[15:0]
DO[15:0]
F0_DAT[15:0]
LA0_B[15:0]
LA0_[15:0]
OFD16_33
OPAD16
L0_[15:0]
DO18
CLK40
L0_16
L0_17
LA0 pin2
DO19
L1_16
L1_17
LA1 pin2
STAT[31:16]
F0_CTL[15:0]
L1_MA[15:0]
RSTATE[15:0]
OEM[31:16]
DO[35:20]
LA1_B[15:0]
LA1_[15:0]
L1_[15:0]
CC16CE
LOCK1
SLOWCLK
SRL16E
BCLK
BCLK_EN
INV
FTC
FBLINK
@INIT="0000"
FIBERLED
Page 33
F_OK0
LFOK0
RXDV0
BCLK
FBLINK
CLK
RST
FOK
LFOK
RXDV
DV_LED
FOK_LED0
DV_LED0
FOKLED0
DVLED0
OBUF
OPAD
F_OK4
LFOK4
RXDV4
FOK_LED4
DV_LED4
FOKLED4
DVLED4
F_OK1
LFOK1
RXDV1
FOK_LED1
DV_LED1
FOKLED1
DVLED1
F_OK5
LFOK5
RXDV5
FOK_LED5
DV_LED5
FOKLED5
DVLED5
F_OK2
LFOK2
RXDV2
FOK_LED2
DV_LED2
FOKLED2
DVLED2
F_OK6
LFOK6
RXDV6
FOK_LED6
DV_LED6
FOKLED6
DVLED6
F_OK3
LFOK3
RXDV3
FOK_LED3
DV_LED3
FOKLED3
DVLED3
F_OK7
LFOK7
RXDV7
FOK_LED7
DV_LED7
FOKLED7
DVLED7
FPGA_ID
FOK_LED_F6
FOK_LED_F7
DV_LED_F6
DV_LED_F7
SOP4B1
AND2B1
SlowCLK=2.5MHz, BCLK_EN=38 Hz. Shift 13 will give ~1.5Hz BCLK, Shift 5 gives ~4Hz.
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
Input Control
DDU Input Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
1
PROJECT
D785D
DATE
11-27-2006_9:42
FILE
INCNTRL . 10
PAGE
2I



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Input Unit DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785D
		DATE 3-28-2007_13:42	FILE IN_UNIT . 1	PAGE 3



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Input Unit DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785D	
		DATE 11-15-2006_15:50		FILE IN_UNIT . 2	PAGE 3A



LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data (L means LAST Flag will be set for that word)

Assume 4 E-Codes at DMB End are sequential with no gaps

BRAM FIFO Output

Normal event sync:	X	X
	X	X
	E_L	E
	E	E

Normal, but lose 1st E-Word: (or lose last E-Word)	X	X
	X	X
	E_L	E_L
	Fill	E

Normal, but lose 2nd E-Word: (or lose 3rd E-Word)	X	X
	X	X
	E_L	E
	Fill	E

Normal, but BAD 1st E-Code:	X	X
	X	X
	E_L	X
	E	E

Normal, but BAD 2nd E-Code:	X	X
	X	X
	X_L	E
	E	E

BAD 3rd or 4th E-Code is no problem

Lost 1 word OR 3 extra:

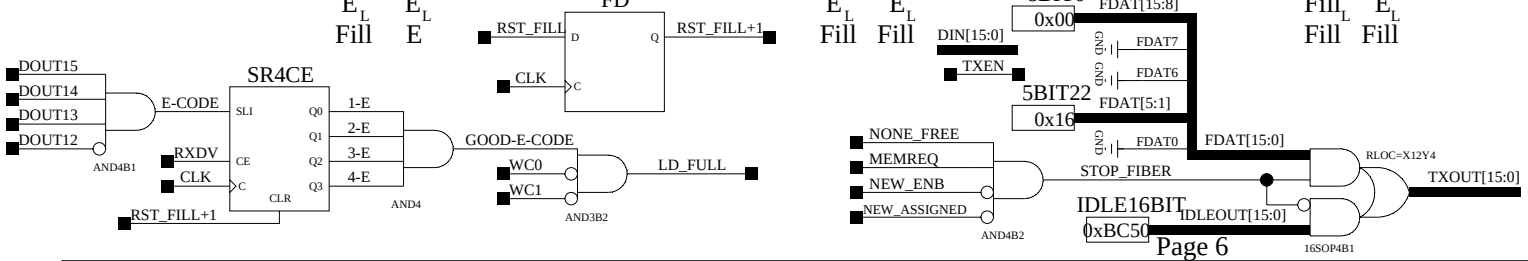
X	X
E	X
E_L	E_L
Fill	E

Lost 2 words OR 2 extra:

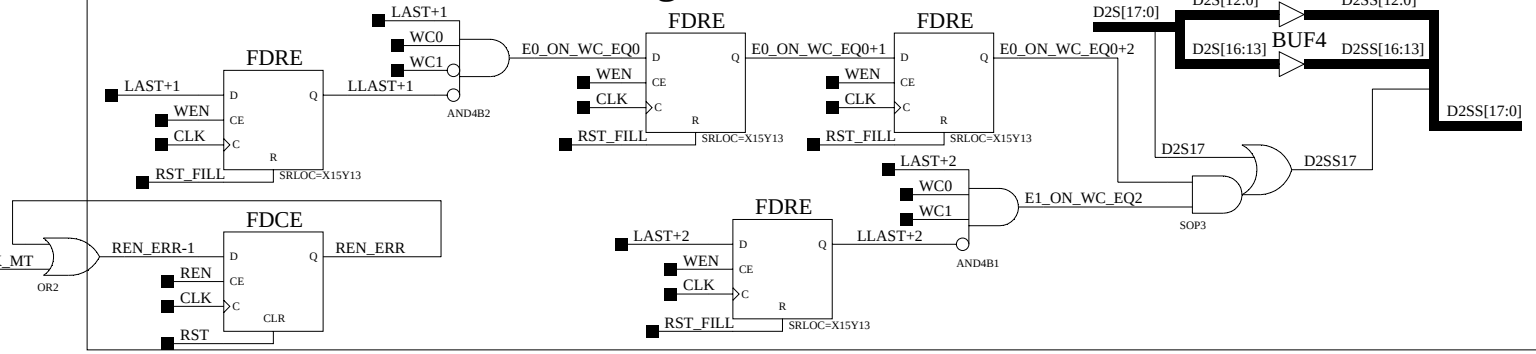
X	X
E	E
E_L	E_L
Fill	Fill

Lost 3 words OR 1 extra:

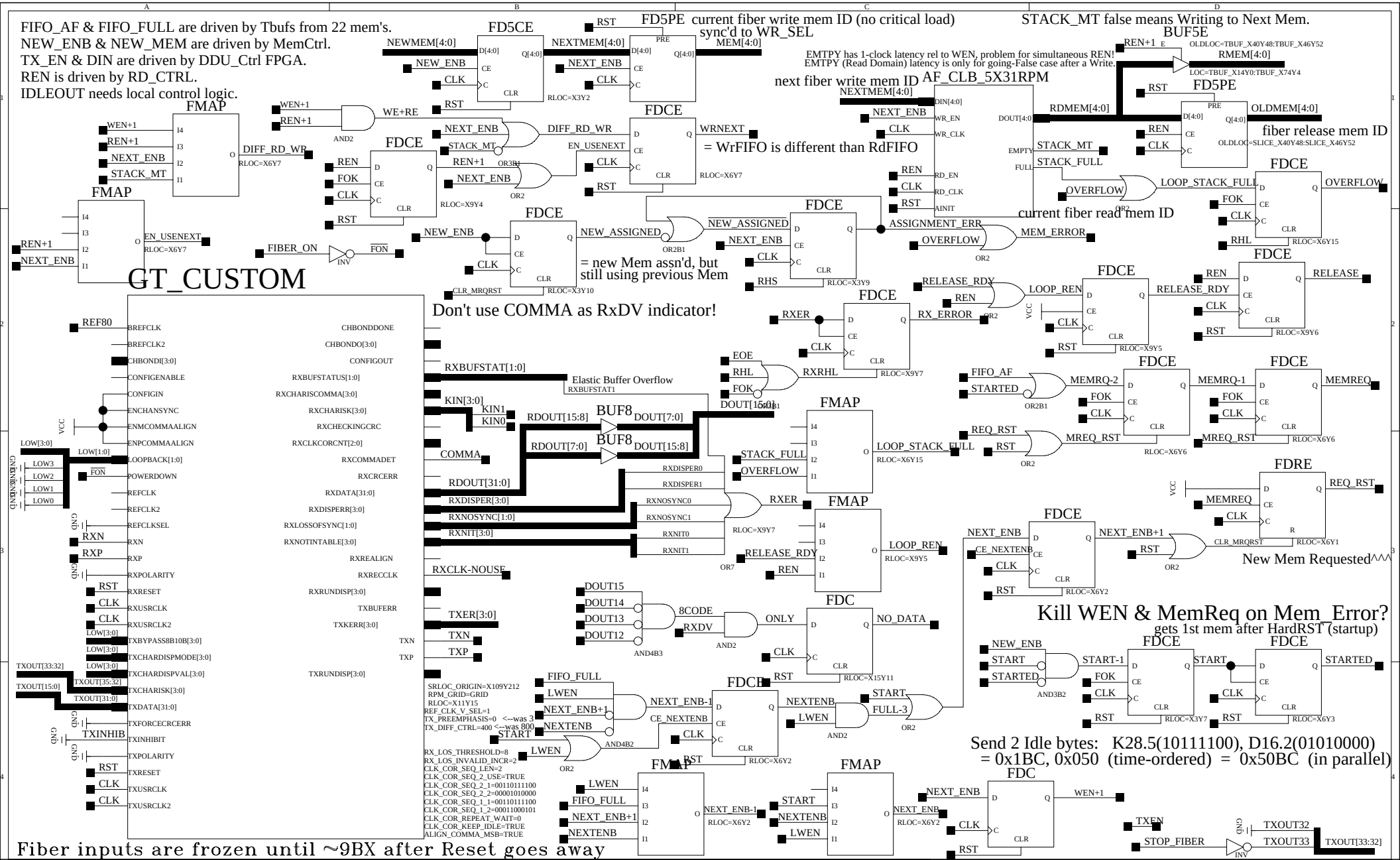
E	X
E	E
$Fill_L$	E_L
Fill	Fill



Set LAST Flag for Bad 2nd E-Code case

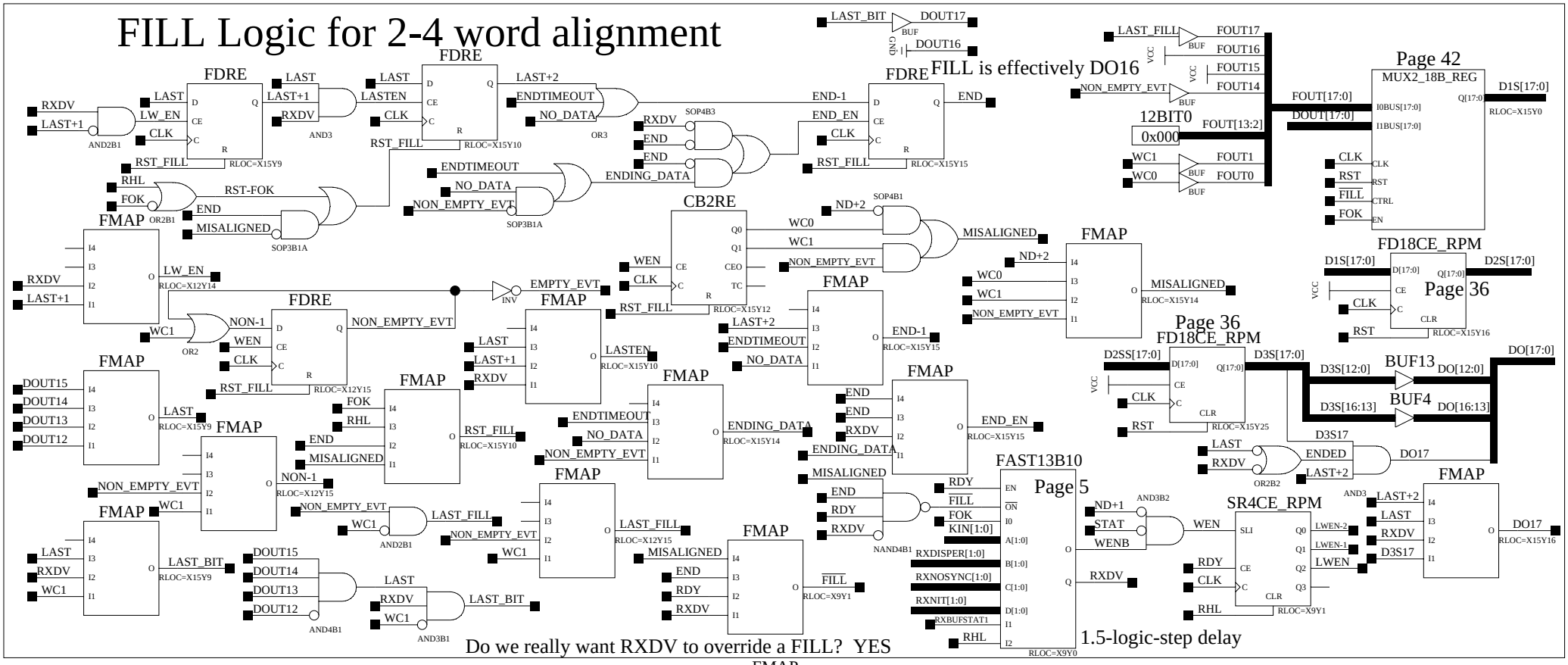


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Input Unit DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785D
		DATE 11-15-2006_15:50	FILE IN_UNIT . 3	PAGE 3B



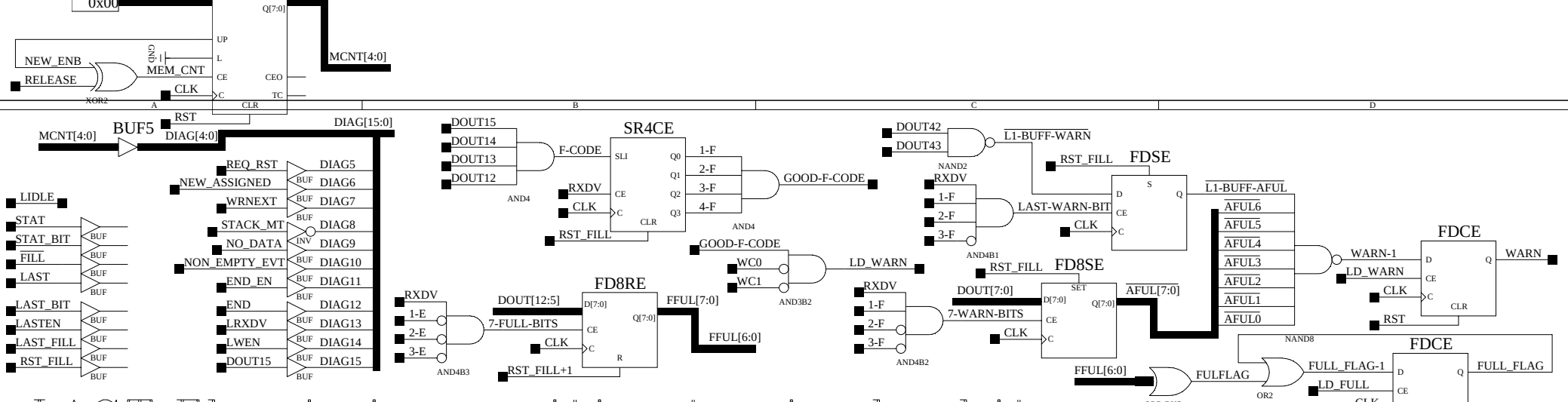
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input Unit DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2D	PROJECT: D785D
		DATE: 3-28-2007_13:43	FILE: IN_UNIT_B . 1	PAGE: 4

FILL Logic for 2-4 word alignment



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE	Input Unit DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2D
		DATE: 11-15-2006_15:51	PROJECT: D785D
		FILE: IN_UNIT_B . 2	PAGE: 4A



LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data (L means LAST Flag will be set for that word)

BRAM FIFO Output

Assume 4 E-Codes at DMB End are sequential with no gaps

Normal event sync:	X	X
	X	X
	E_L	E
	E	E

Normal, but lose 1st E-Word:	X	X
(or lose last E-Word)	X	X
	E_L	E_L
	Fill	E

Normal, but lose 2nd E-Word:	X	X
(or lose 3rd E-Word)	X	X
	E_L	E
	Fill	E

Normal, but BAD 1st E-Code:	X	X
	X	X
	E_L	X
	E	E

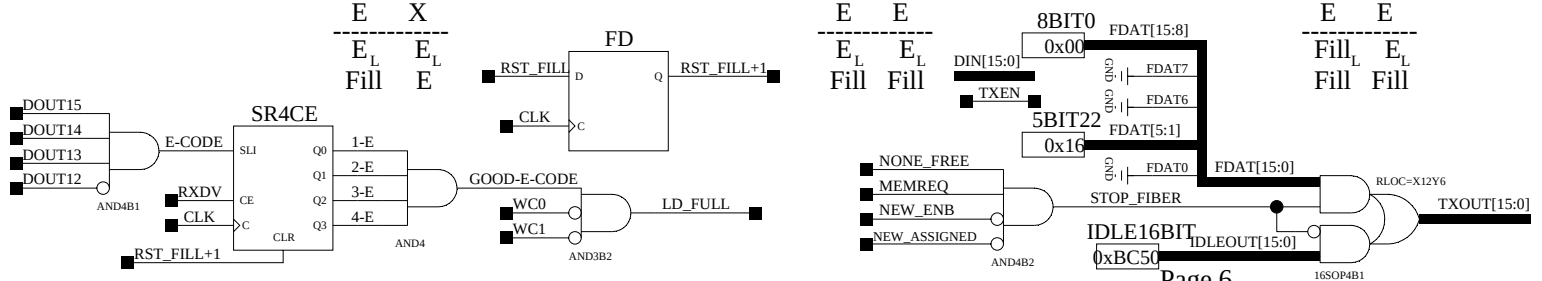
Normal, but BAD 2nd E-Code:	X	X
	X	X
	X_L	E
	E	E

BAD 3rd or 4th E-Code is no problem

Lost 1 word OR 3 extra:	X	X
	E	X
	E_L	E_L
	Fill	E

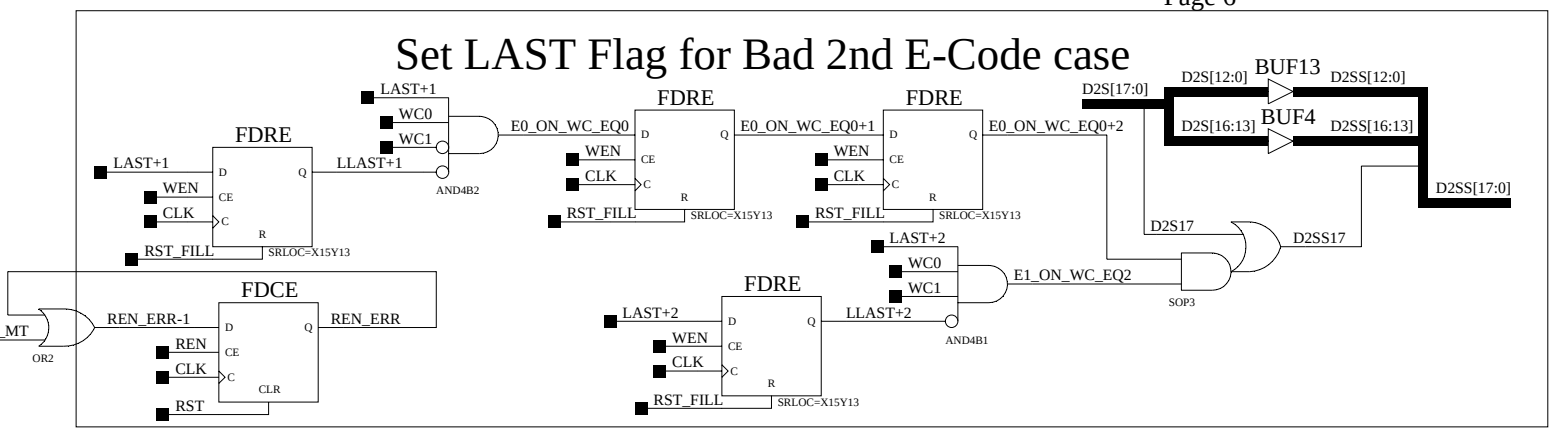
Lost 2 words OR 2 extra:	X	X
	E	E
	E_L	E_L
	Fill	Fill

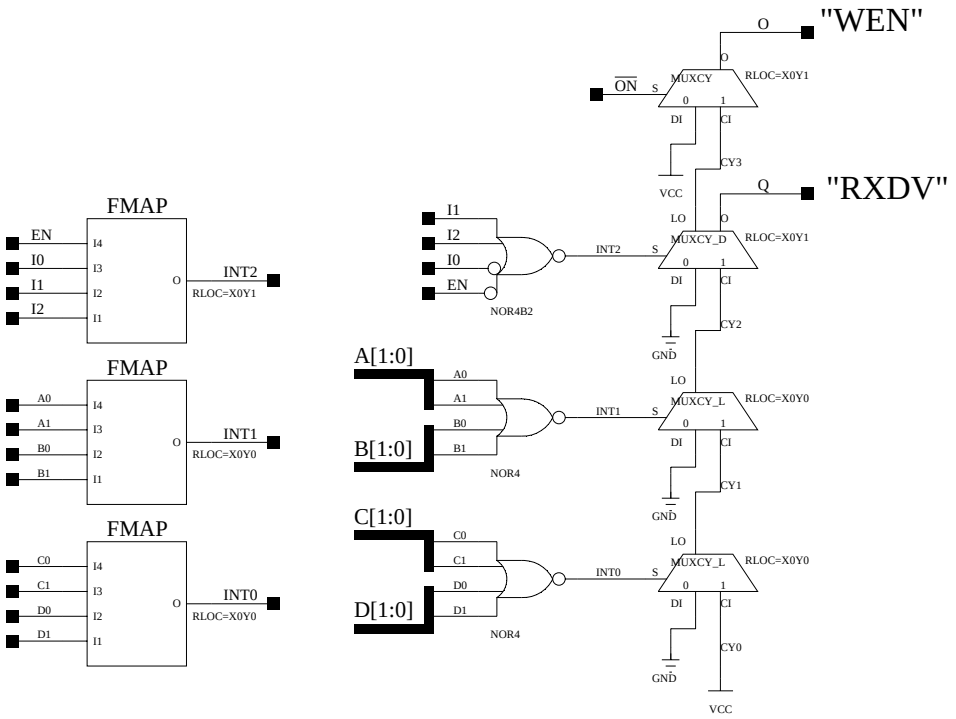
Lost 3 words OR 1 extra:	E	X
	E	E
	$Fill_L$	E_L
	Fill	Fill



Page 6

Set LAST Flag for Bad 2nd E-Code case





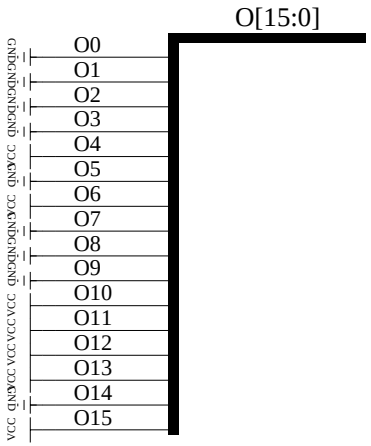
XILINX			JRG
Title:	FAST13B10		
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)

= 0x1BC + 0x050 (time-ordered)

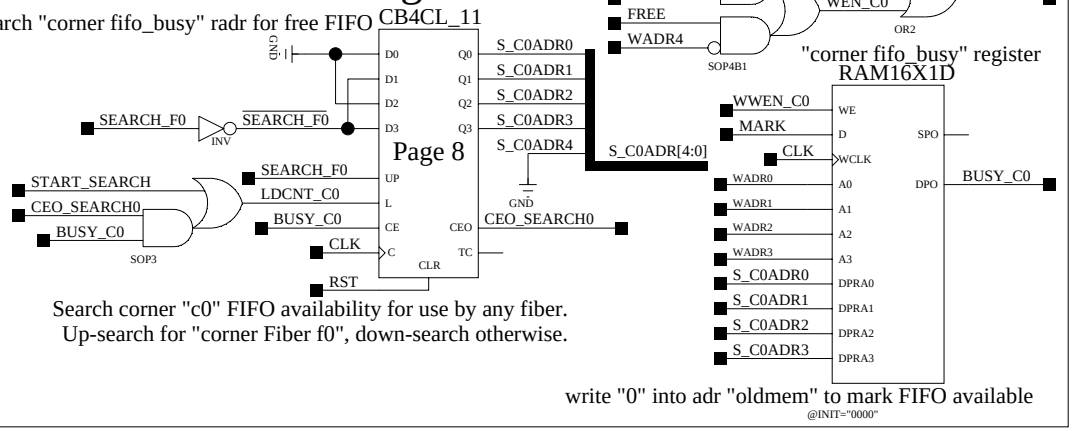
= 0xBC50 (in parallel)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Constant Bus Settings CMS CSC Electronics	BY JRG	PARENT PAGE 3B, 4B	PROJECT D785D
		DATE 1-27-2005_9:50	FILE IDLE16BIT . 1	PAGE 6

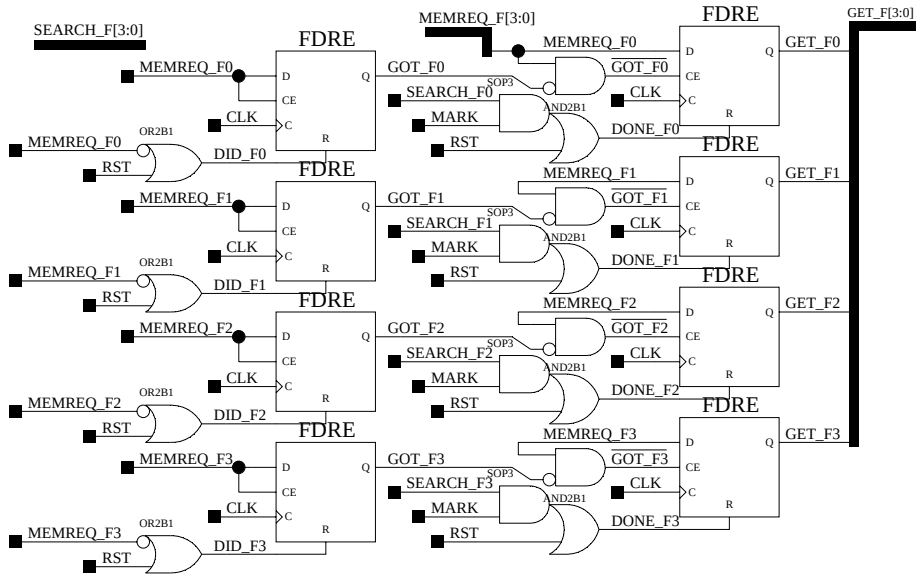
Corner 0 FIFO usage

search "corner fifo_busy" radr for free FIFO

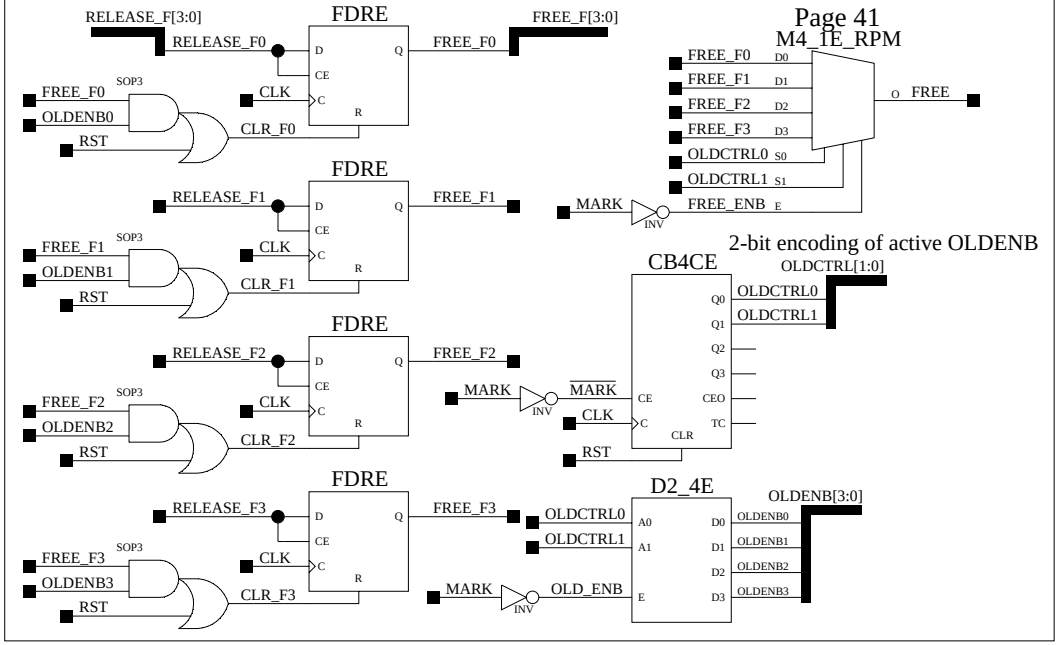


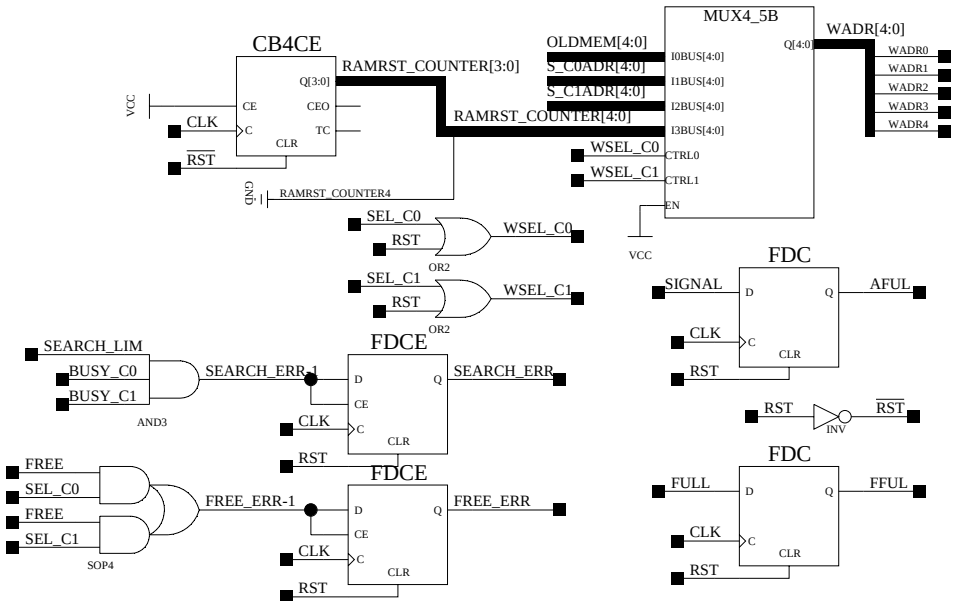
Search corner "c0" FIFO availability for use by any fiber.
Up-search for "corner Fiber f0", down-search otherwise.

Which Fibers need a new FIFO?



FIFO Release Control

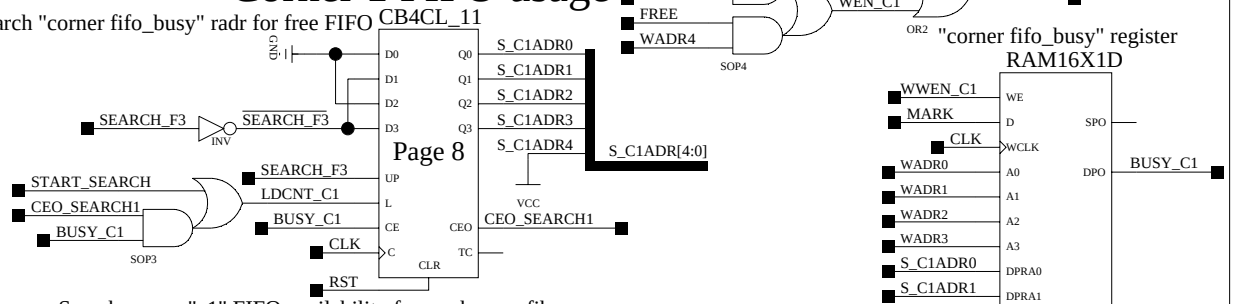




THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Memory Control Unit DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 11-14-2006_17:04	PARENT PAGE: 2, 2D FILE: MEM_CTRL . 1
		PROJECT: D785D	PAGE: 7

Corner 1 FIFO usage

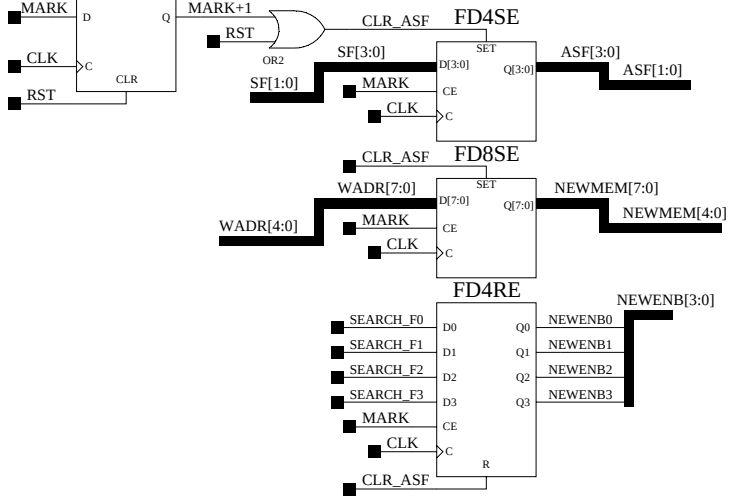
search "corner fifo_busy" radr for free FIFO



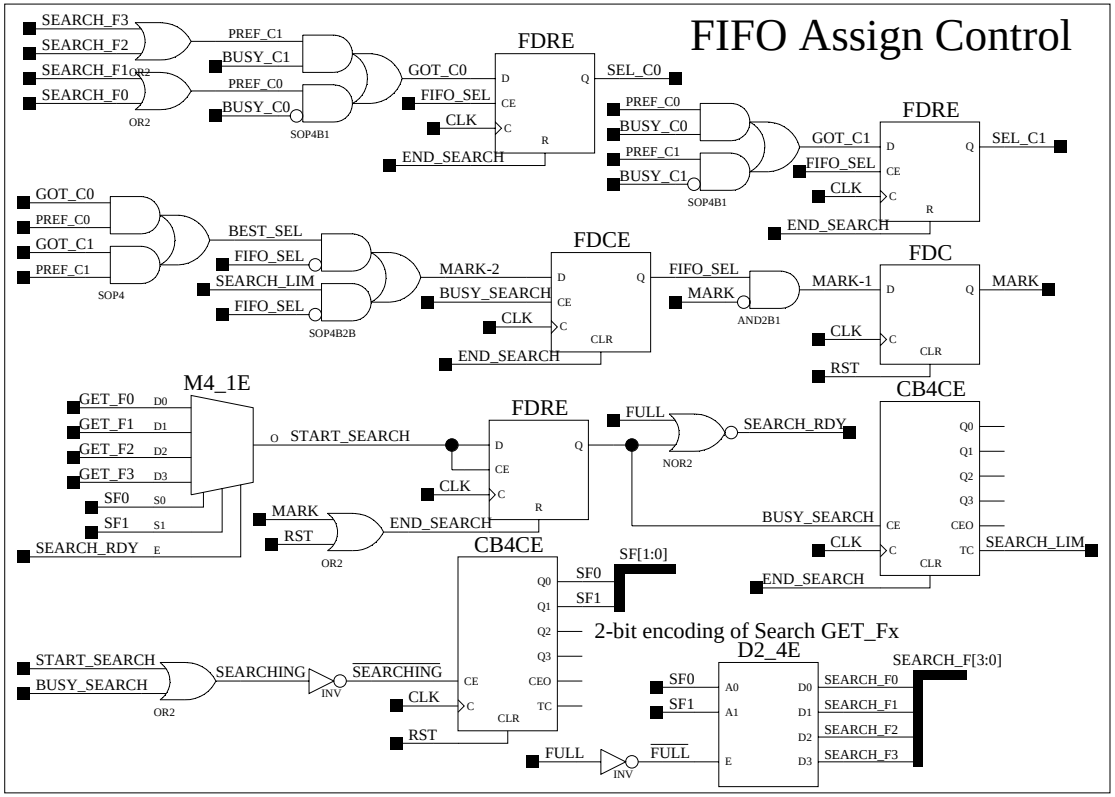
Search corner "c1" FIFO availability for use by any fiber.
Up-search for "corner Fiber f3", down-search otherwise.

write "0" into adr "oldmem" to mark FIFO available

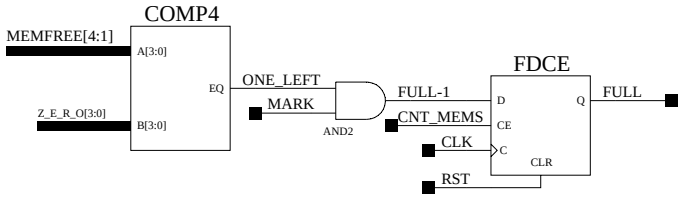
Assign Fiber to FIFO & Assign FIFO to Fiber



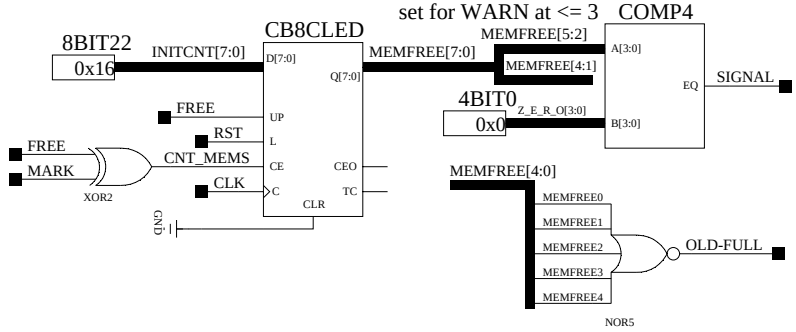
FIFO Assign Control



PREF_C[1:0]
BUSY_C[1:0]
GOT_C[1:0]



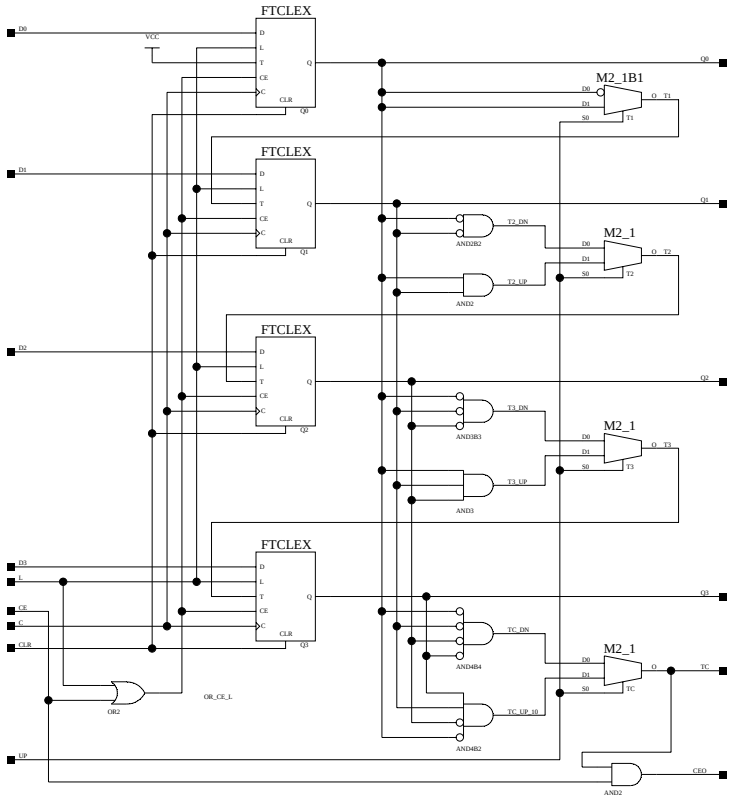
How many of 22 FIFOs are free?



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Memory Control Unit
DDU Input Controller Logic
CMS CSC Electronics

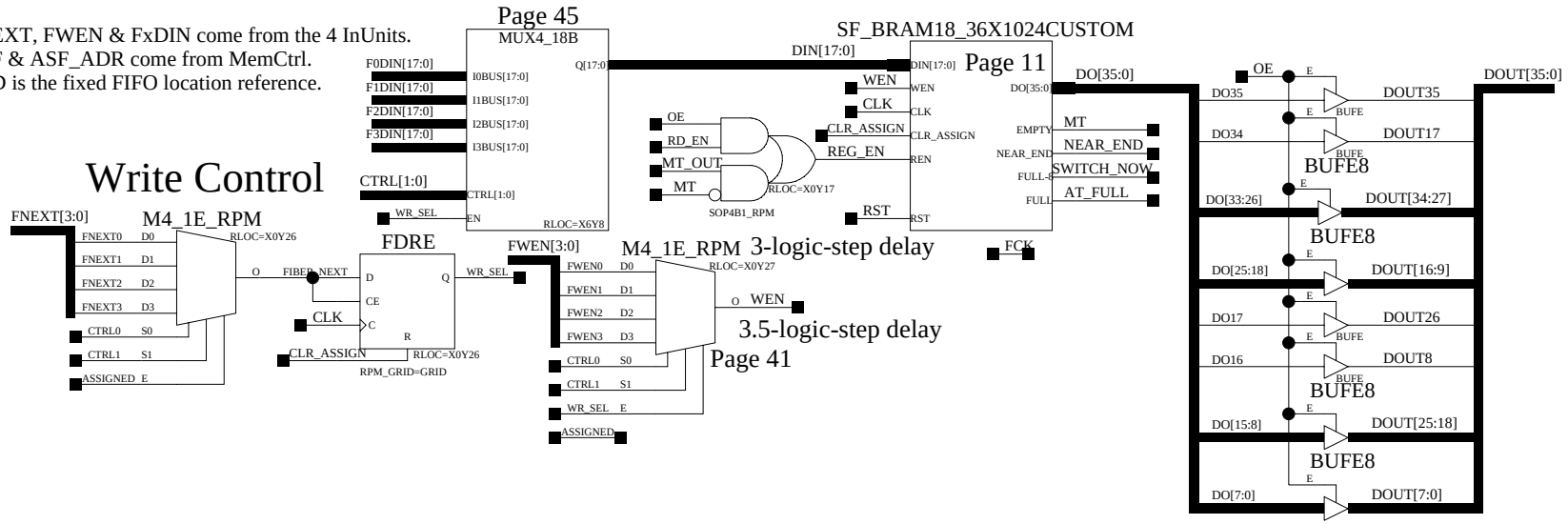
BY	PARENT PAGE	PROJECT
JRG	2, 2D	D785D
DATE	FILE	PAGE
11-14-2006_16:17	MEM_CTRL . 2	7A



XILINX

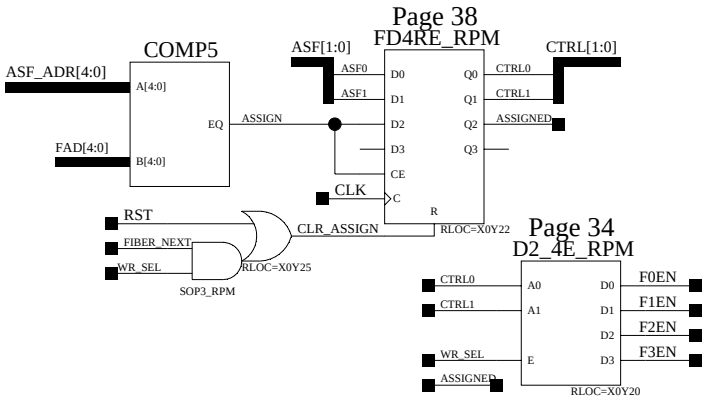
Title:	VIRTEX Family CB4CLED Macro
Comments:	JRG
	4-Bit Loadable,Casc,Dir(up/dwn)
	Binary Counter w/ Clk Enable & Async Clr. Set Up-Count TC thresh at 10 (0Ah)
Date:	21st August 2003
Ver:	1
Sheet Size: C	Rev: A

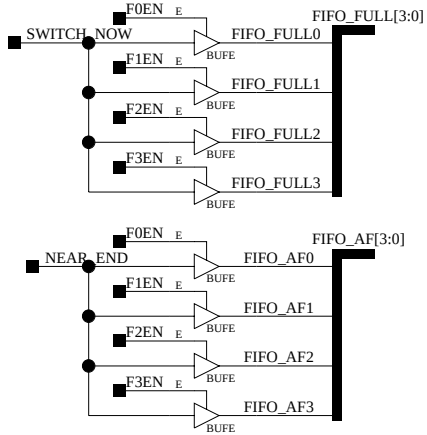
FNEXT, FWEN & FxDIN come from the 4 InUnits.
ASF & ASF_ADR come from MemCtrl.
FAD is the fixed FIFO location reference.



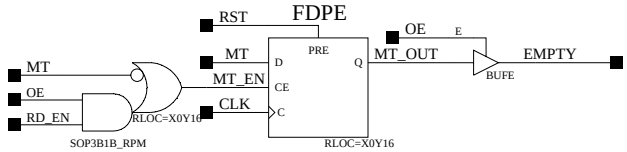
MemIn-MemOut Mapping:

DO35	Dout35
DO34	Dout17
DO33-26	Dout34-27
DO25-18	Dout16-9
DO17	Dout26
DO16	Dout8
DO15-8	Dout25-18
Din7-0	Dout7-0



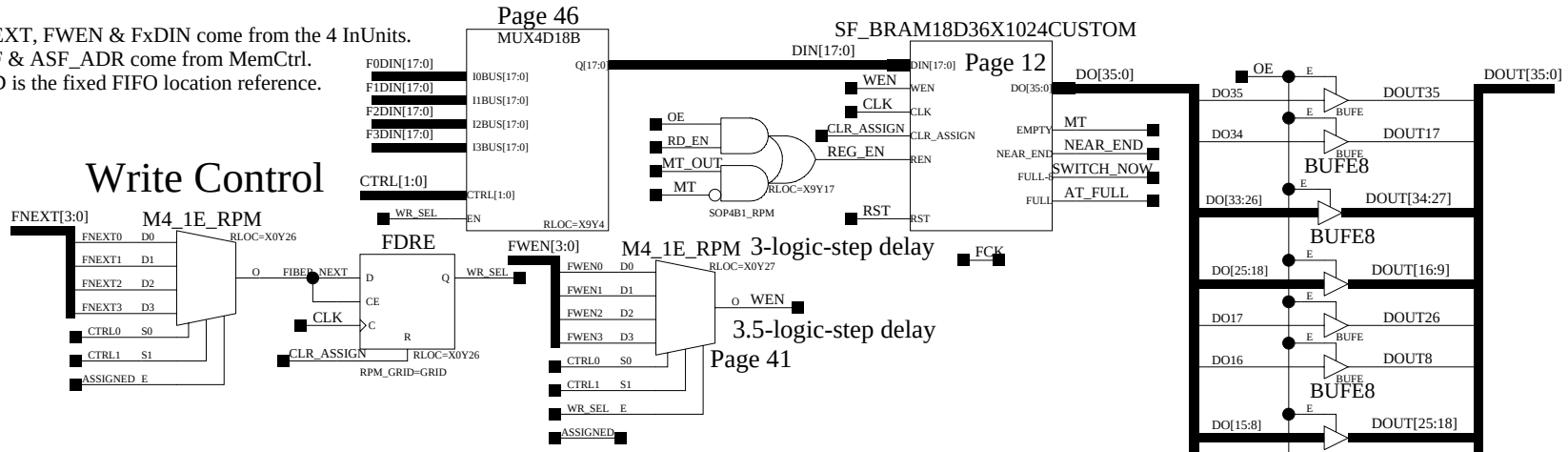


First Word Fall Through logic:



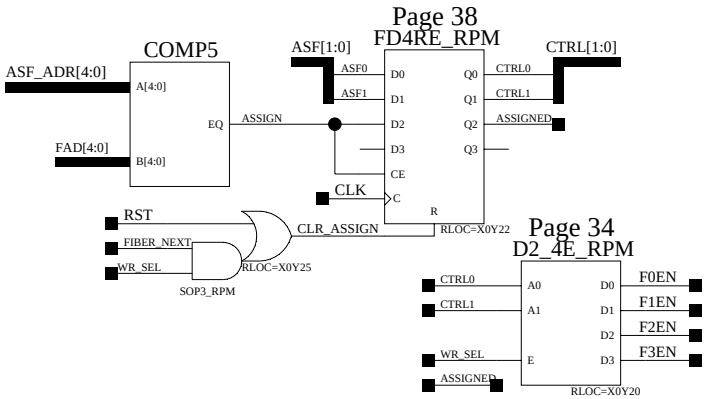
Not Used: REN = OE * RD_EN

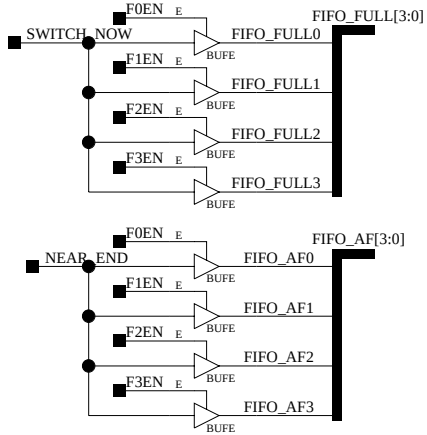
FNEXT, FWEN & FxDIN come from the 4 InUnits.
ASF & ASF_ADR come from MemCtrl.
FAD is the fixed FIFO location reference.



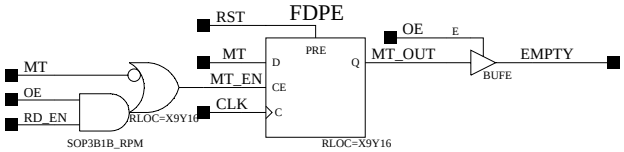
MemIn-MemOut Mapping:

DO35	Dout35
DO34	Dout17
DO33-26	Dout34-27
DO25-18	Dout16-9
DO17	Dout26
DO16	Dout8
DO15-8	Dout25-18
Din7-0	Dout7-0





First Word Fall Through logic:



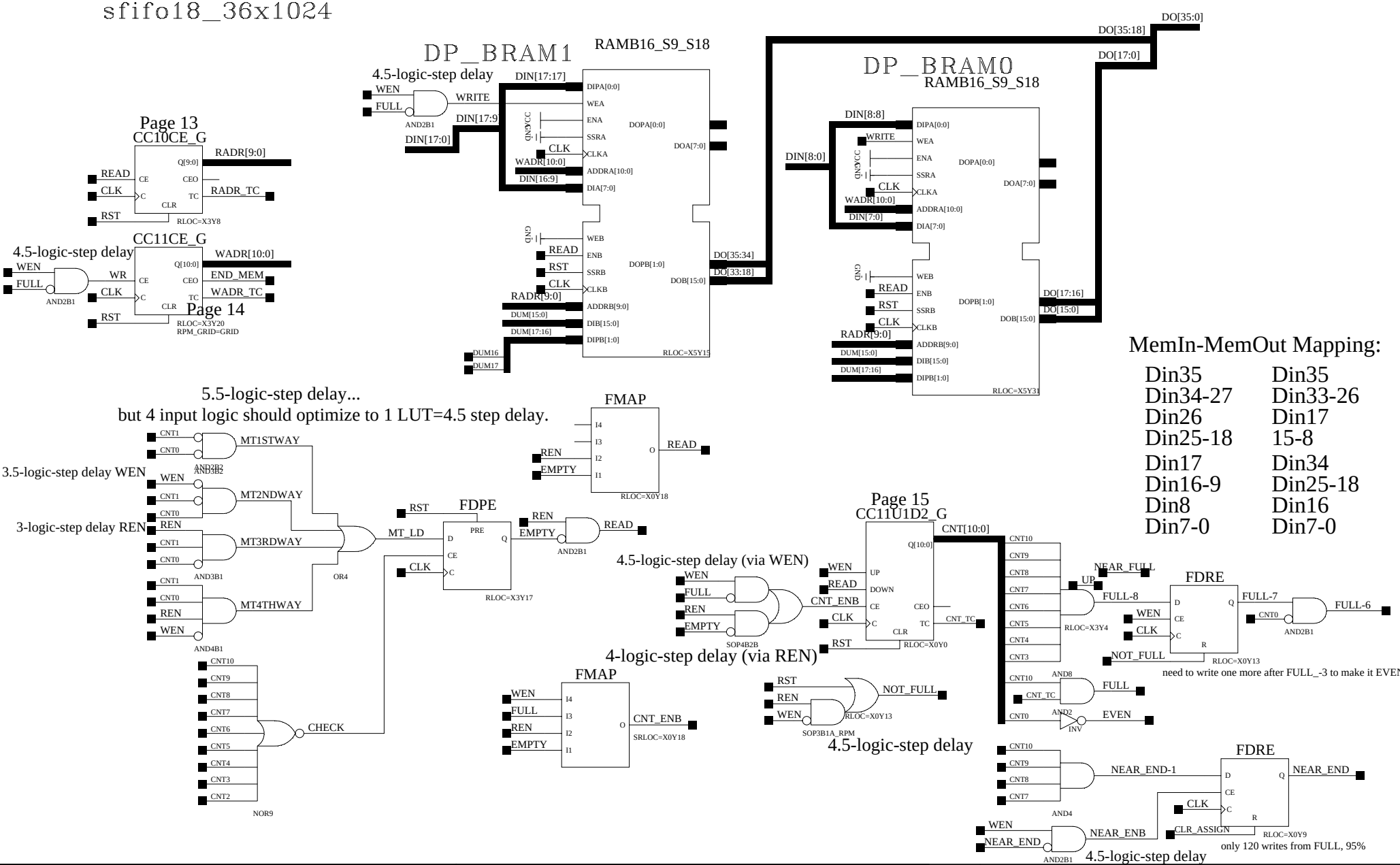
Not Used: REN = OE * RD_EN

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Memory Unit (FPGA BRAM FIFO) *Diagonal* w/FWFT
DDU Input Controller Logic
CMS CSC Electronics

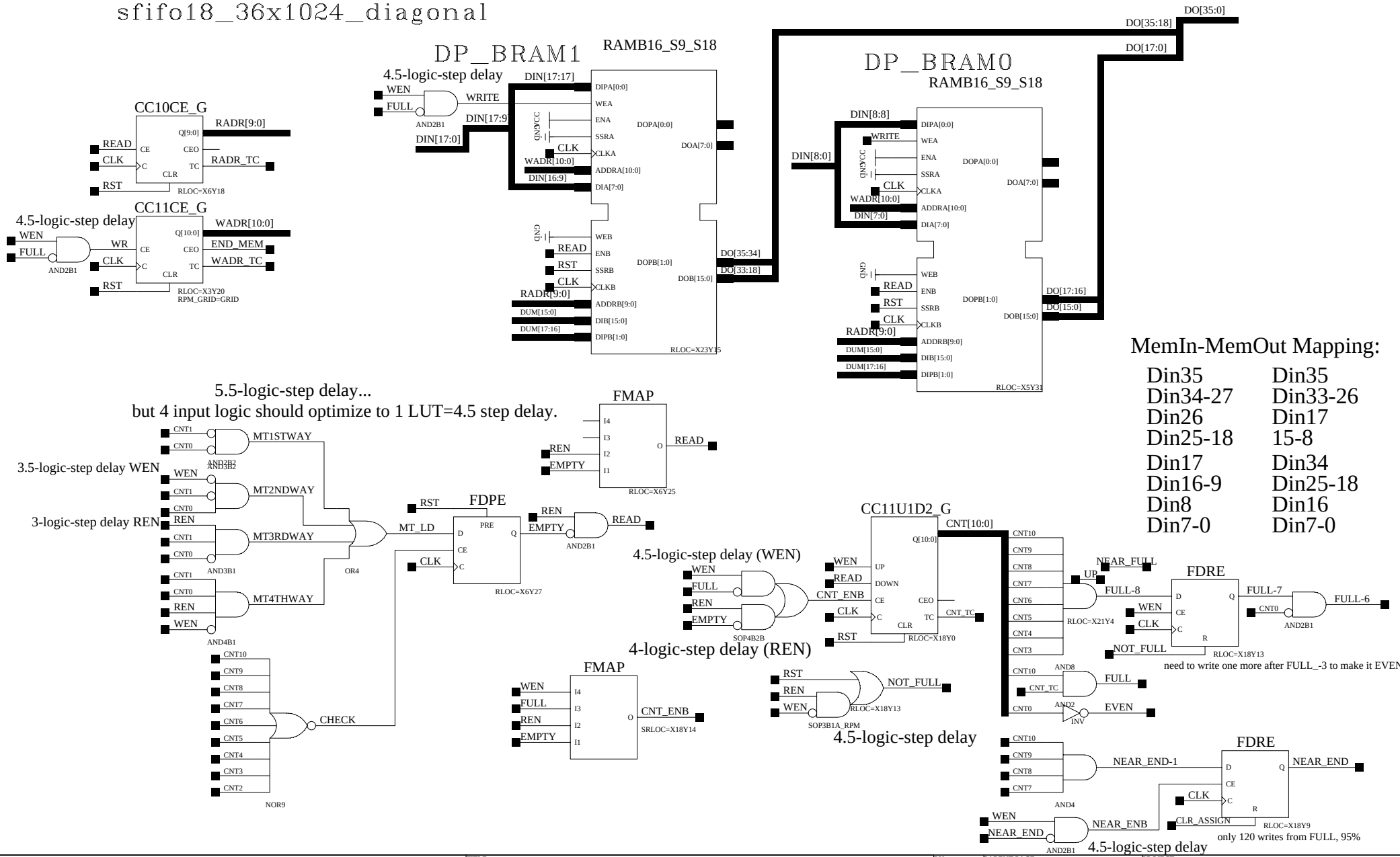
BY	PARENT PAGE	PROJECT
JRG	2C	D785D
DATE	FILE	PAGE
7-18-2005_14:44	MEMD_UNIT . 1	10

sfifo18_36x1024



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Sync. FIFO, 18 In, 36 Out by 1024 Deep DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 9	PROJECT D785D	
		DATE 7-18-2005_15:06	FILE SF_BRAM18_36X1024CUSTOM . 1		PAGE 11

sfifo18_36x1024_diagonal



MemIn-MemOut Mapping:

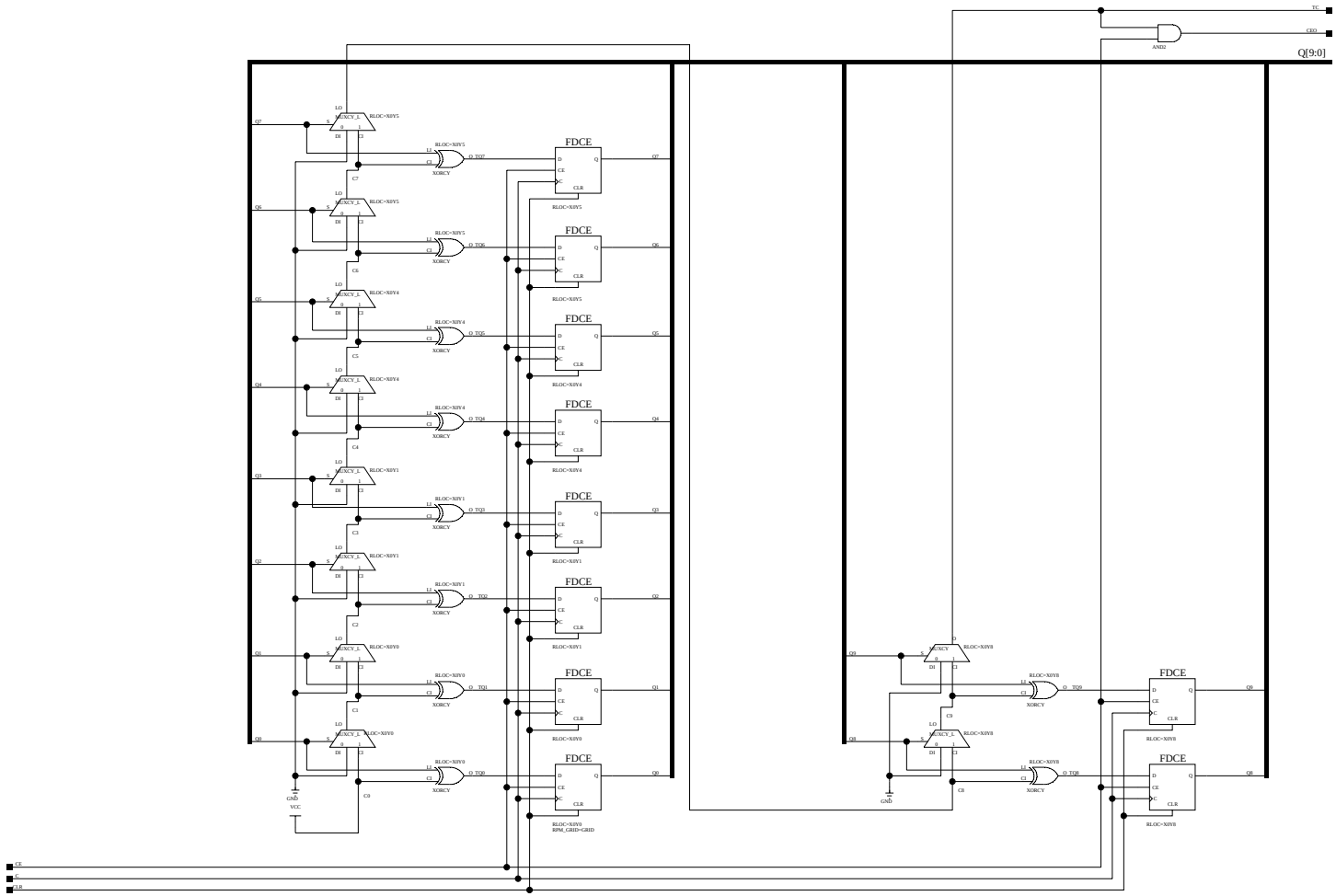
Din35	Din35
Din34-27	Din33-26
Din26	Din17
Din25-18	15-8
Din17	Din34
Din16-9	Din25-18
Din8	Din16
Din7-0	Din7-0

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Sync. FIFO, 18 In, 36 Out by 1024 Deep *DIAGONAL*
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	10	D785D

DATE	FILE	PAGE
1-27-2005_9:52	SF_BRAM18D36X1024CUSTOM . 1	12



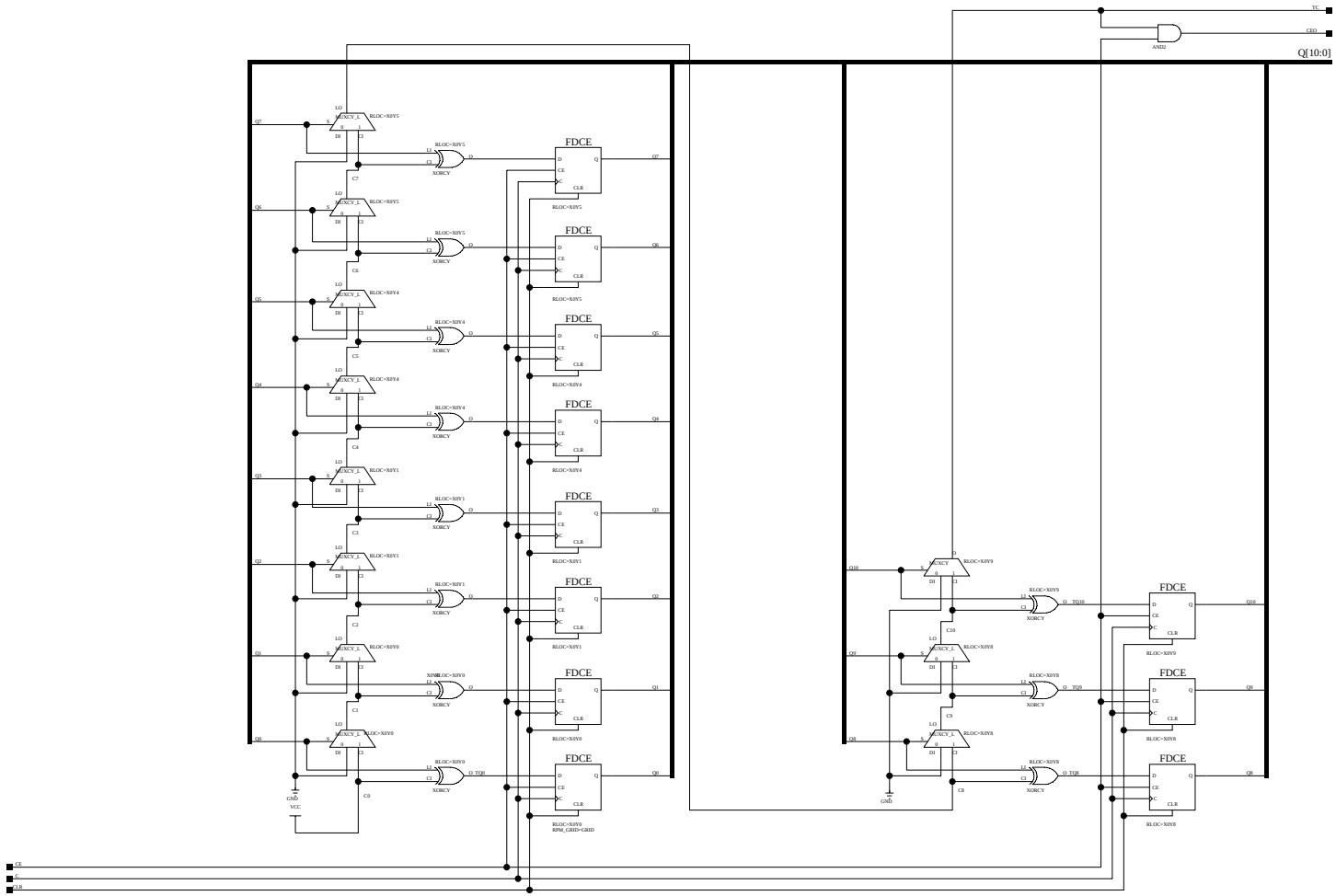
XILINX JRG

Title: VIRTEX Family CC10CE Macro

Comments: 10-Bit Cascadable Binary Counter
w/ Clk Enable & Async Clr (using MUXCY_L), RPM_GRID coords X0Y0.

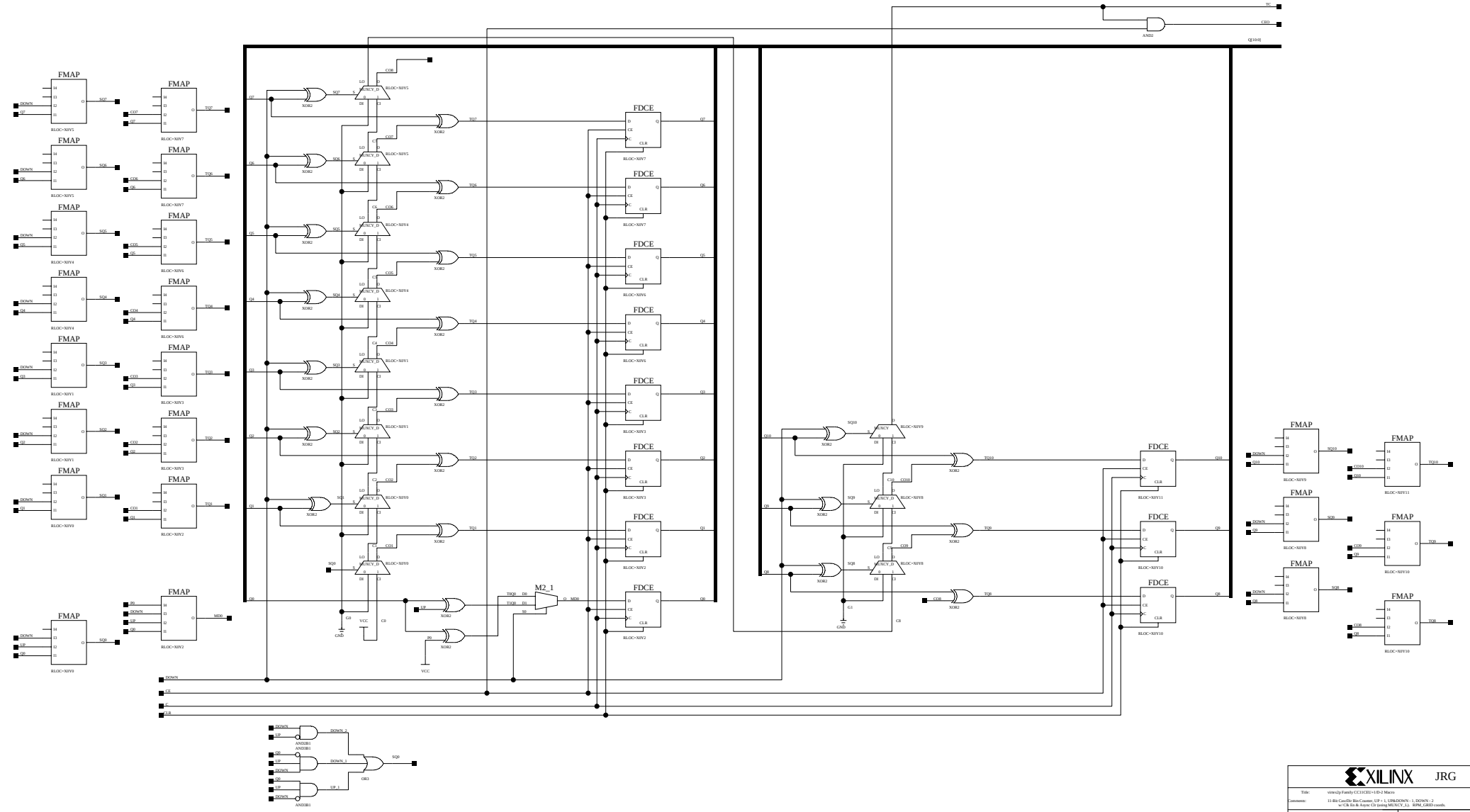
Date: 15th August 2003 | Ver: 1

Sheet Size: D | Rev: A



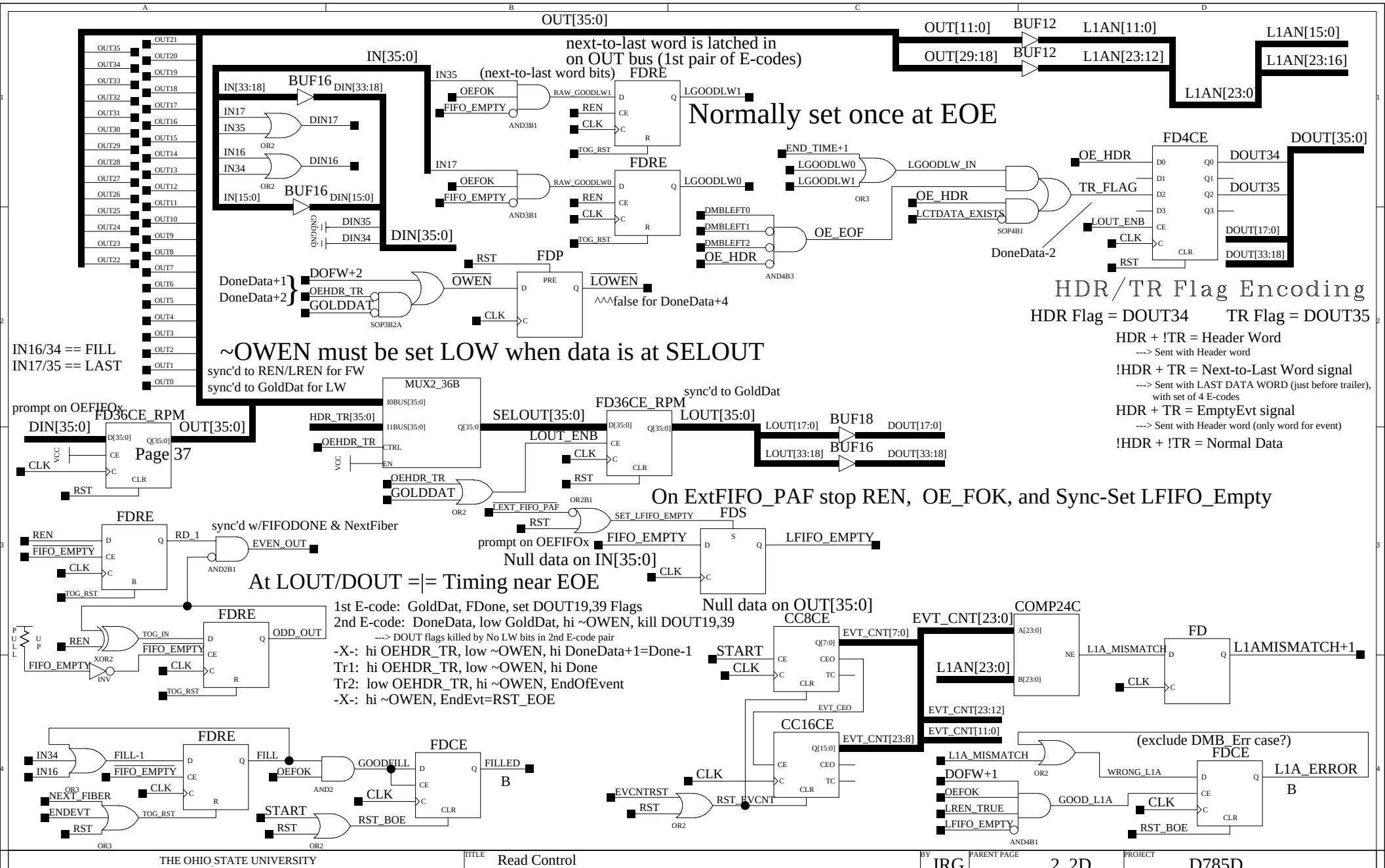
XILINX	JRG
Title:	VIRTEX Family CC11CE Macro
Comments:	11-Bit Cascadable Binary Counter w/ Clk Enable & Async Clr (using MUXCY_L). RPM_GRID coords X0Y0.
Date:	4th September 2003
Sheet Size:	D
Ver:	1
Rev:	A

UP = Increment 1
UP.DOWN = Decrement 1
DOWN = Decrement 2
Assume that CE includes DOWN+UP



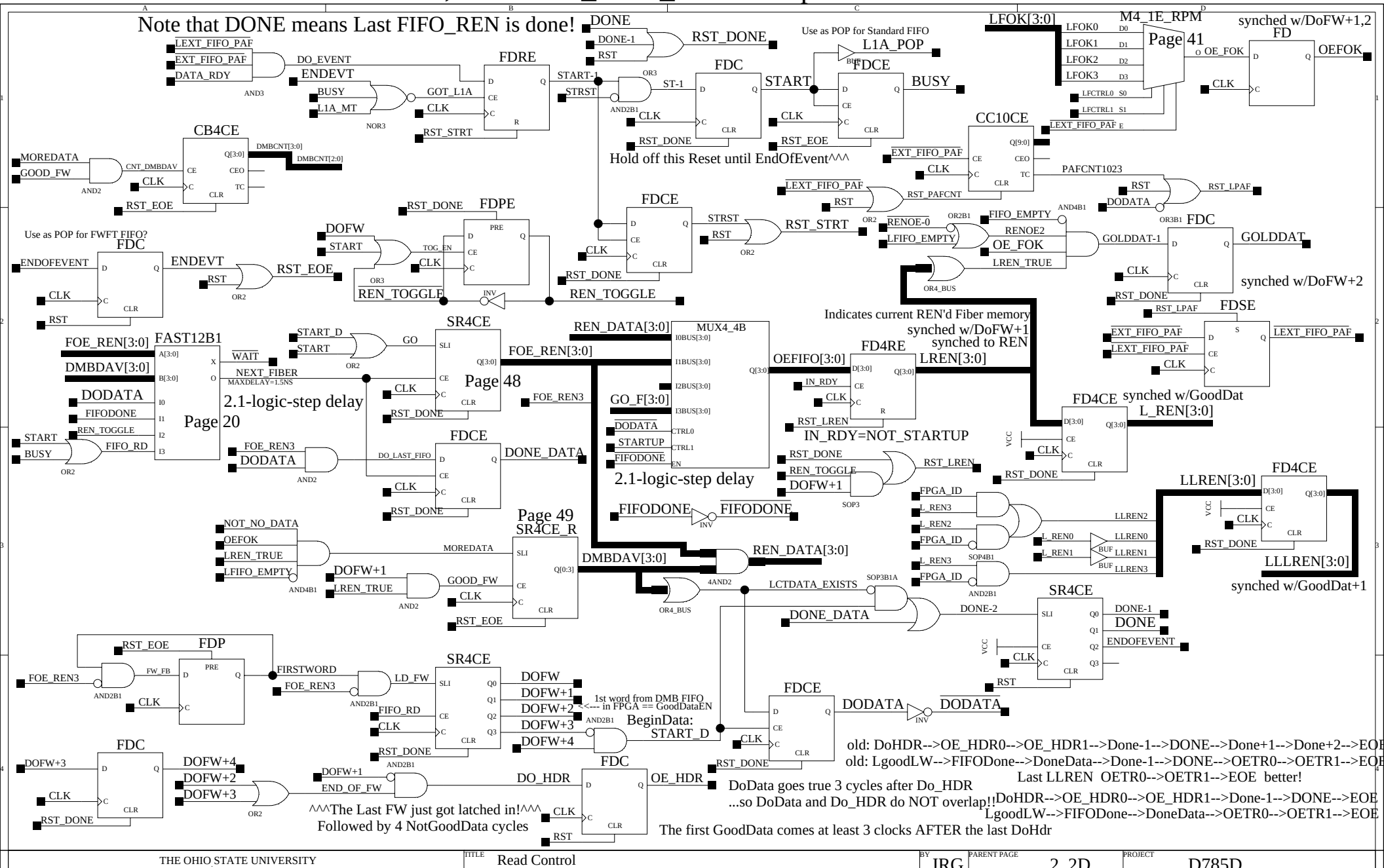
XILINX JRG

Title:	virtex2p Family CC11CEU+UD-2 Macro
Comments:	11-Bit CascDir Bin Counter, UP = 1, UP&DOWN - 1, DOWN - 2 w/ Clk En & Async Clr (using MUXCY_L) - RPM_GRID coords.
Date:	22nd October 2003
Sheet Size: D	

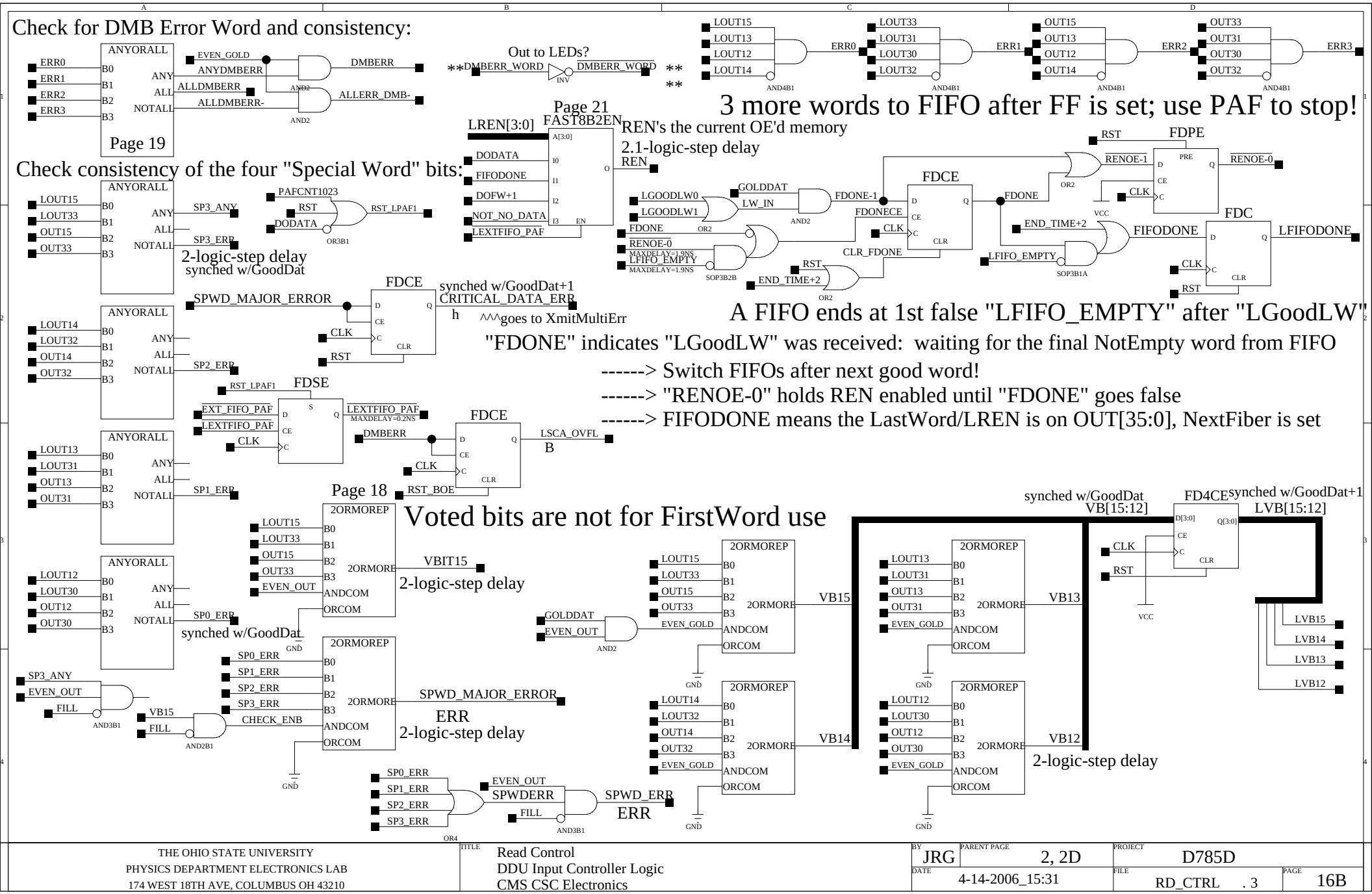


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2, 2D	PROJECT: D785D
		DATE: 1-3-2007_14:23	FILE: RD_CTRL . 1	PAGE: 16

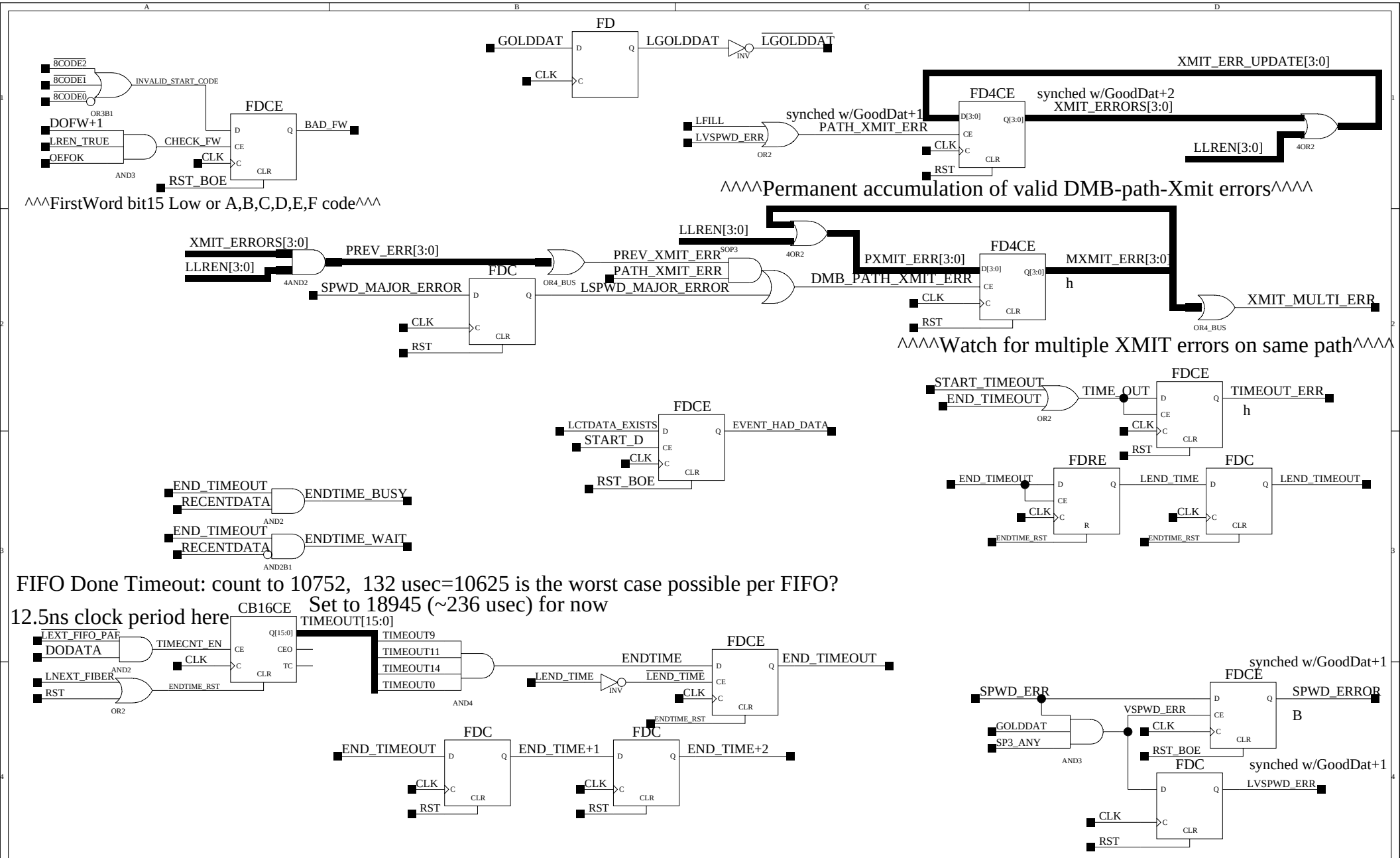
3 more words to FIFO after FF is set; use LEXT_FIFO_PAF to stop REN/OWEN!



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Read Control DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2, 2D	PROJECT D785D
		DATE 11-22-2006_15:44	FILE RD_CTRL . 2	PAGE 16A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2, 2D	PROJECT: D785D
		DATE: 4-14-2006_15:31	FILE: RD_CTRL . 3	PAGE: 16B



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2, 2D	PROJECT: D785D
		DATE: 11-22-2006_15:48	FILE: RD_CTRL . 4	PAGE: 16C

Status Monitor

Pick 8 Status signals, include in DAQ HDR/TR

-create logic for OEHDR/TR and their format

Also set 4 FMM bits for each input channel

removed from Hdr/Tr---> B LSCA_OVFL
--DDUctrl detects easily...
"SCA_OVFL"

B L1A_ERROR
B FILLED
OR2 → SINGLEERROR

In Hdr/Tr, removed from data--->
--DDUctrl can detect...

h MULT_L1A_ERR
h MEM_ERR
OR2 → SYNCERROR

#Bits useful at EOE (for Used Memories in event? 22 bits)

L1A #

12b HDR0TR[11:0] EVT_CNT[11:0] BUF12 HDR0TR[11:0]

12b HDR0TR[29:18] EVT_CNT[23:12] BUF12 HDR0TR[29:18]

HDR1TR[3:0]

4b DMBDAV

DMBDAV0 BUF HDR1TR0
DMBDAV1 BUF HDR1TR1
FPGA_ID BUF
DMBDAV3
DMBDAV2
FPGA_ID → HDR1TR2
DMBDAV3
FPGA_ID SOP4B1 → HDR1TR3

DMB Count

3b HDR1TR[6:4] DMBCNT[2:0] BUF3 HDR1TR[6:4]

HDR1TR[7] L1A_ERROR BUF HDR1TR7 B

HDR1TR[11:8]

1=alive, 0=killed

KILL_F0 BUF HDR1TR8
KILL_F1 BUF HDR1TR9
FPGA_ID BUF
KILL_F3
KILL_F2
FPGA_ID → HDR1TR10
KILL_F3
FPGA_ID SOP4B1 → HDR1TR11

Killed Channels

HDR1TR[21:18]

4b Live Channels

LFOK0 BUF HDR1TR18
LFOK1 BUF HDR1TR19
FPGA_ID BUF
LFOK3
LFOK2
FPGA_ID → HDR1TR20
LFOK3
FPGA_ID SOP4B1 → HDR1TR21
AND2B1

HDR1TR[29:22] "C-Code-Stat"

HDR1TR[29:22]

TIMEOUT_ERR BUF HDR1TR22 P
HSTUCK_DATA BUF HDR1TR23 P
XMIT_MULTI_ERR BUF HDR1TR24 P
FIBER_ERR BUF HDR1TR25 P
MEM_ERR BUF HDR1TR26 P
SINGLEERROR BUF HDR1TR27 B
SYNCERROR BUF HDR1TR28 P
"Hard Error"----->> CRITICALERROR BUF HDR1TR29 P

hdr1tr[29:22]
Bring
These
Out

SyncErr AND ~MemErr == MultL1Err

synched to LLLLREN/OE_TR1, inc CritDataErr

h TIMEOUT_ERR
h HSTUCK_DATA
h XMIT_MULTI_ERR
h FIBER_ERR
OR4 → CRITICALERROR "Hard Error"

Includes DLLerror,--->
RxError, SpwdError

SINGLE_WARN
SEL_HDRTR
SEL_HDRTR
SOP4B1 → HDR_TR17

FILLED
SEL_HDRTR
P MULT_L1A_ERR
SEL_HDRTR
SOP4B1 → HDR_TR16

HDR_TR35
HDR_TR34

HDR_TR[35:0]

STUCK_DATA
FDCE
CLK
RST
HSTUCK_DATA

HDR0TR[11:0]
HDR1TR[11:0]
SEL_HDRTR
MUX2_12B
HDR_TR[11:0]

4BITC 0x0C → HDR_TR[15:12]

HDR0TR[29:18]
HDR1TR[29:18]
SEL_HDRTR
MUX2_12B
HDR_TR[29:18]

4BITC 0x0C → HDR_TR[33:30]

FDC
DONE_DATA+1 → DONE_DATA+2
CLK
RST

DONE_DATA+2
END_TIME+2
OR2 → ENDING_SEL
OE_HDR
DOFW+3
SOP3B1A

DMBCNT[2:0]
CB4CLED
DMBCNT0 → DMBLEFT0
DMBCNT1 → DMBLEFT1
DMBCNT2 → DMBLEFT2
START_D
OE_HDR
LFIFODONE
CLK
RST_EOE

^^^count DMBs left for readout^^^

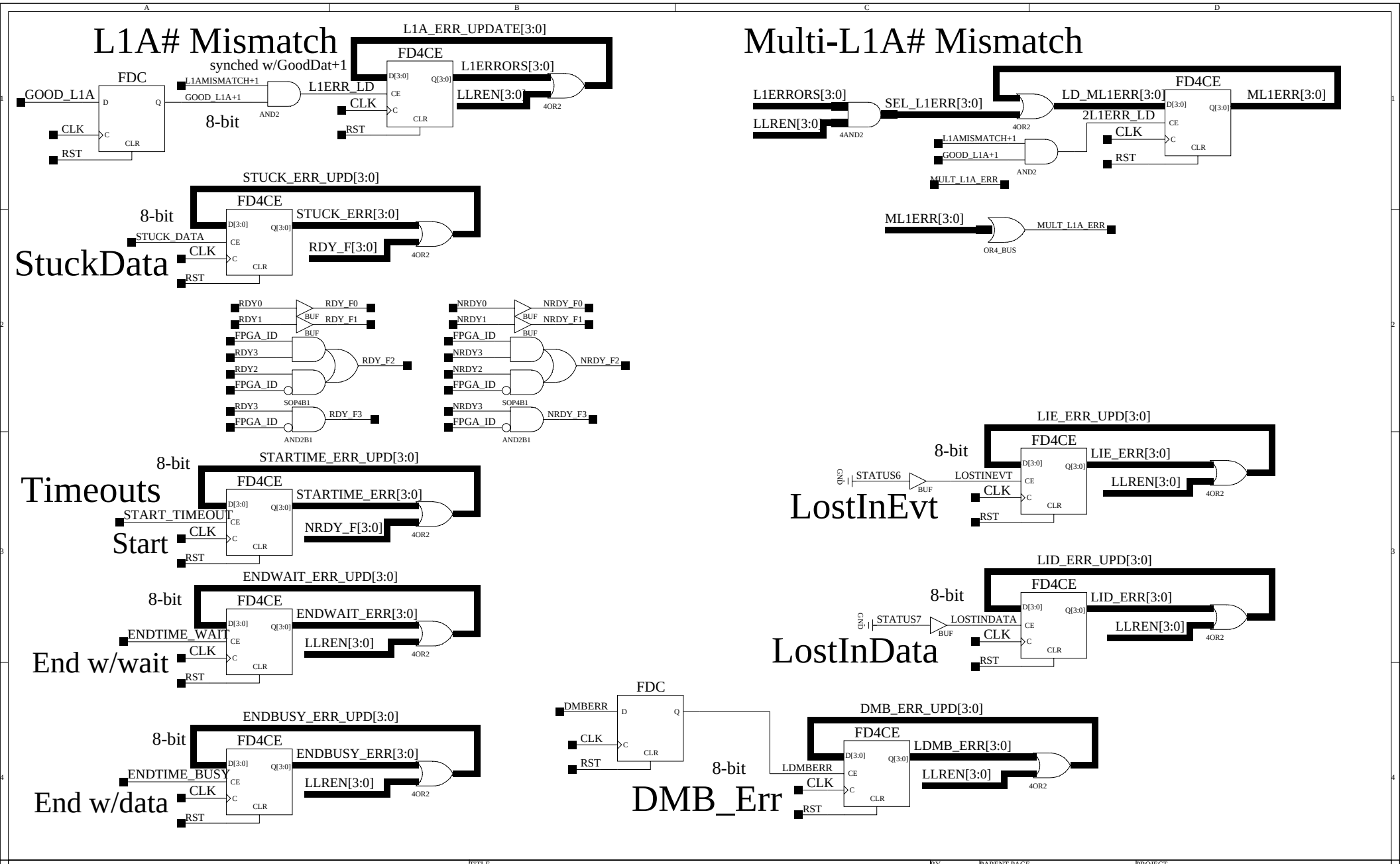
END_TIMEOUT
END_TIME+1
DONE_DATA
DONE_DATA+1
DOFW+2
DOFW+3
OR6

FDC
DONE_DATA
CLK
RST

DOFW+1
EN_HDRTR
AND2B1 → DO_HDR_TR

FDC
CLK
RST
OEHDR_TR

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Read Control DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2, 2D	PROJECT D785D
			DATE 1-3-2007_14:23	FILE RD_CTRL . 5	PAGE 16D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2, 2D	PROJECT: D785D
		DATE: 12-19-2005_13:31	FILE: RD_CTRL . 6	PAGE: 16E

H1: 0x/5T/NN.NNNN/XXX/I.II/VK
(BOE1 type L1A _Number BXN ID FOV K-Status)

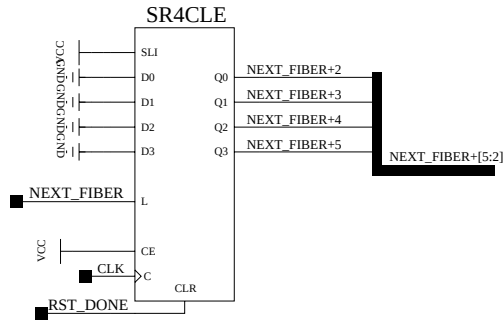
H2: 0x/8000/0001/8000/HHHH
(49-bit ~unique constant DMBfull(15))

H3: 0x/LLLL/oooo/ZZZZ/GGMY
(LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt)

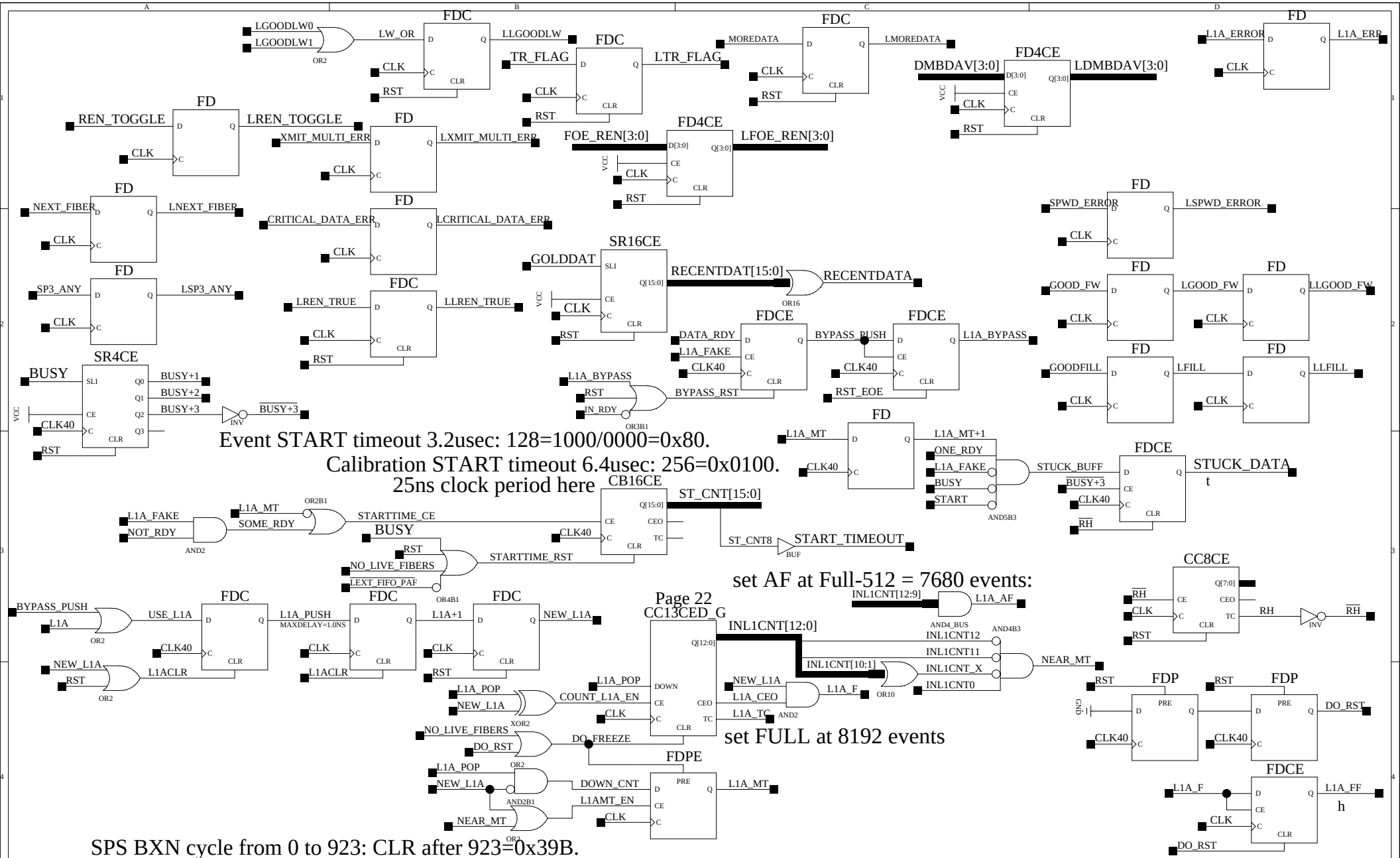
T-2: 0x/8000/FFFF/8000/8000
(64-bit unique constant)

T-1: 0x/SSSS.SSSS/QQQQ/PPPP
(DDU EOE Status DMBerr DMBwarn(15))

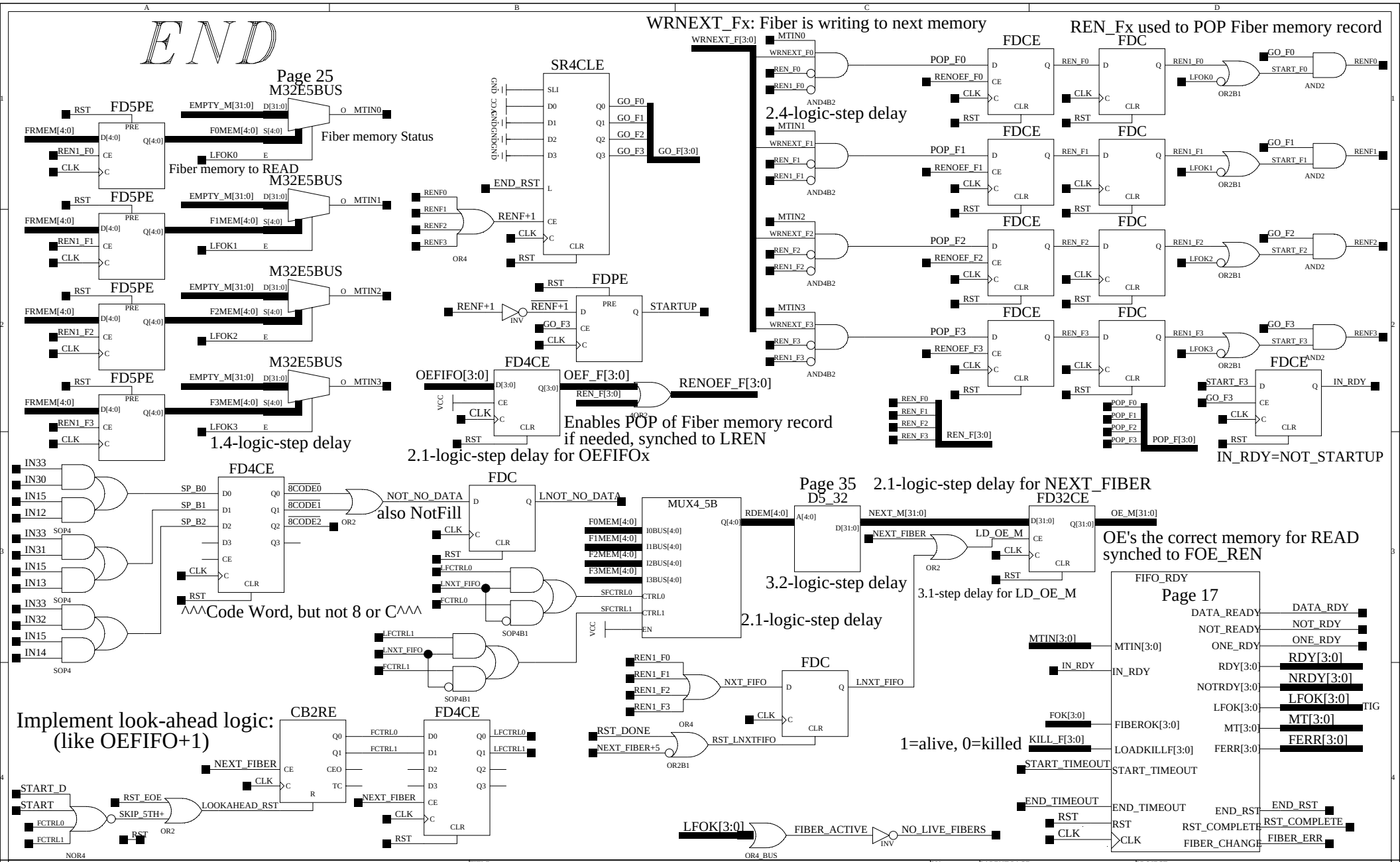
TR: 0x/A/?/WW.WWWW/RRRR/UUMK
(EOE WordCount CRCword EOEstat K-Status)

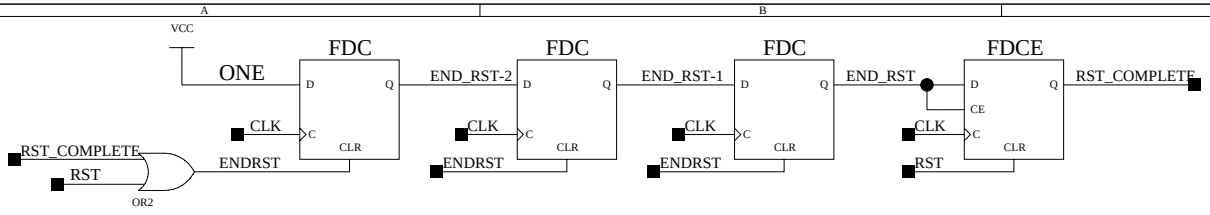


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2, 2D	PROJECT: D785D
		DATE: 11-27-2006_9:41	FILE: RD_CTRL . 7	PAGE: 16F

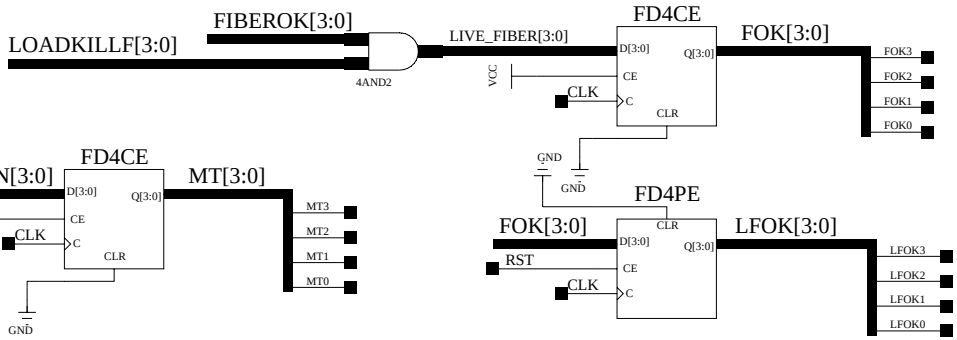


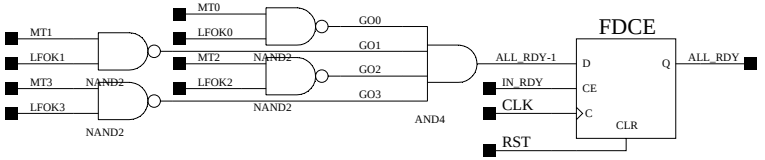
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Read Control DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2, 2D	PROJECT D785D
		DATE 1-11-2006_17:59	FILE RD_CTRL . 8	PAGE 16G

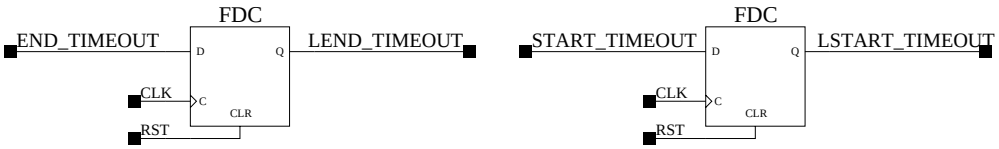

END
Page 25
WRNEXT_Fx: Fiber is writing to next memory
REN_Fx used to POP Fiber memory record
M32E5BUS
FD5PE
Fiber memory Status
Fiber memory to READ
SR4CLE
2.4-logic-step delay
FDCE
FDC
FDPE
OR4
AND4B2
OR2B1
AND2
FD4CE
Enables POP of Fiber memory record
if needed, synched to LREN
2.1-logic-step delay for OEFIFOx
1.4-logic-step delay
IN_RDY=NOT_STARTUP
Page 35
2.1-logic-step delay for NEXT_FIBER
D5_32
FD32CE
OE's the correct memory for READ
synched to FOE_REN
3.2-logic-step delay
3.1-step delay for LD_OE_M
MUX4_5B
2.1-logic-step delay
SOP4
SOP4B1
^^^Code Word, but not 8 or C^^^
also NotFill
Implement look-ahead logic:
(like OEFIFO+1)
CB2RE
NOR4
1=alive, 0=killed
FIFO_RDY
Page 17
OR4_BUS
INV
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
Read Control
DDU Input Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 2, 2D
PROJECT D785D
DATE 11-27-2006_9:41
FILE RD_CTRL . 9
PAGE 16H



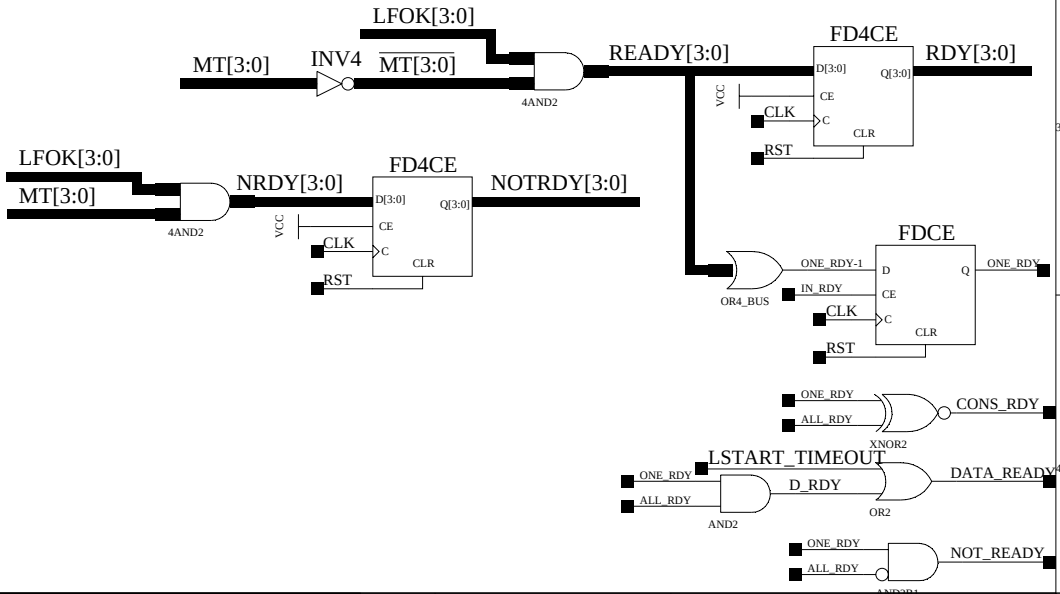
Access FIBEROK from JTAG as a fiber check.
---> RESET required after fiber status change for now...
Change in FIBEROK is BAD! Set error code.
...notify FMM and maybe set STATUS bit, but
...data is OK until FIFO read time-out occurs.
...but how to know WHEN the bad-data comes out?
---> timeout will probably occur for that event



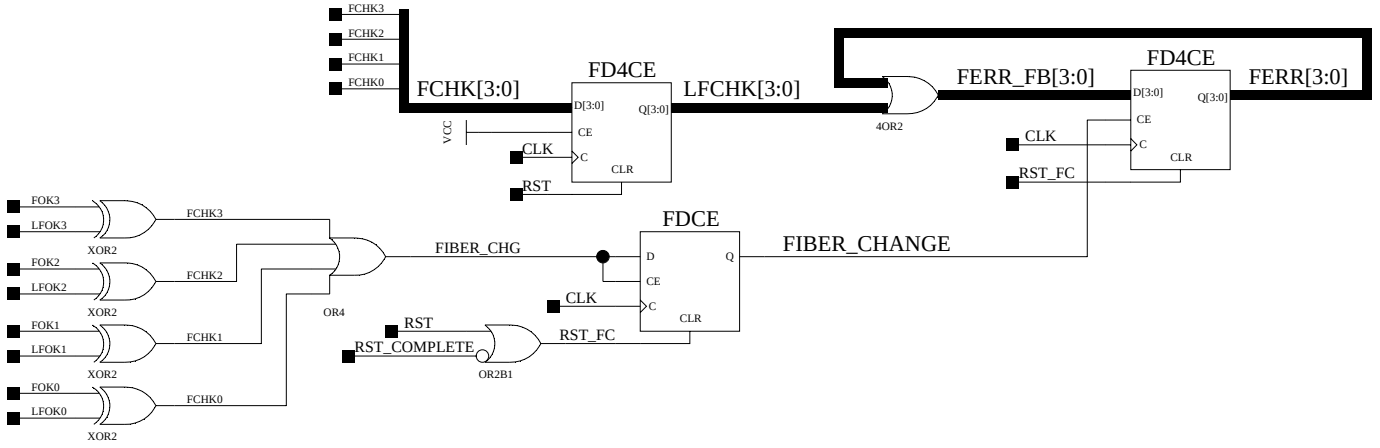




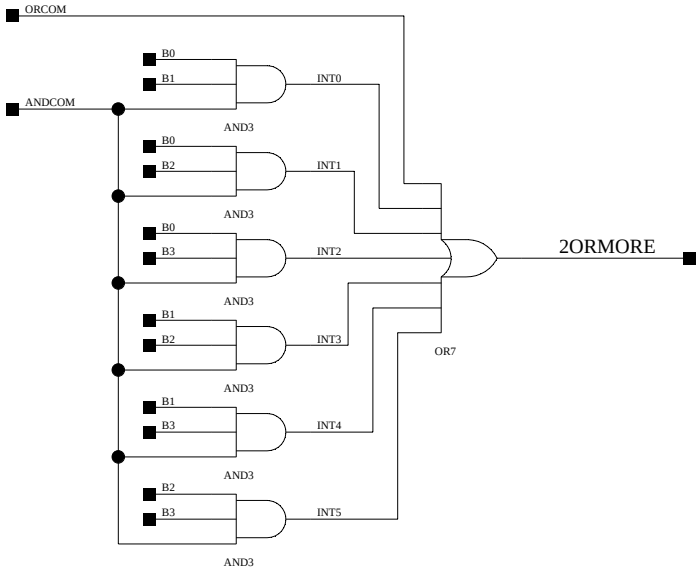
MASK fiber on Start/End TIMEOUT? Kill it in LFOK...



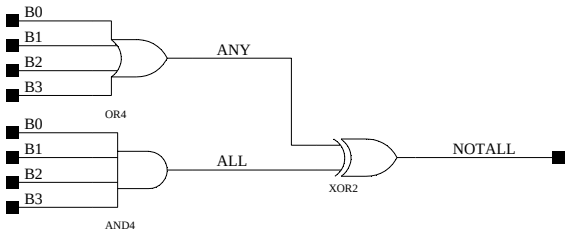
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 16H	PROJECT: D785D
		DATE: 5-10-2006_14:26	FILE: FIFO_RDY . 1	PAGE: 17



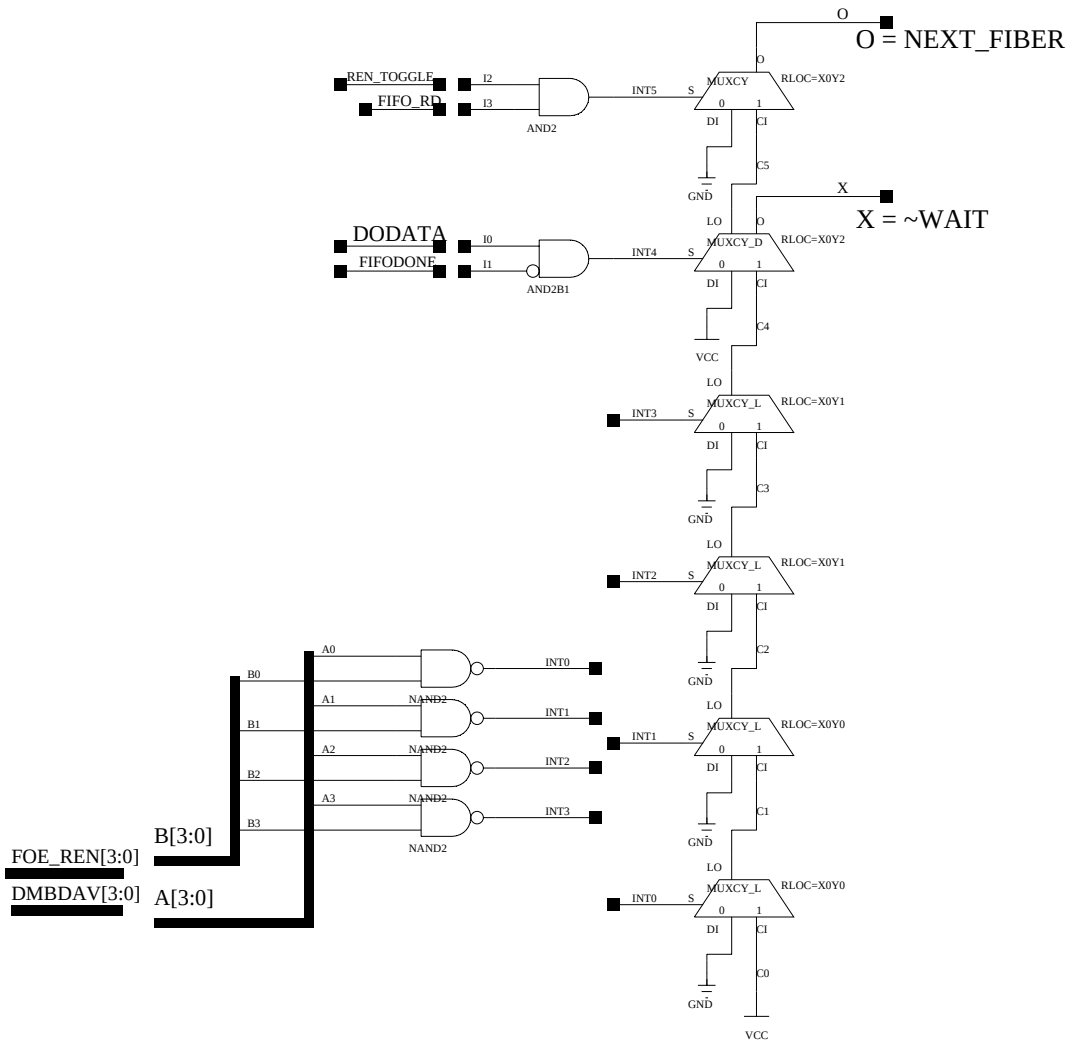
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 16H	PROJECT: D785D
		DATE: 1-27-2005_9:59	FILE: FIFO_RDY . 2	PAGE: 17A



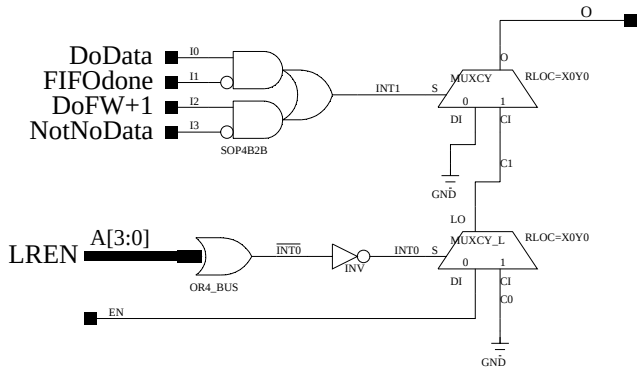
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 16B	PROJECT D785D
			DATE 1-27-2005_10:00	FILE 2ORMOREP . 1	PAGE 18



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for ALL bits set, ANY bits set and NOTALL bits set DDU Input Controller Logic CMS CSC Electronics	BY: JRG DATE: 1-27-2005_10:01	PARENT PAGE: 16B	PROJECT: D785D FILE: ANYORALL . 1 PAGE: 19



XILINX			JRG
Title:	FAST12B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 2 as AND similar to: OR of 4 AND2 .AND. AND2B1 .AND. AND2		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A



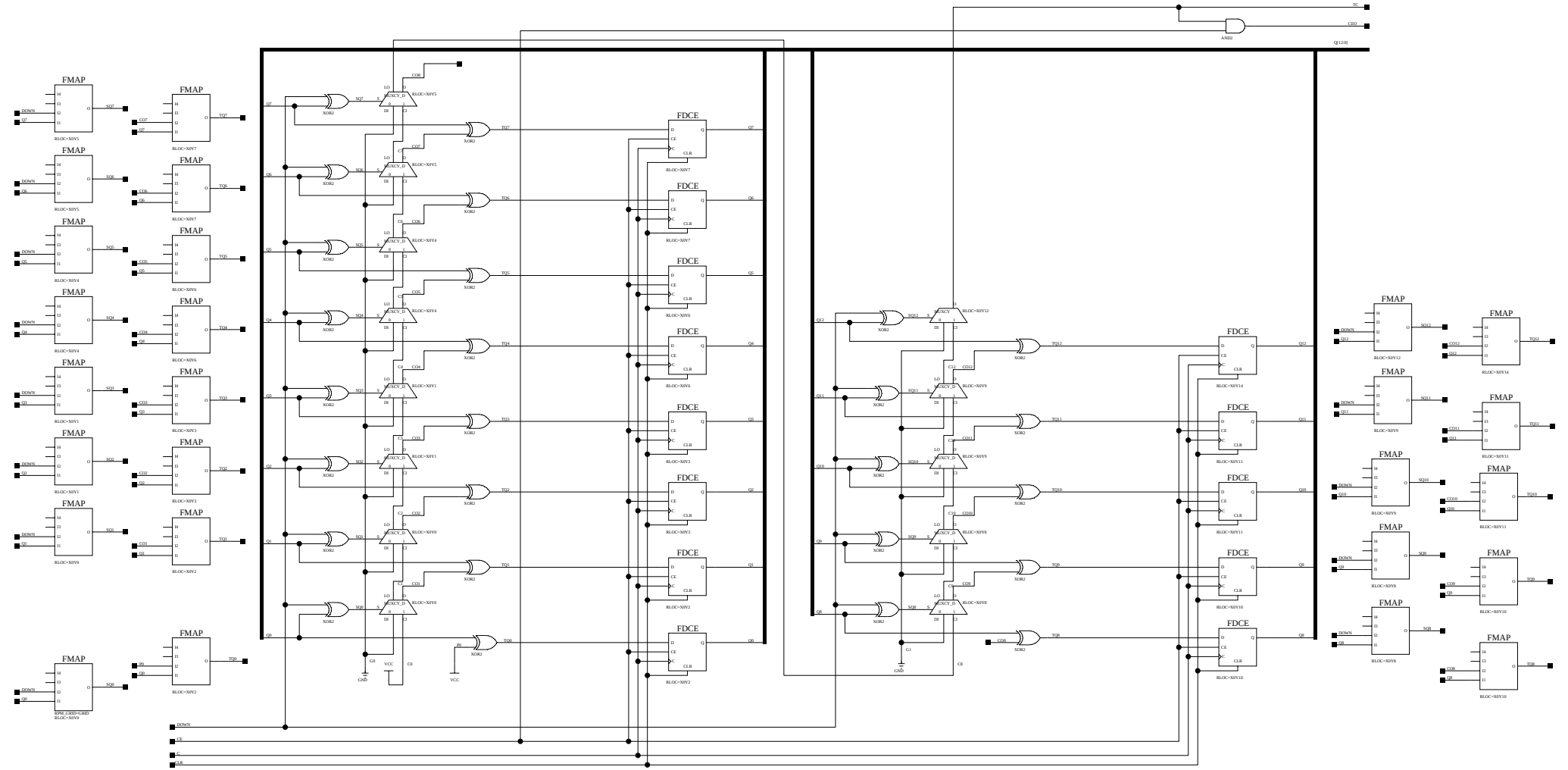
XILINX

JRG

Title:	FAST8B2EN		
Comments:	Custom Fast, Complex Logic for DDU, use 2 MUXCY as AND similar to: OR4 AND SOP4B2b		
Date:	14th September 2004	Ver:	1
Sheet Size: B		Rev:	A

DOWN = Decrement 1

Assume that CE includes DOWN+UP



XILINX JRG

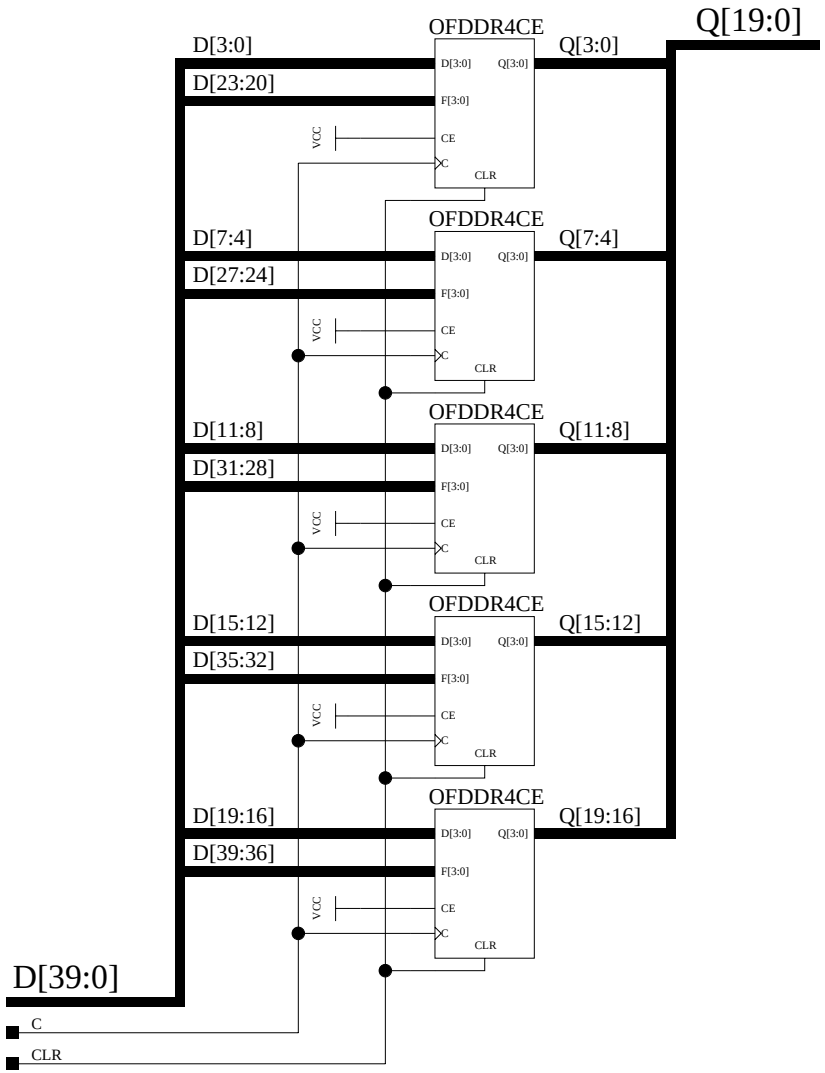
Title: virtex2p Family CC13CED Macro

Comments: 13-Bit CascDir Bin Counter
w/ Clk En & Async Clr (using MUXCY_L). RPM_GRID coords.

Date: 22nd October 2003 Ver: 1

Sheet Size: D Rev: A

the D byte goes out last (on C rising edge)
the F byte goes out first (on C falling edge)

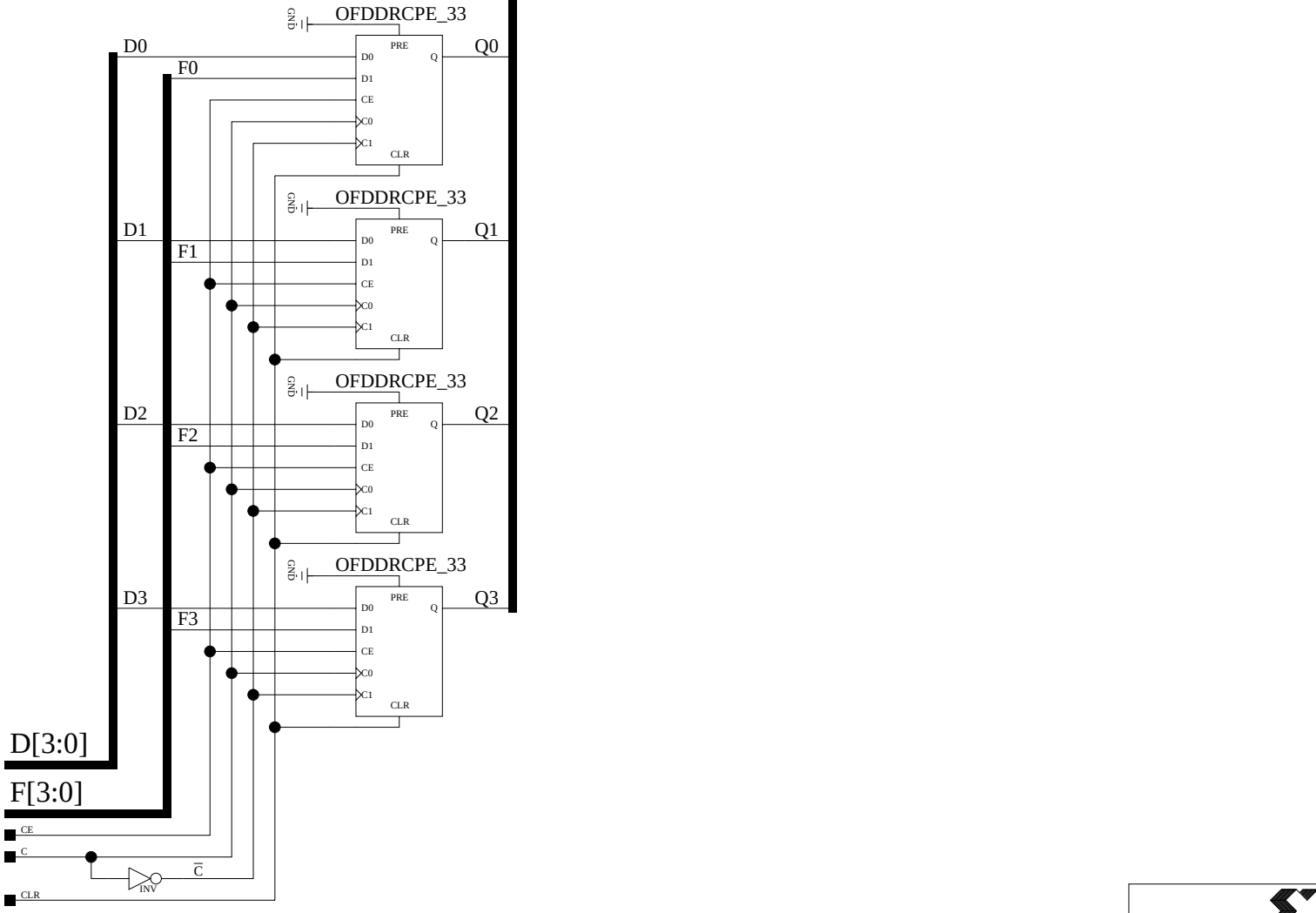


XILINX

Title: VIRTEX Family OFDDR40 Macro
Comments: 40-Bit Output DDR Flip-Flop w/Asynchronous Clear
JRG

Date:	16th December 2003	Ver:	1
Sheet Size: B		Rev:	A

the D byte goes out last (on C rising edge)
the F byte goes out first (on C falling edge)



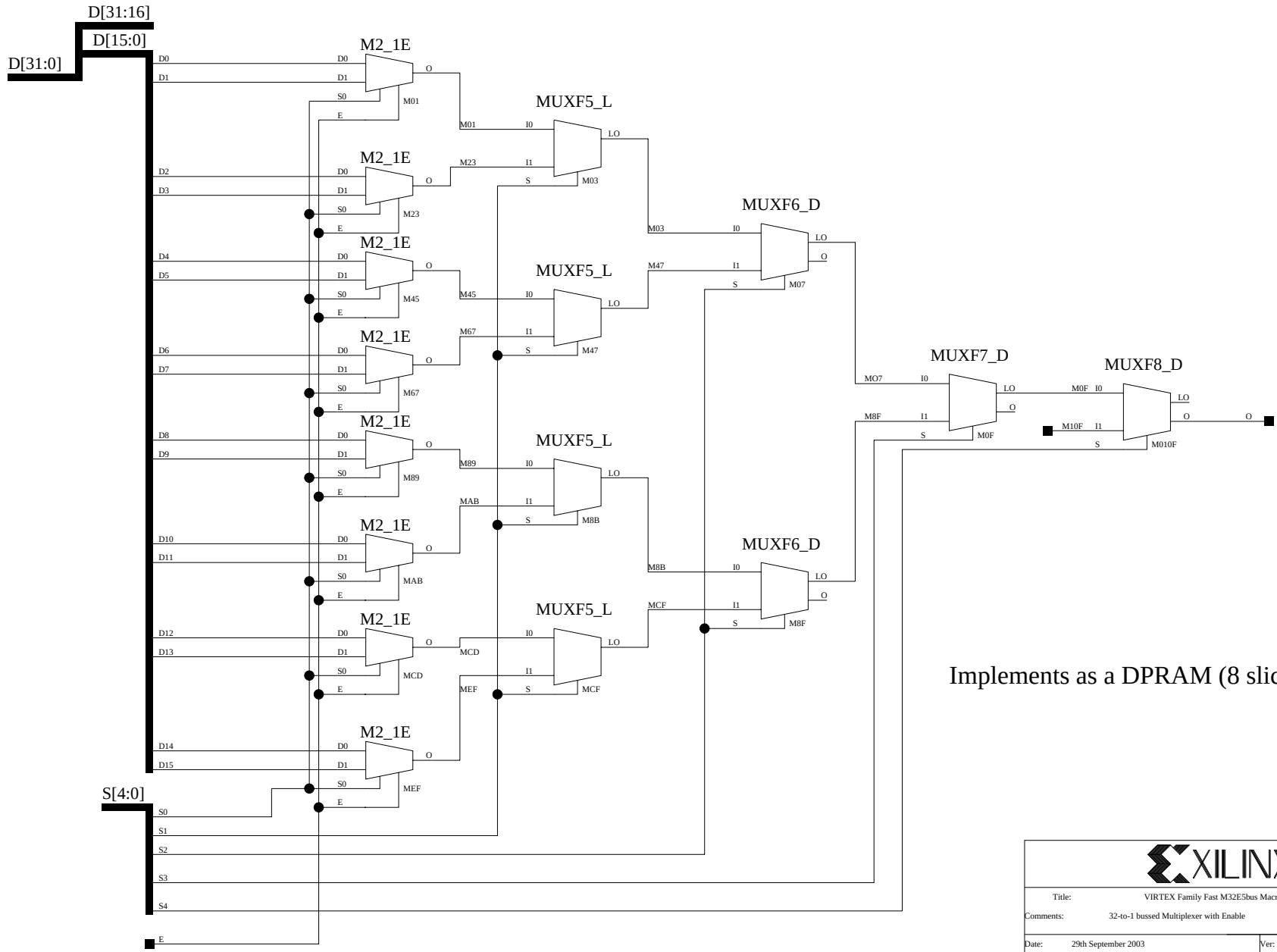
XILINX

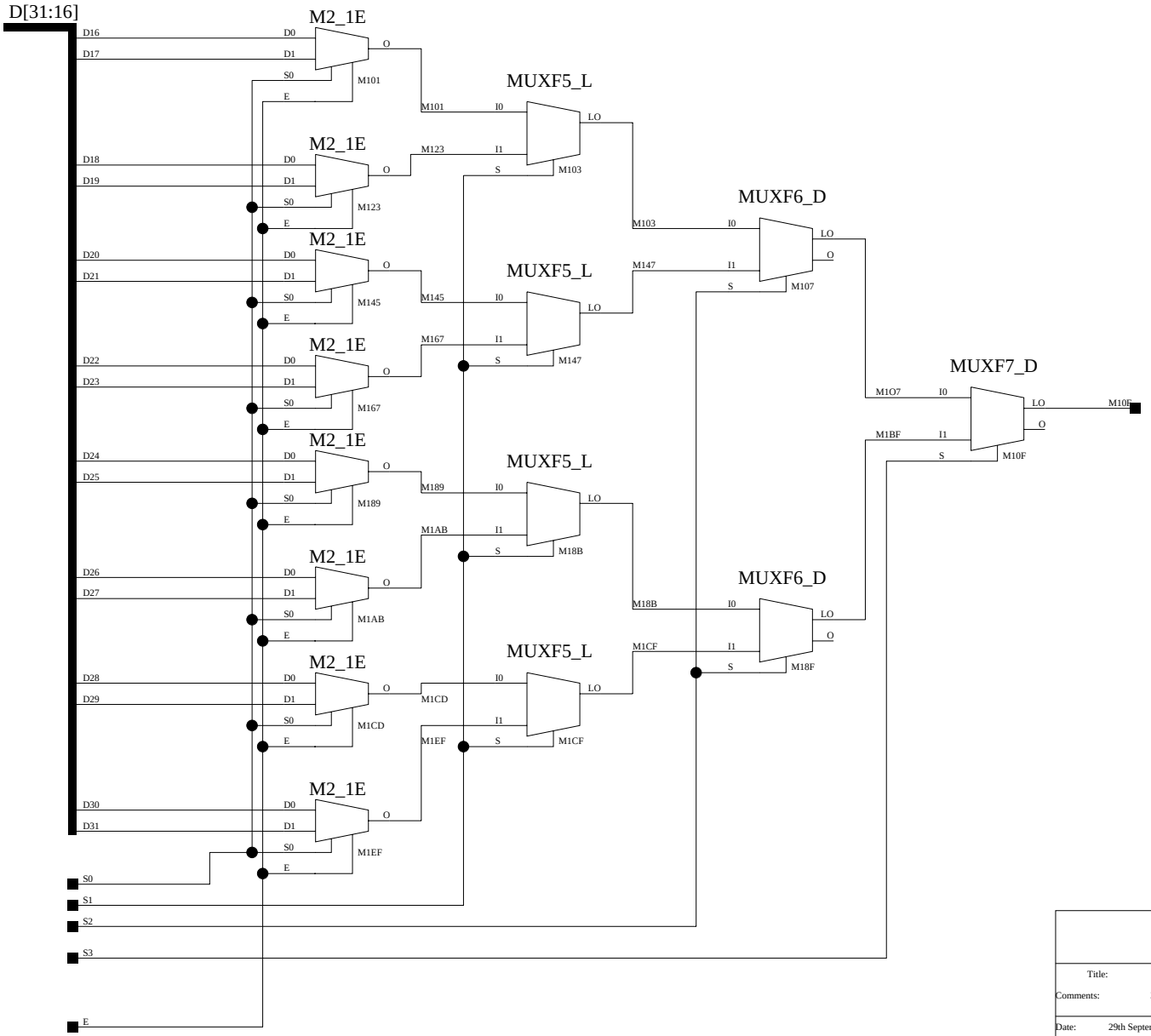
Title: VIRTEX Family OFDDR4 Macro

JRG

Comments: 4-Bit Output DDR Flip-Flop w/Asynchronous Clear and Clock Enable

Date:	16th December 2003	Ver:	1
Sheet Size: B		Rev:	A


D[31:16]
D[15:0]
D[31:0]
M2_1E
MUXF5_L
MUXF6_D
MUXF7_D
MUXF8_D
D0
D1
S0
E
O
M01
M23
M45
M67
M89
MAB
MCD
MEF
I0
I1
S
LO
M03
M47
M07
MO7
M8F
M0F
M10F
M8B
MCF
M010F
S[4:0]
S1
S2
S3
S4
Implements as a DPRAM (8 slices)
XILINX
JRG
Title: VIRTEX Family Fast M32E5bus Macro
Comments: 32-to-1 bussed Multiplexer with Enable
Date: 29th September 2003
Ver: 1
Sheet Size: B
Rev: A
drawn by KS
Copyright (c) 1993, Xilinx Inc.



drawn by KS

XILINX JRG

Title: VIRTEX Family Fast M32E5bus Macro

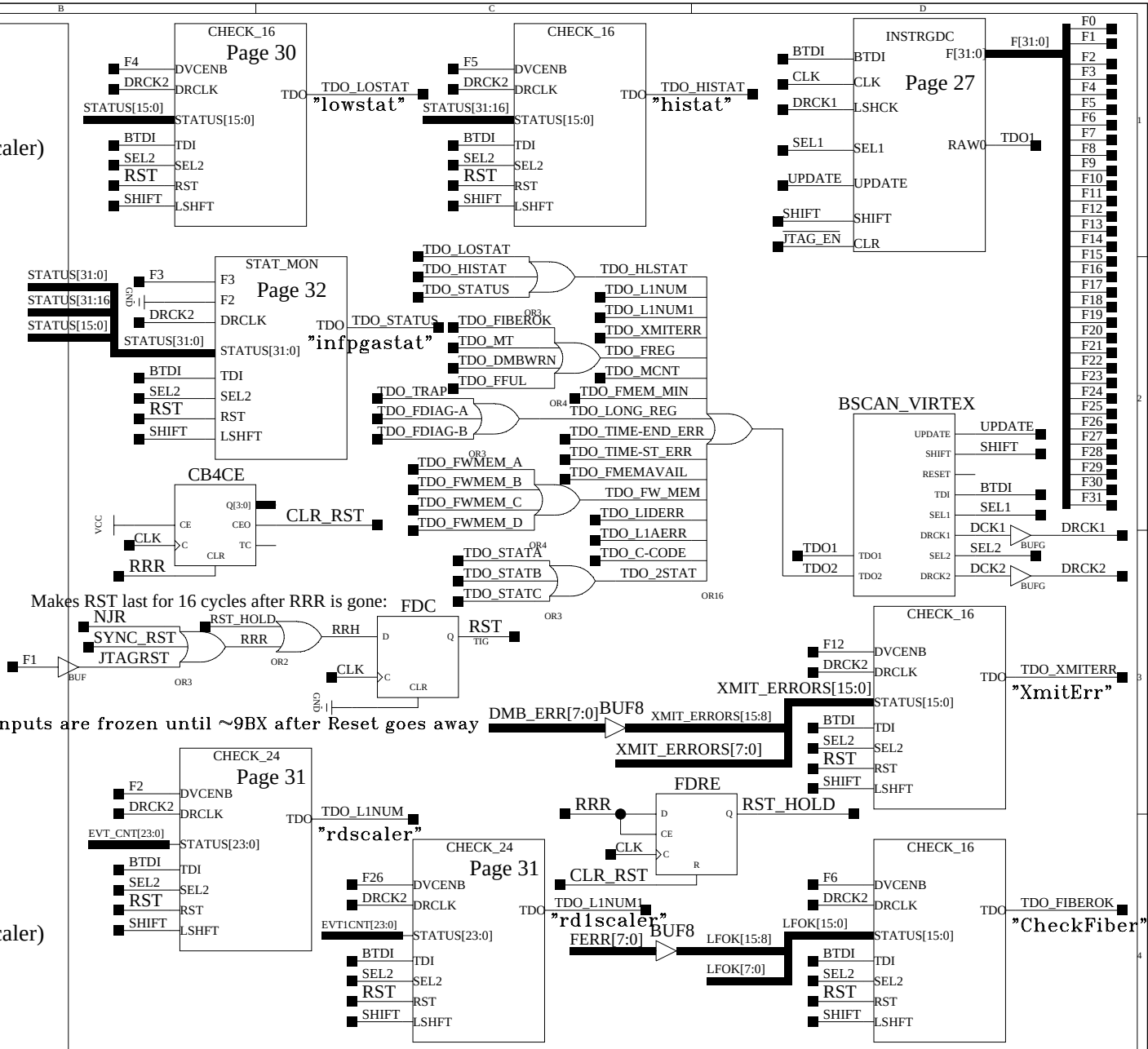
Comments: 32-to-1 bussed Multiplexer with Enable

Date: 29th September 2003 | Ver: 1

Sheet Size: B | Rev: A

JTAG Instruction Decode

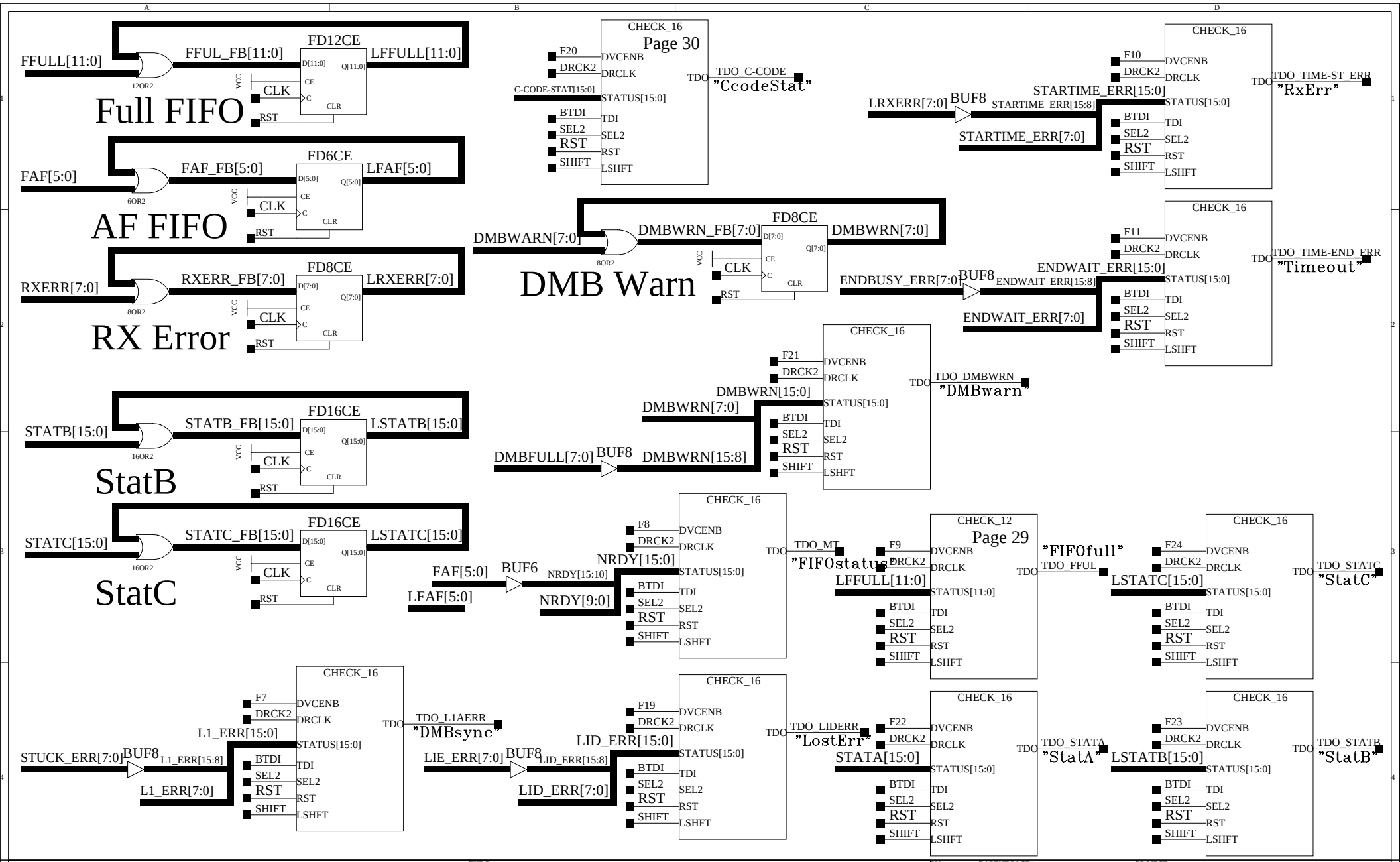
OpCode		Function [OpName]
	0	No Operation [NOOP]
	1	FPGA Reset [toggle]
	2	RdCtrl0 Current DDU L1A Number (24-bit scaler)
	3	Check status (capture and shift) [32 bits]
Old	4	Check status, low-word [16 bits]
Code	5	Check status, high-word [16 bits]
7	6a	Check FiberOK status (Check_FOK) [8 bits]
6	6b	Check FiberErr status (Check_Ferr) [8 bits]
11	7a	L1A Mismatch [8-bits]
26	7b	Stuck Buffer Errors [8-bits]
25	8a	FIFO Empty Status [10-bits]
20	8b	Almost Full FIFOs [6-bits]
21	9	Full FIFOs [12-bits]
13	10a	Timeout: start [8-bits]
17	10b	RX Errors [8-bits]
14	11a	Timeout: end-wait [8-bits]
15	11b	Timeout: end-active [8-bits]
12	12a	Data Xmit Errors [8-bits]
16	12b	DMB Errors [8-bits]
	13	Fiber 1 & 0 Write Memory [10-bits]
	14	Fiber 3 & 2 Write Memory [10-bits]
	15	Fiber 5 & 4 Write Memory [10-bits]
	16	Fiber 7 & 6 Write Memory [10-bits]
	17	FIFO Mem Available 1 & 0 [10-bits]
	18	FIFO Mem Min Available 1 & 0 [10-bits]
19	*19a	Lost In Data [8-bits]
18	*19b	Lost In Event [8-bits]
	20	C-Code Status [16-bits]
	21	DMB Warn/Full Status [16-bits]
22	22	Status Register A [16-bits]
23	23	Status Register B [16-bits]
24	24	Status Register C [16-bits]
	25	Diagnostic Trap [192-bits]
	26	RdCtrl1 Current DDU L1A Number (24-bit scaler)
	* 28	# Mem assigned to Fibers 2-0 [16-bits]
	* 30	Fiber 3-0 Mem Diagnostic [InRD0, 4 * 8-bits]
	* 31	Fiber 7-4 Mem Diagnostic [InRD1, 4 * 8-bits]



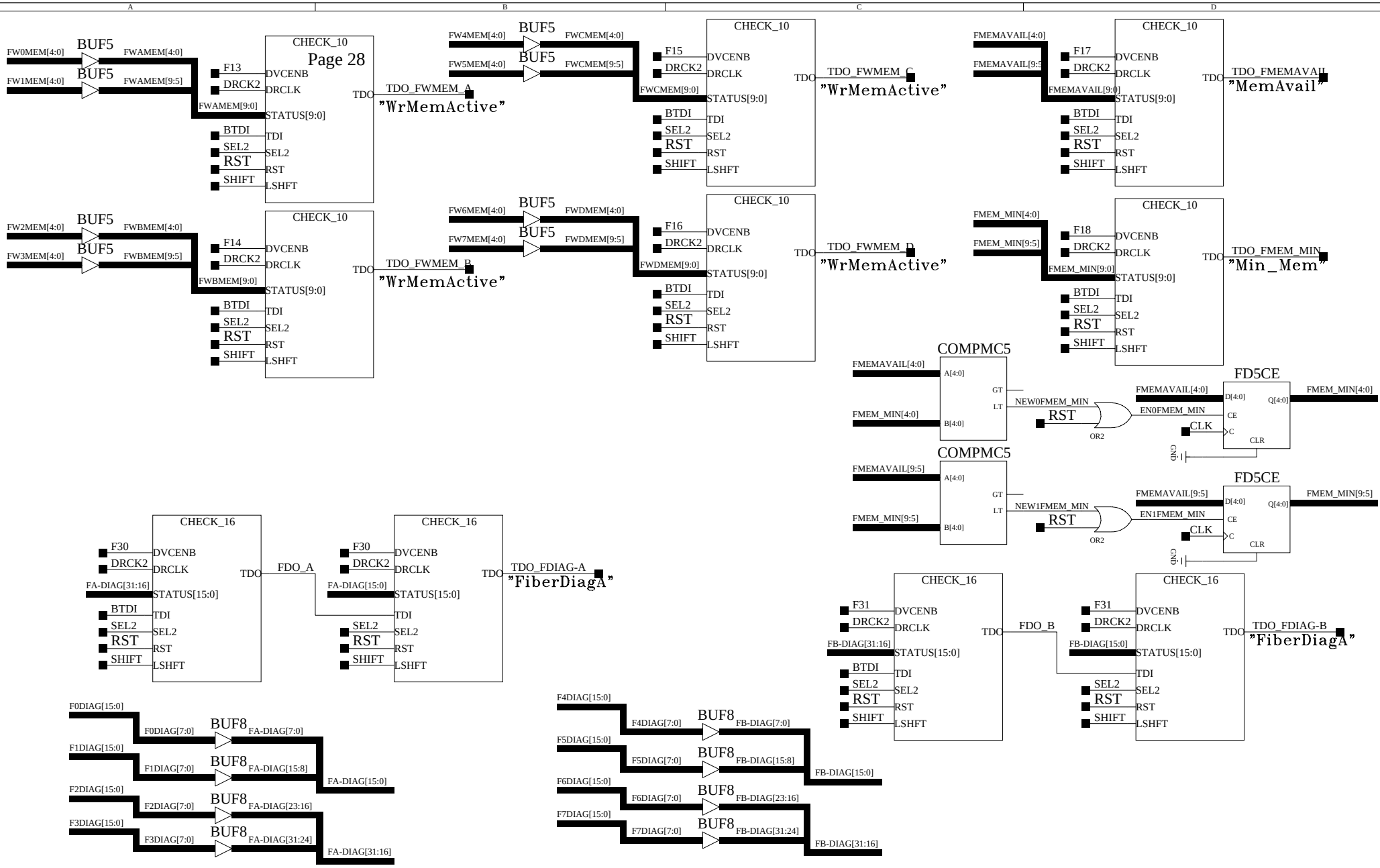
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: JTAG Status Monitor Signals
DDU Input Controller Logic
CMS CSC Electronics

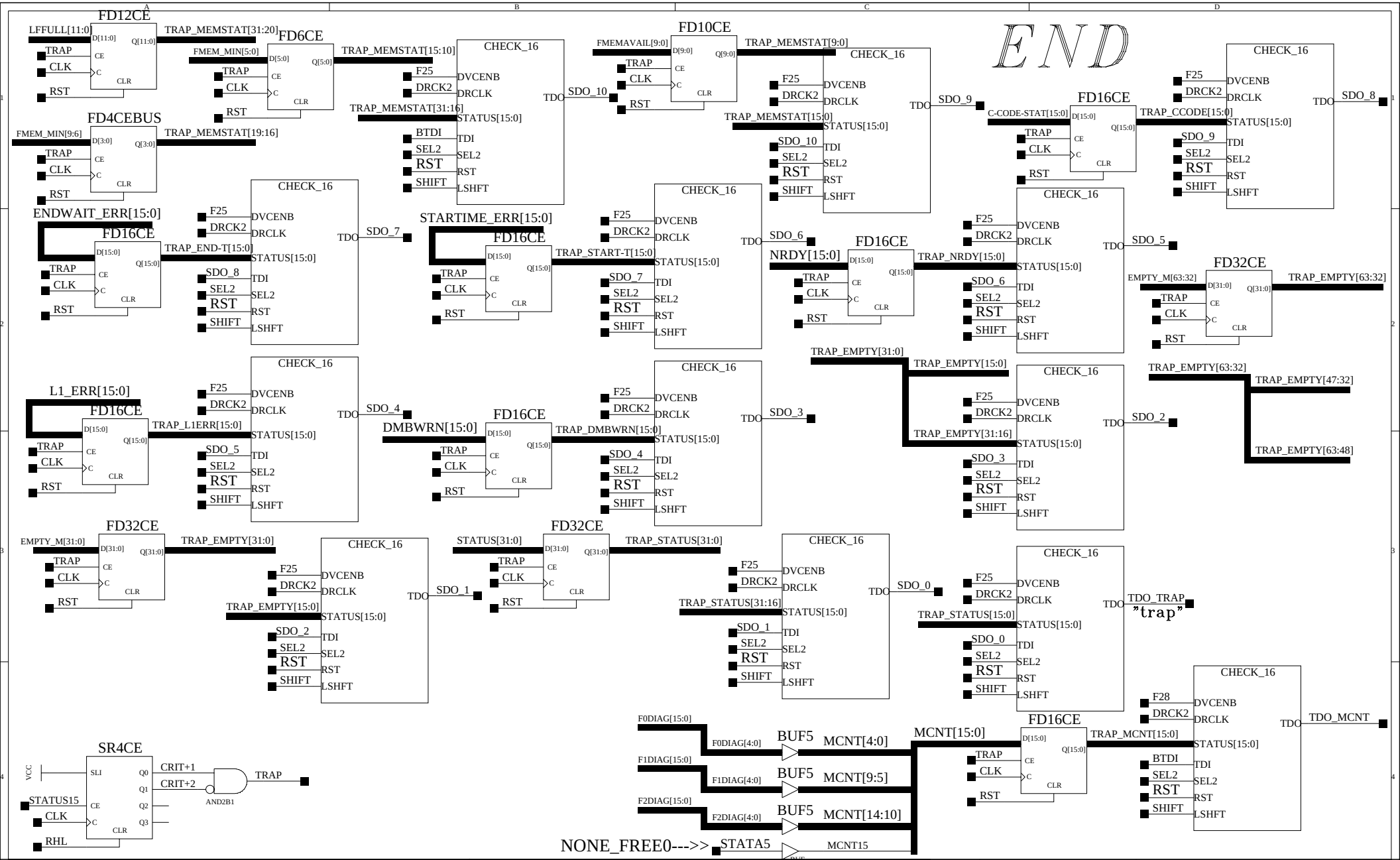
BY	PARENT PAGE	PROJECT
JRG	2A	D785
DATE	FILE	PAGE
12-7-2006_14:09	JTAG . 1	26



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Signals DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2A	PROJECT: D785
		DATE: 2-17-2006_10:23	FILE: JTAG . 2	PAGE: 26A

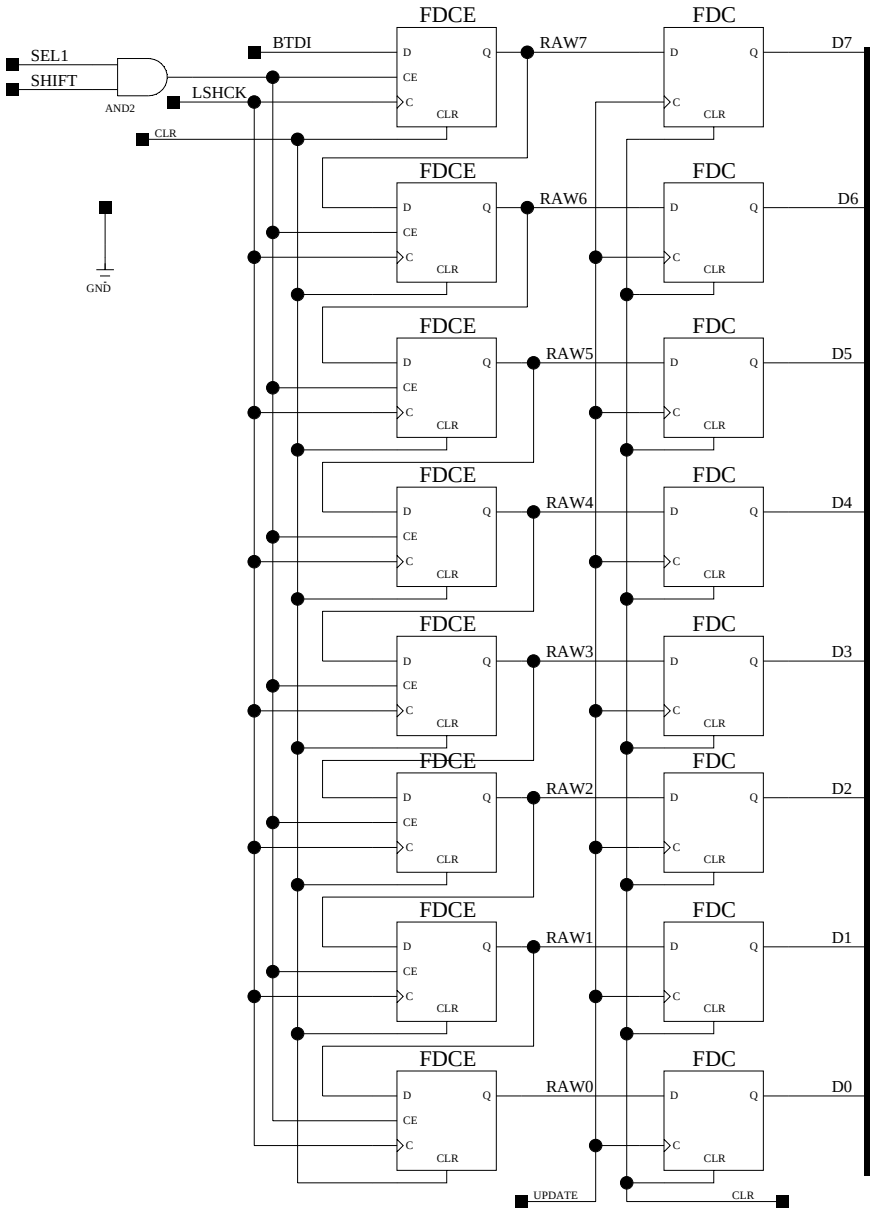


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Signals DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2A
		DATE: 3-10-2006_12:56	PROJECT: D785
		FILE: JTAG . 3	PAGE: 26B

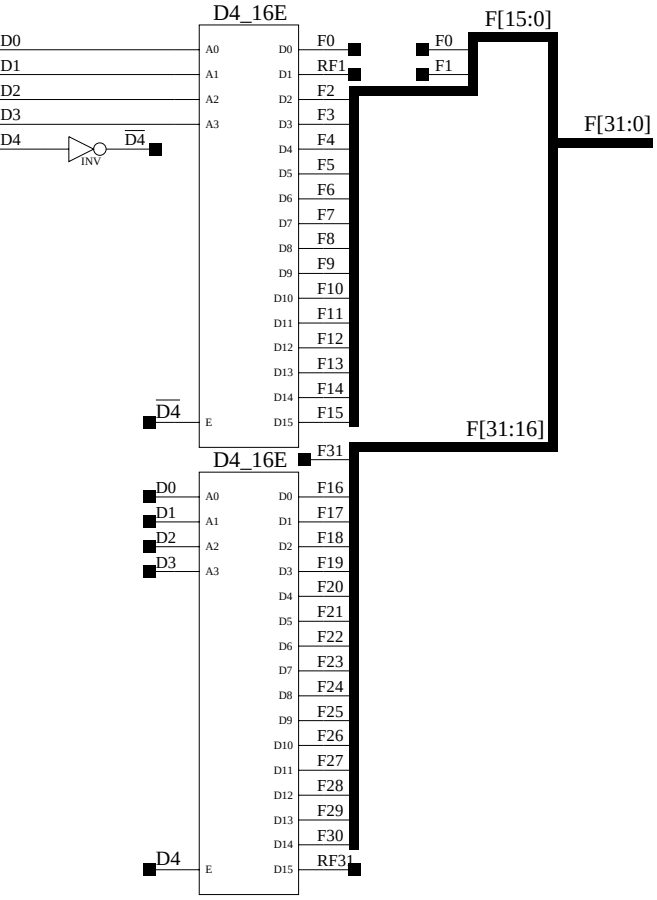


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Critical Error Trap DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2A	PROJECT D785
		DATE 2-17-2006_10:22	FILE JTAG . 4	PAGE 26C

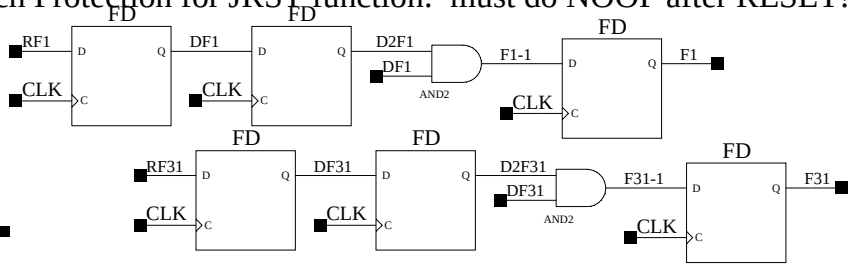
8 Bit Instruction Register



decode first 32 OpCodes (5 bits)

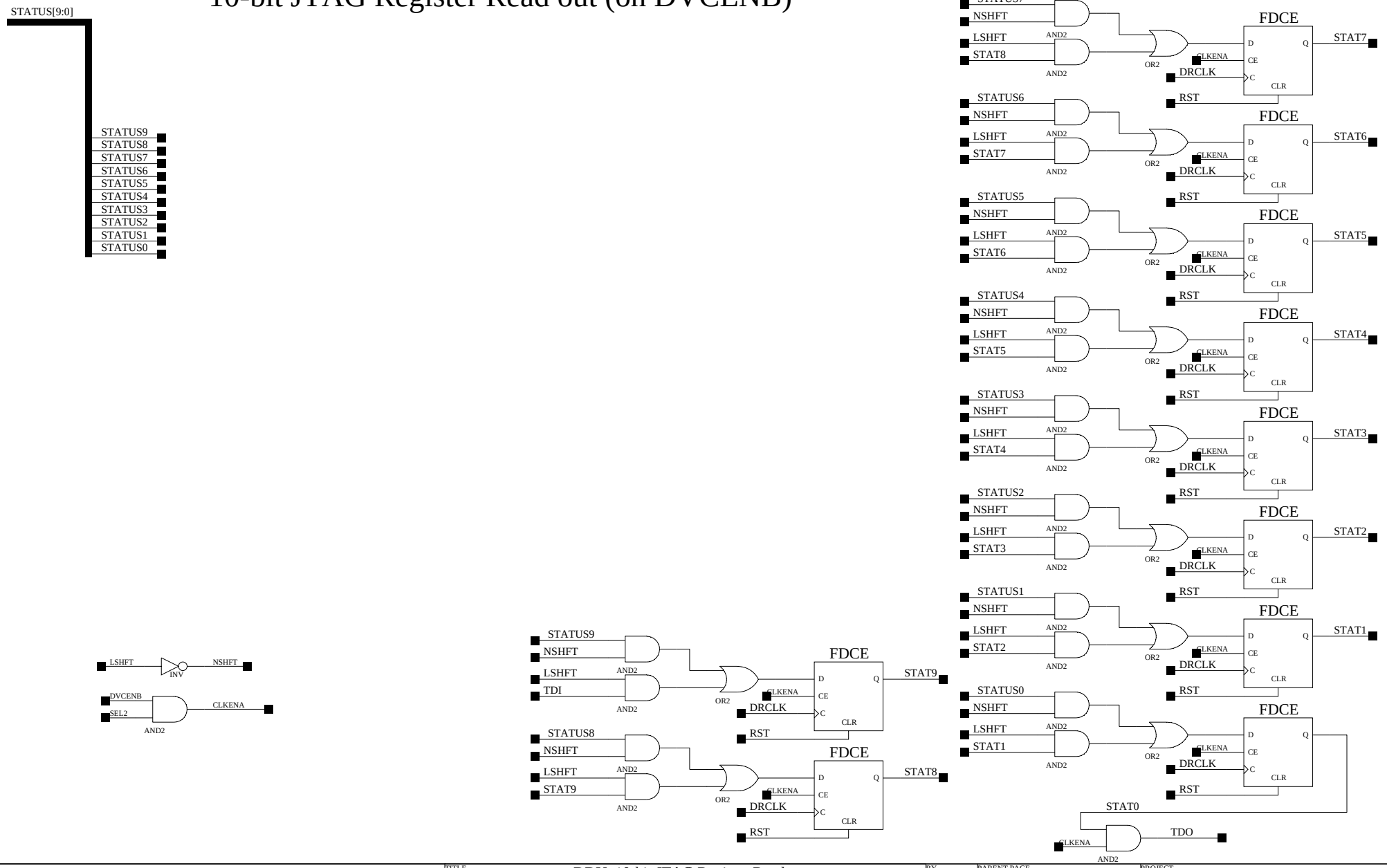


Glitch Protection for JRST function: must do NOOP after RESET!



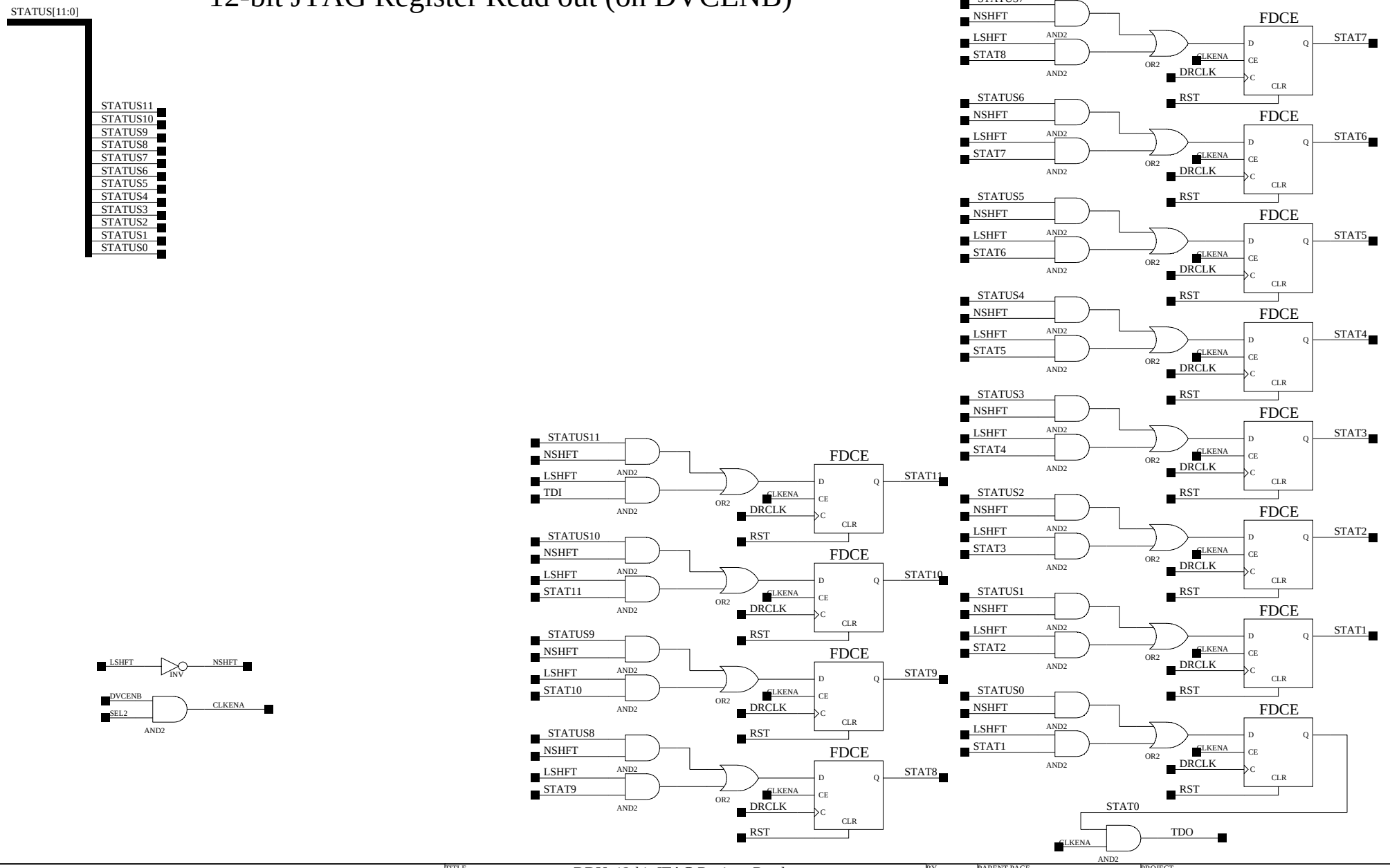
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Instruction Decode DDU Input Controller Logic CMS CSC ELECTRONICS	BY: JRG	PARENT PAGE: 26	PROJECT: D785D
		DATE: 1-27-2005_10:13	FILE: INSTRGDC . 1	PAGE: 27

10-bit JTAG Register Read out (on DVCENB)



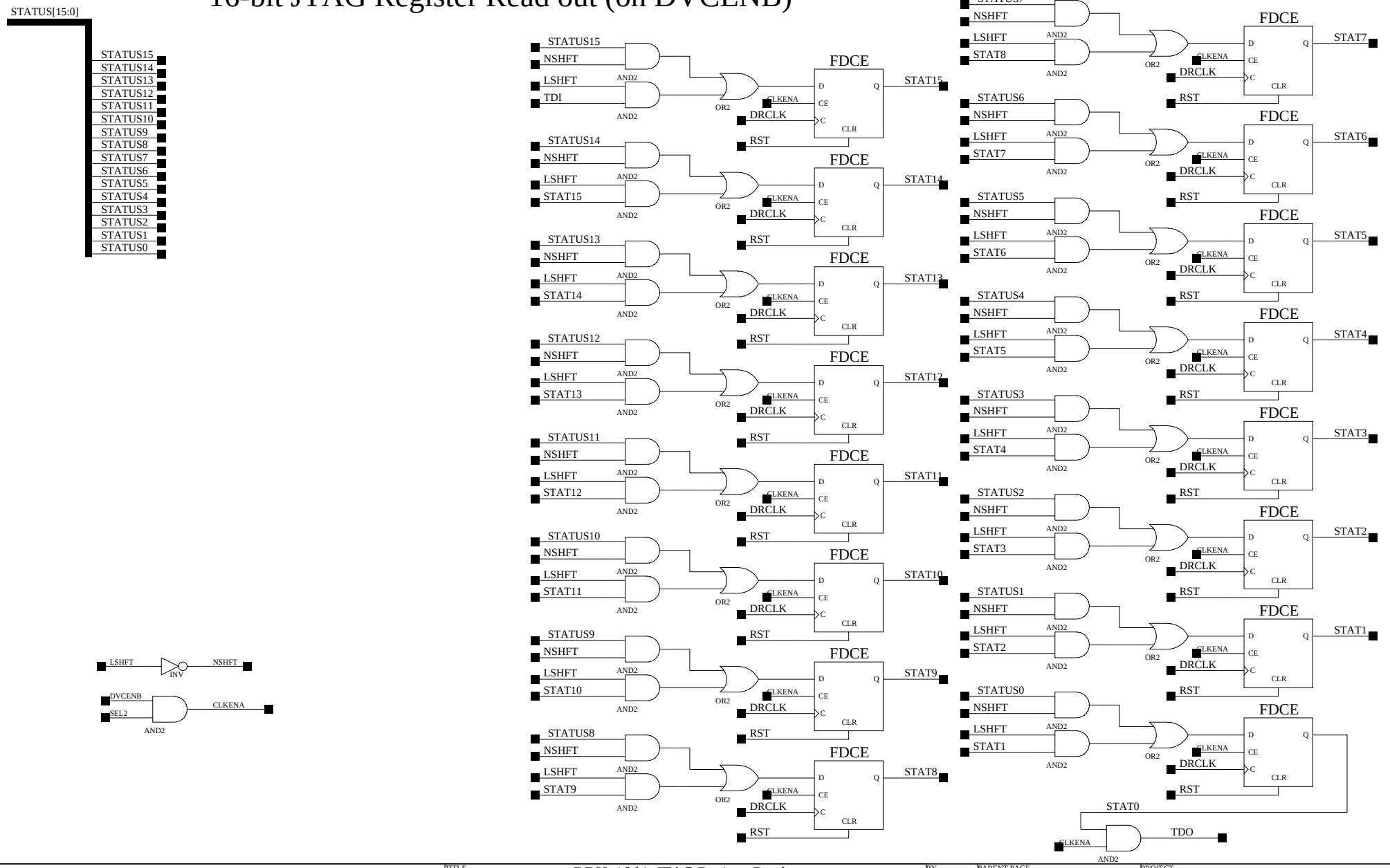
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 10-bit JTAG Register Readout DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26B	PROJECT: D785
		DATE: 1-27-2005_10:18	FILE: CHECK_10 . 1	PAGE: 28

12-bit JTAG Register Read out (on DVCENB)



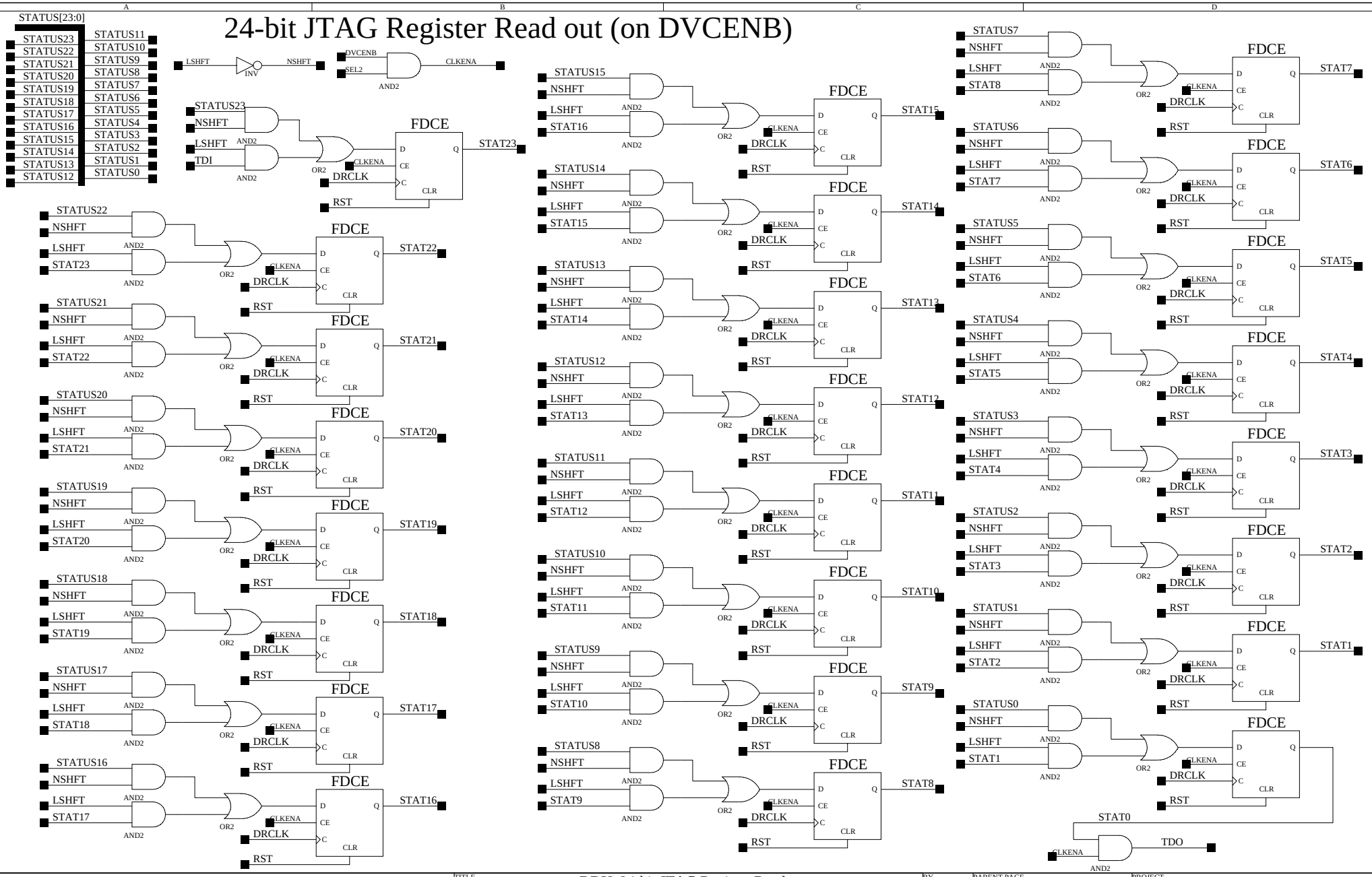
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 12-bit JTAG Register Readout DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26A	PROJECT: D785
		DATE: 1-27-2005_10:18	FILE: CHECK_12 . 1	PAGE: 29

16-bit JTAG Register Read out (on DVCENB)

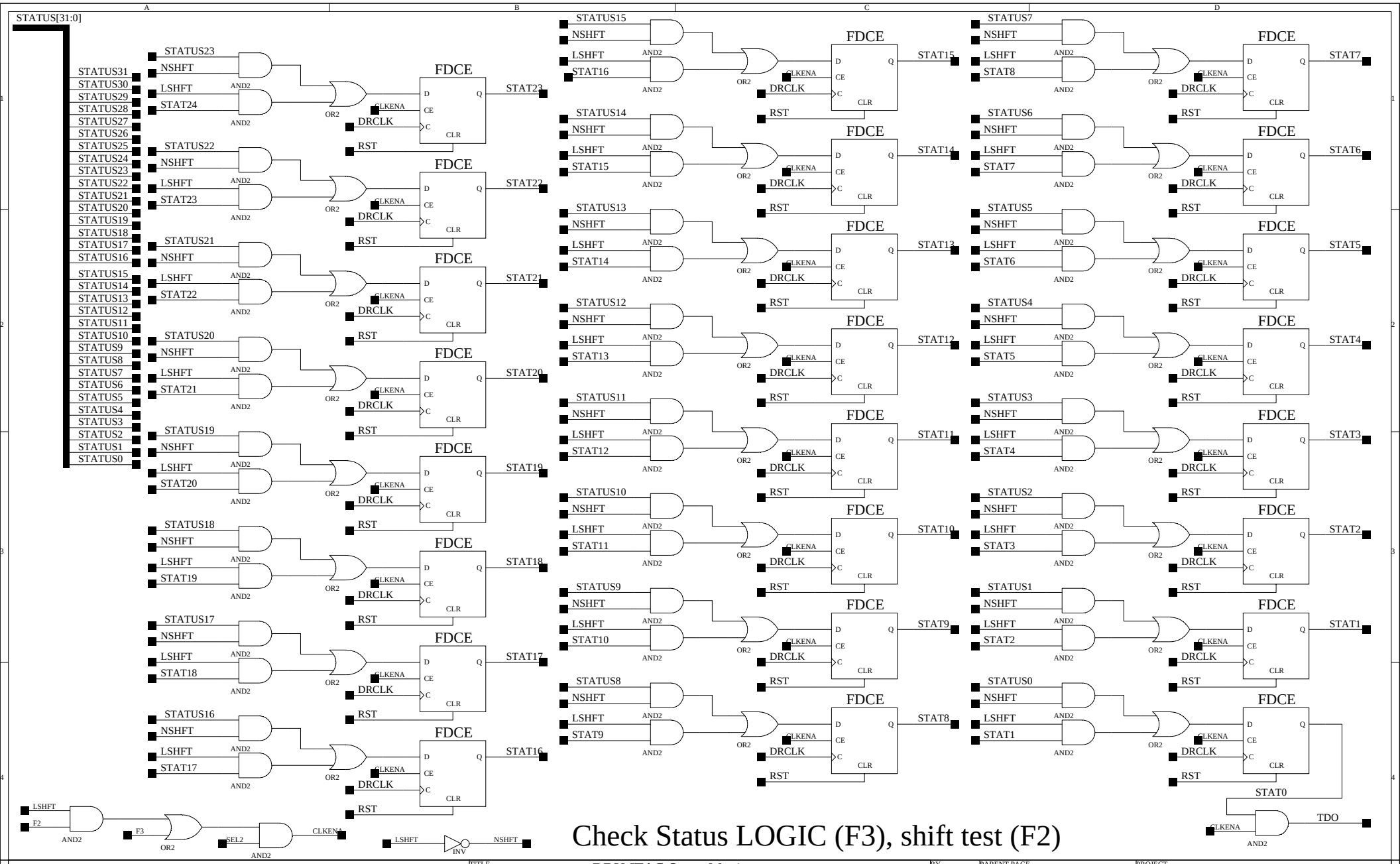


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 16-bit JTAG Register Readout DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26	PROJECT: D785
		DATE: 11-8-2005_16:02	FILE: CHECK_16 . 1	PAGE: 30

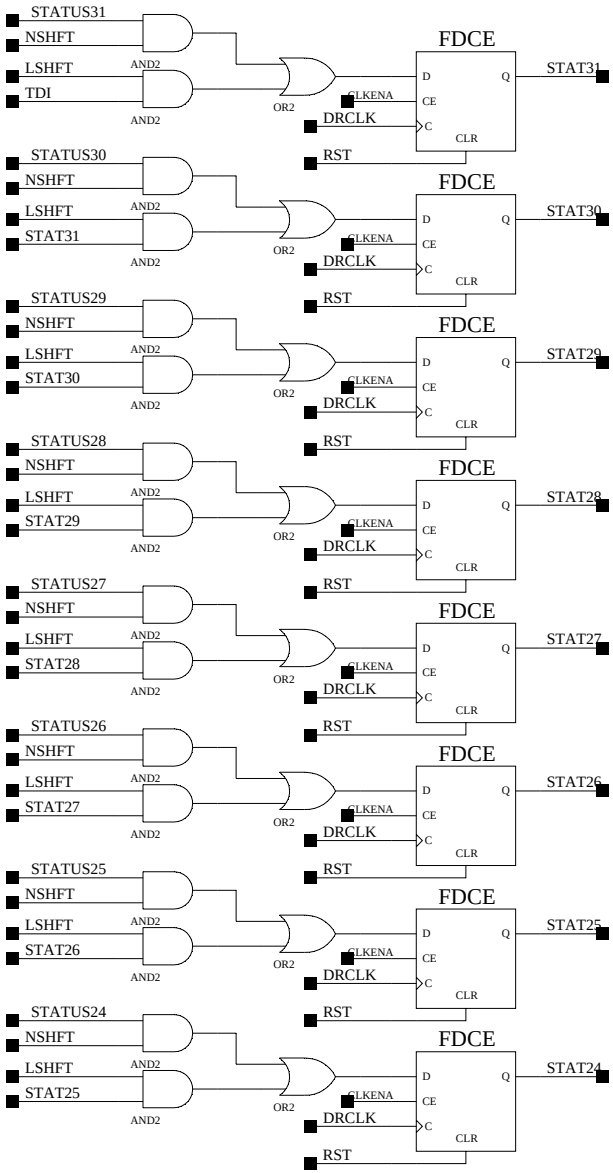
24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26	PROJECT: D785D
		DATE: 1-27-2005_10:19	FILE: CHECK_24_1	PAGE: 31



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26	PROJECT: D785
		DATE: 1-27-2005_10:20	FILE: STAT_MON_1	PAGE: 32



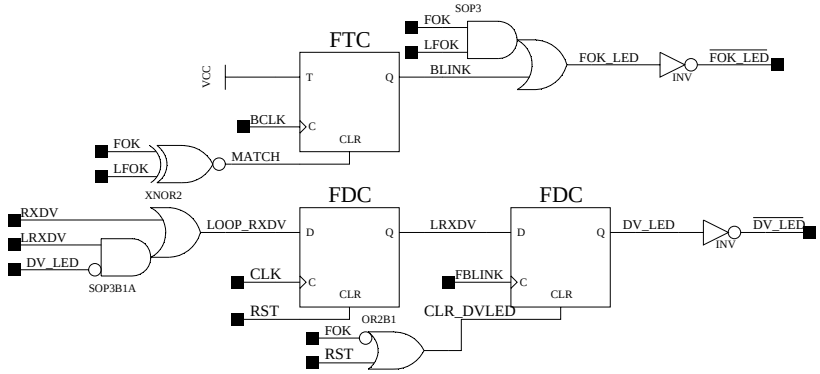
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU JTAG Status Monitor DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 26	PROJECT: D785D	
		DATE: 1-27-2005_10:20		FILE: STAT_MON_2	PAGE: 32A

FOK LED

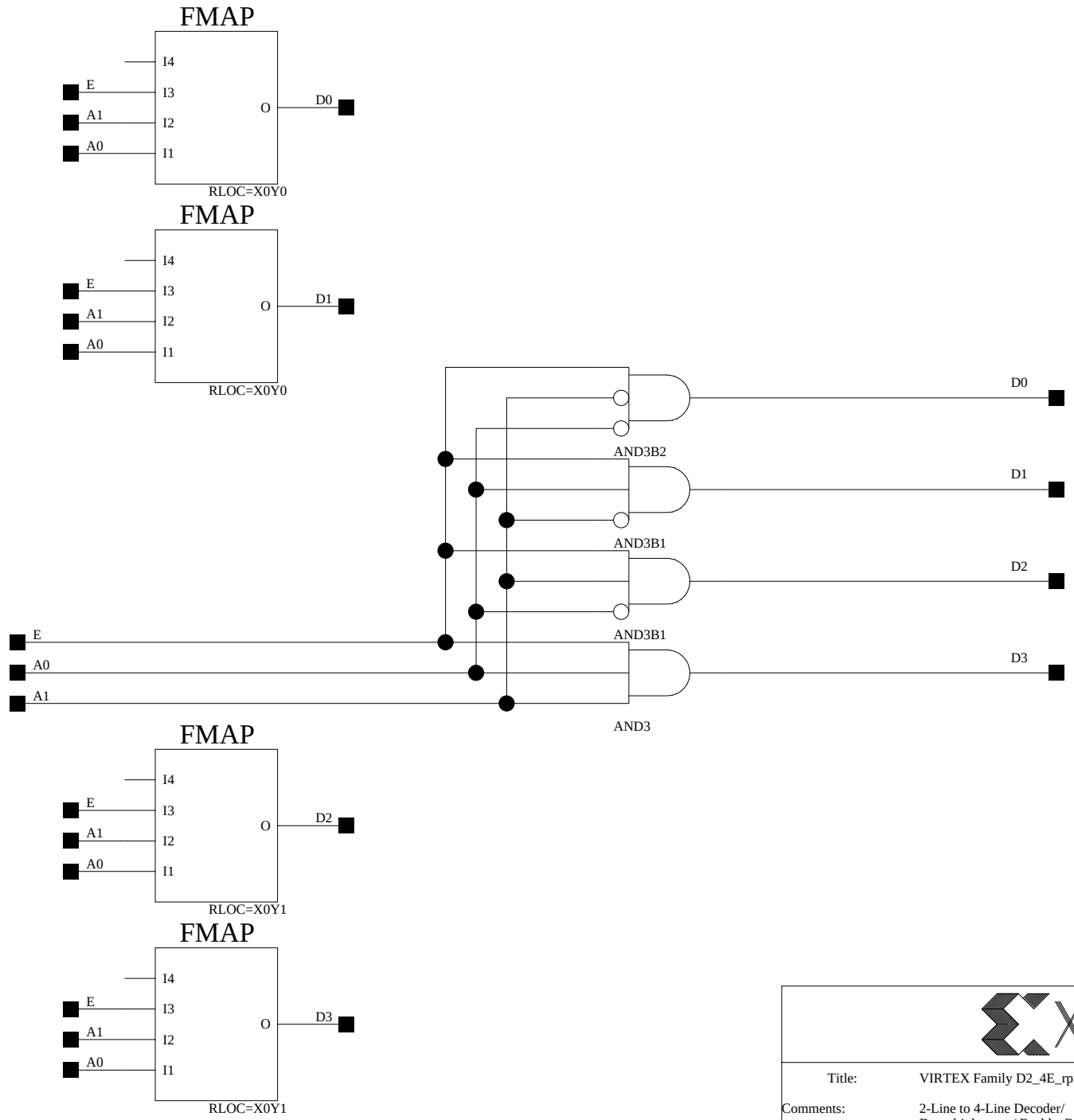
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED

--LIT == Active Data Xmit
--OFF == No data to Xmit

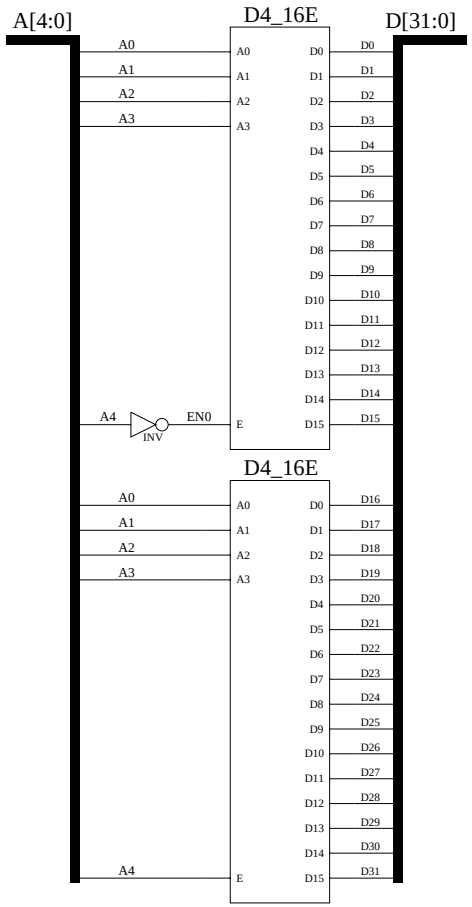


XILINX			JRG
Title:	FIBERLED		
Comments:	Custom LED Slow-Blink Control for Fiber Inputs		
Date:	27th January 2004	Ver:	1
Sheet Size: B		Rev:	A



XILINX			JRG
Title:	VIRTEX Family D2_4E_rpm Macro		
Comments:	2-Line to 4-Line Decoder/ Demultiplexer w/ Enable, RPM		
Date:	11th November 2003	Ver:	1
Sheet Size: A		Rev:	A

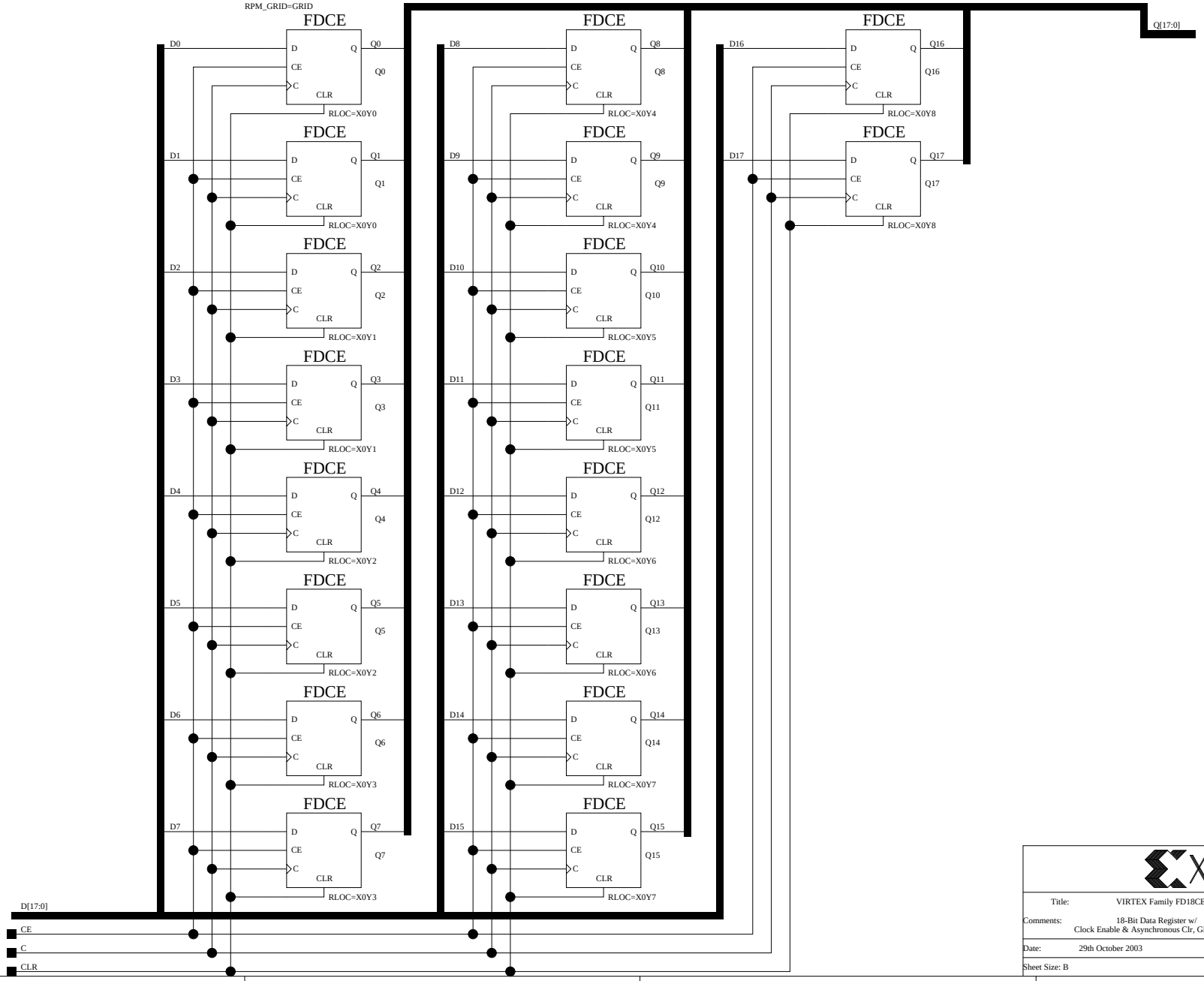
drawn by KS



XILINX

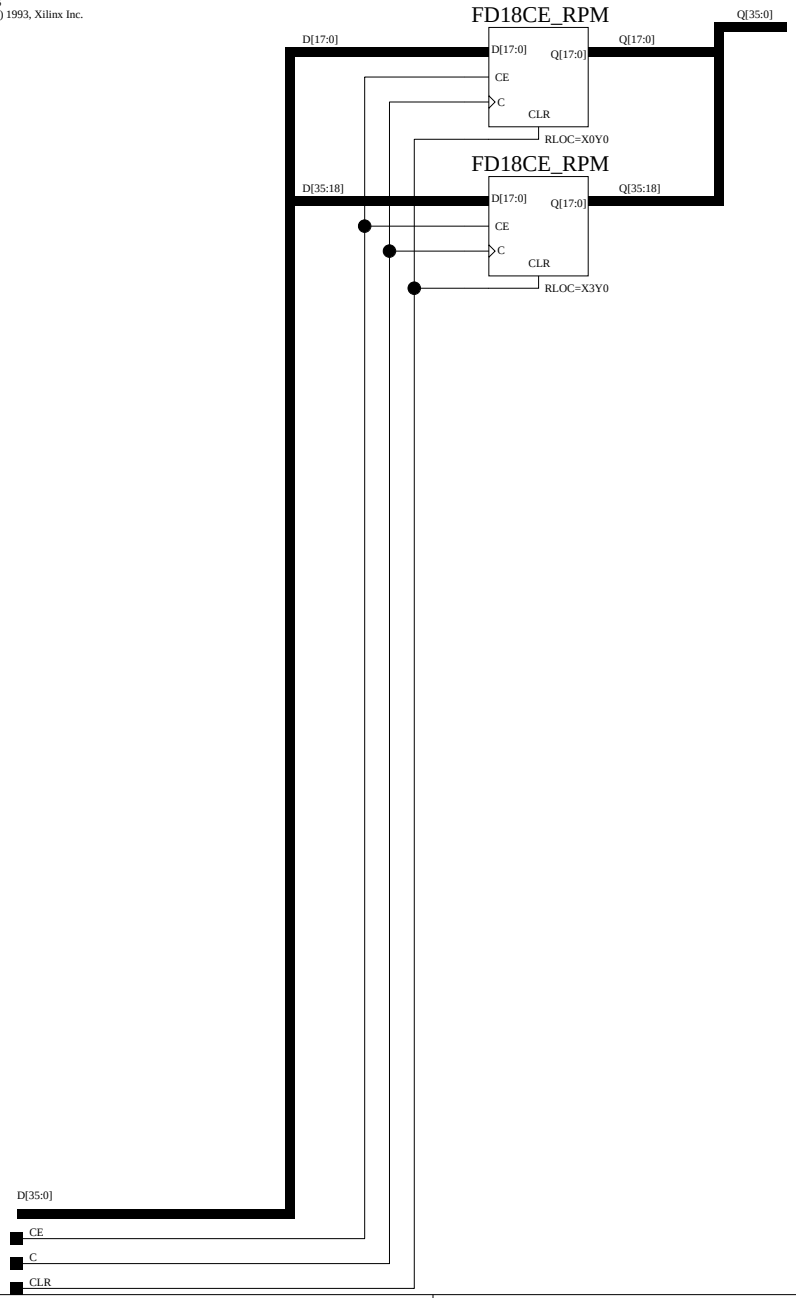
Title:	VIRTEX Family Decode 32E Macro		
Comments:	5-bit to 32-bit Decoder	JRG	
Date:	30th September 2003	Ver:	1
Sheet Size: B		Rev:	A

RPM_GRID=GRID



Title:	VIRTEX Family FD18CE_RPM Macro		JRG
Comments:	18-Bit Data Register w/ Clock Enable & Asynchronous Clr, GRID Coords X0Y0-X0Y8		
Date:	29th October 2003	Ver:	1
Sheet Size: B		Rev:	A

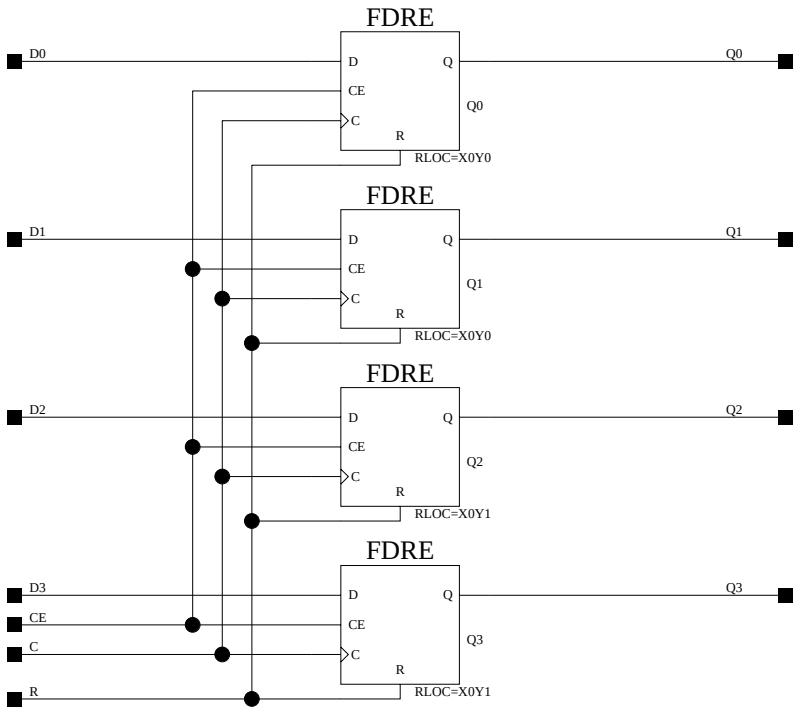
drawn by KS



XILINX

Title:	VIRTEX Family FD36CE_RPM Macro
Comments:	36-Bit Data Register w/ Clock Enable & Asynchronous Clr, GRID Coords X0Y0-X3Y8
Date:	30th October 2003
Ver:	1
Sheet Size: B	Rev: A

JRG

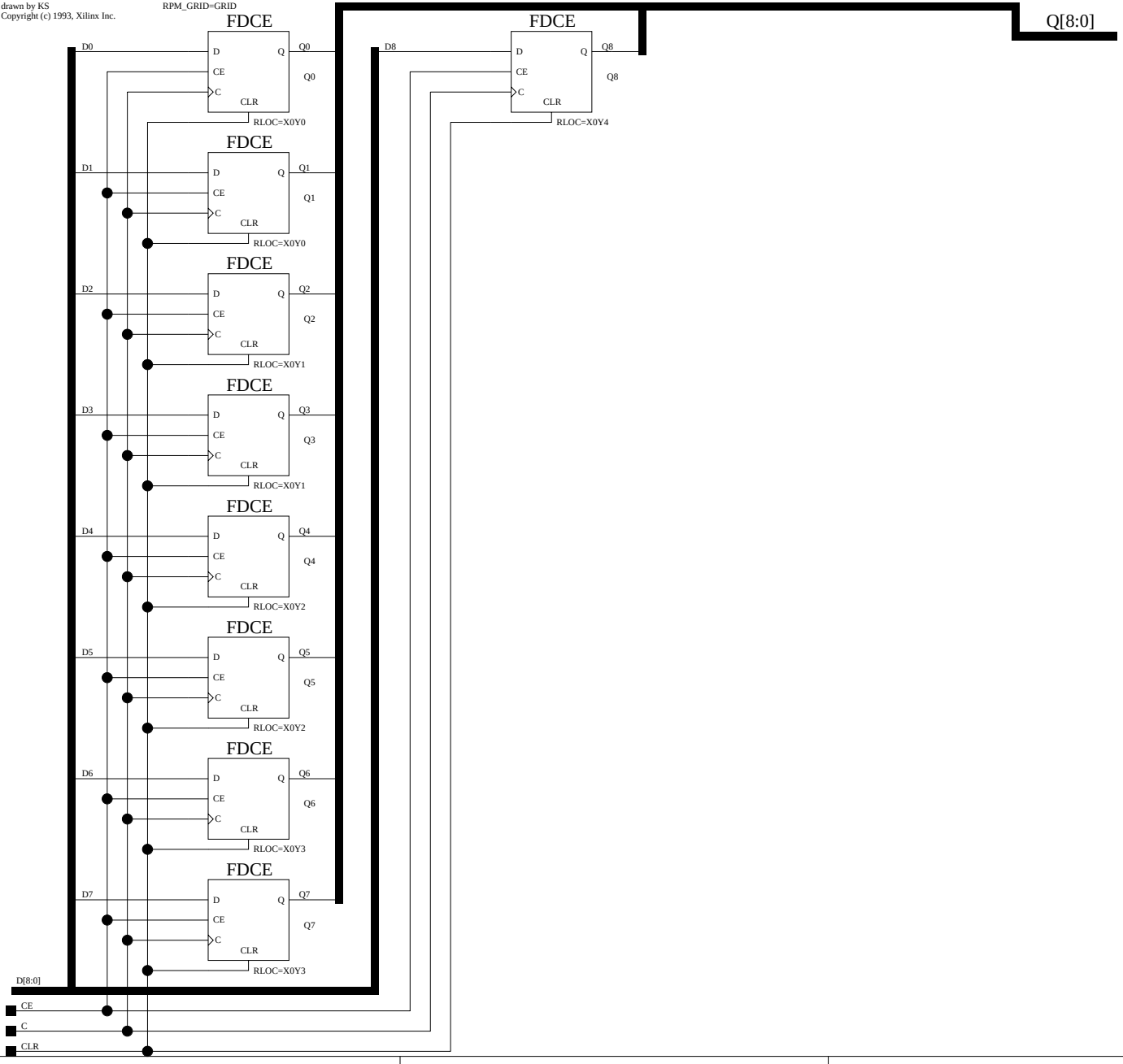


XILINX JRG

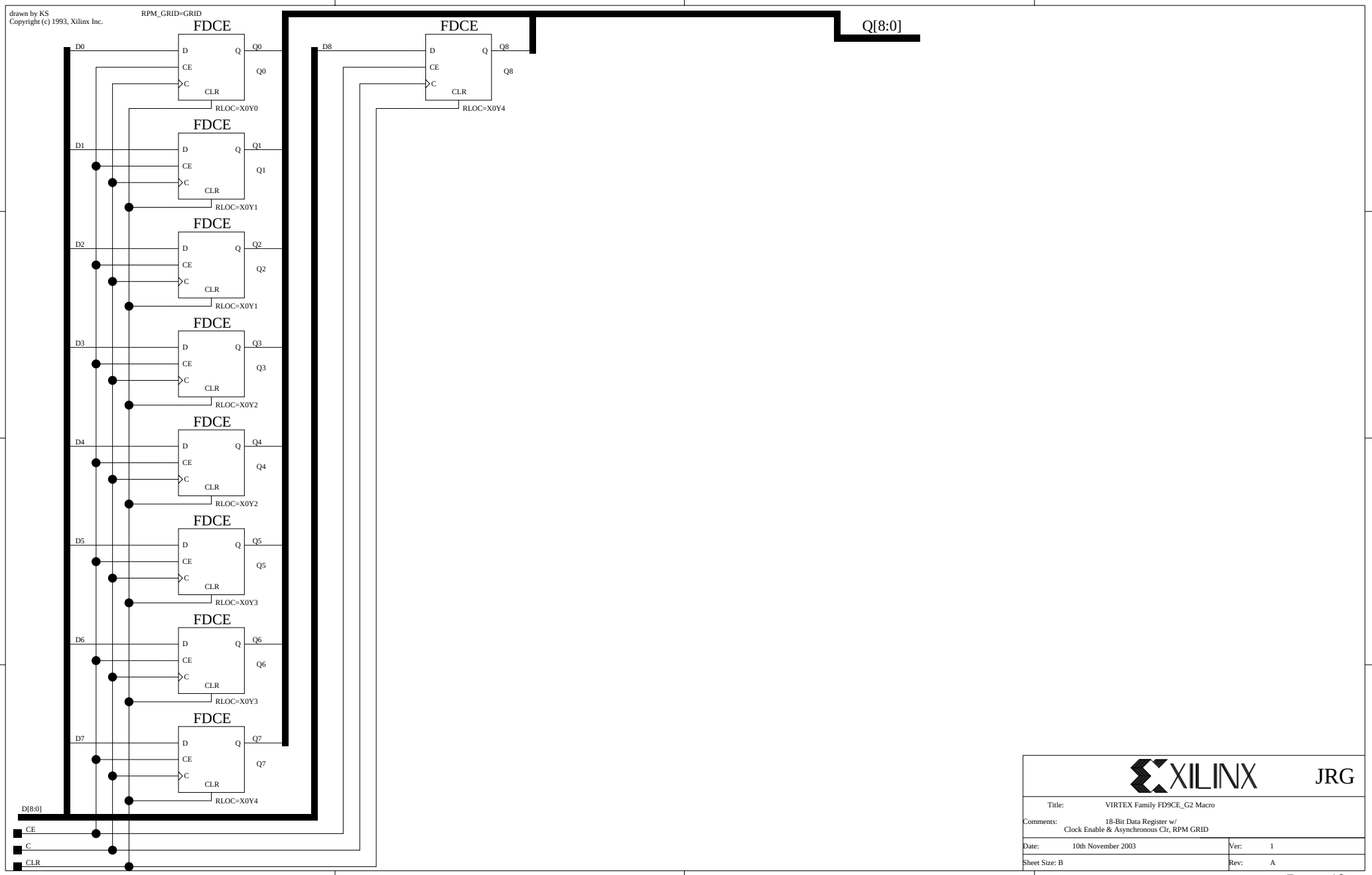
Title:	VIRTEX Family FD4RE Macro		
Comments:	4-Bit Data Register w/ Clock Enable & Sync Reset, RPM coords X0Y0.		
Date:	4th November 2003	Ver:	1
Sheet Size: A		Rev:	A

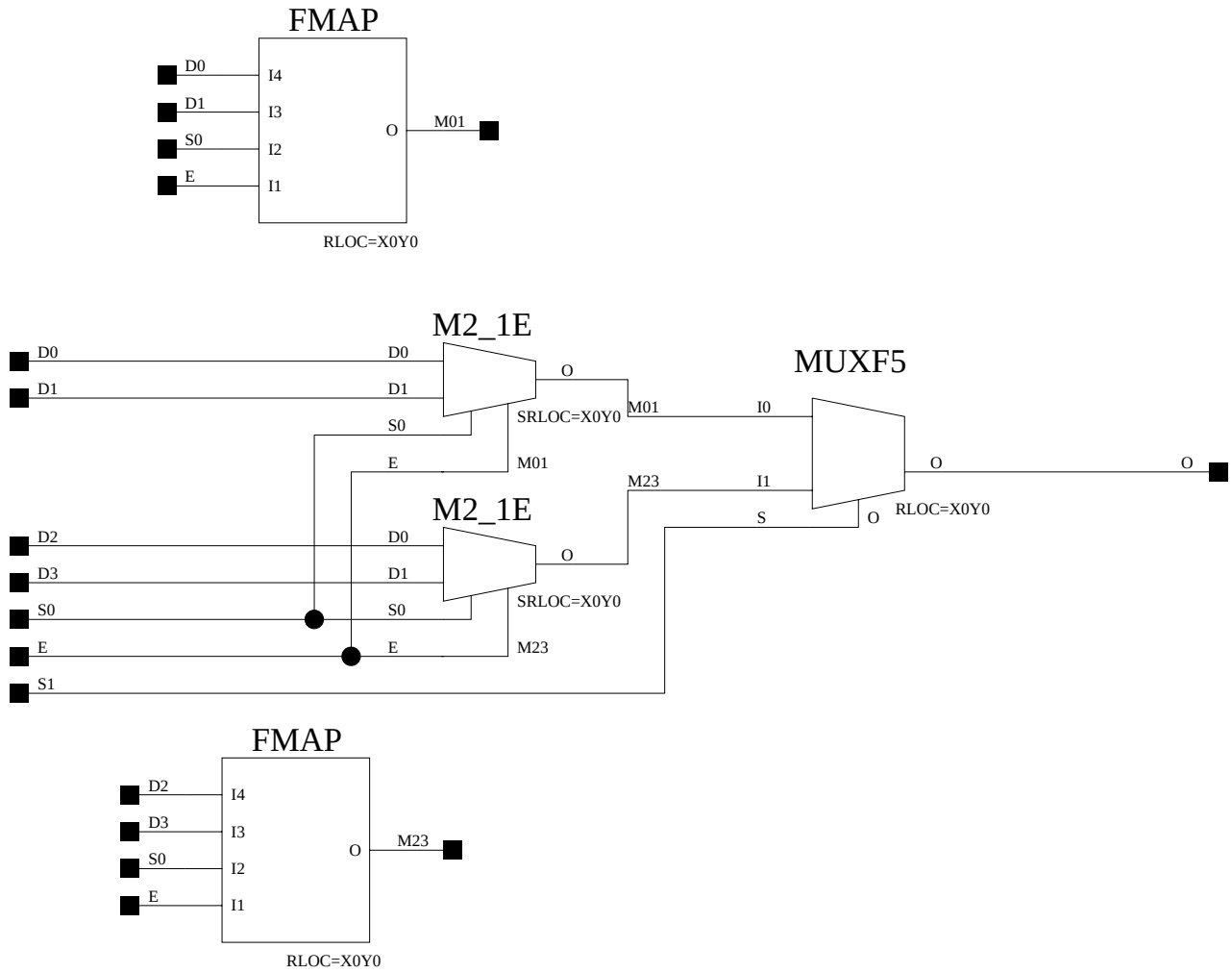
drawn by KS

RPM_GRID=GRID



XILINX			JRG
Title:	VIRTEX Family FD9CE_G Macro		
Comments:	18-Bit Data Register w/ Clock Enable & Asynchronous Clr, RPM GRID		
Date:	10th November 2003	Ver:	1
Sheet Size: B		Rev:	A

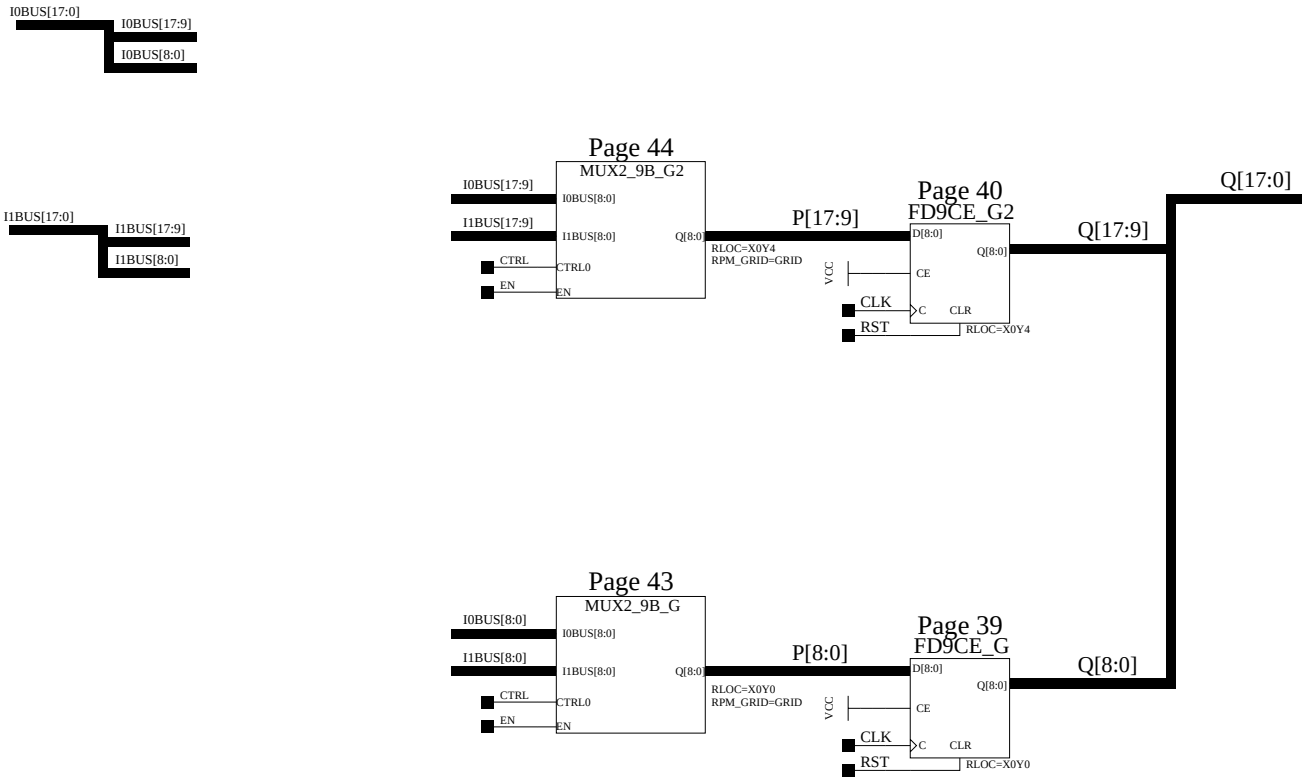

drawn by KS
Copyright (c) 1993, Xilinx Inc.
RPM_GRID=GRID
FDCE
D0
Q0
RLOC=X0Y0
D1
Q1
RLOC=X0Y1
D2
Q2
RLOC=X0Y1
D3
Q3
RLOC=X0Y2
D4
Q4
RLOC=X0Y2
D5
Q5
RLOC=X0Y3
D6
Q6
RLOC=X0Y3
D7
Q7
RLOC=X0Y4
D8
Q8
RLOC=X0Y4
D
CE
C
CLR
Q
Q[8:0]
D[8:0]
CE
C
CLR
XILINX
JRG
Title: VIRTEX Family FD9CE_G2 Macro
Comments: 18-Bit Data Register w/
Clock Enable & Asynchronous Clr, RPM GRID
Date: 10th November 2003
Ver: 1
Sheet Size: B
Rev: A



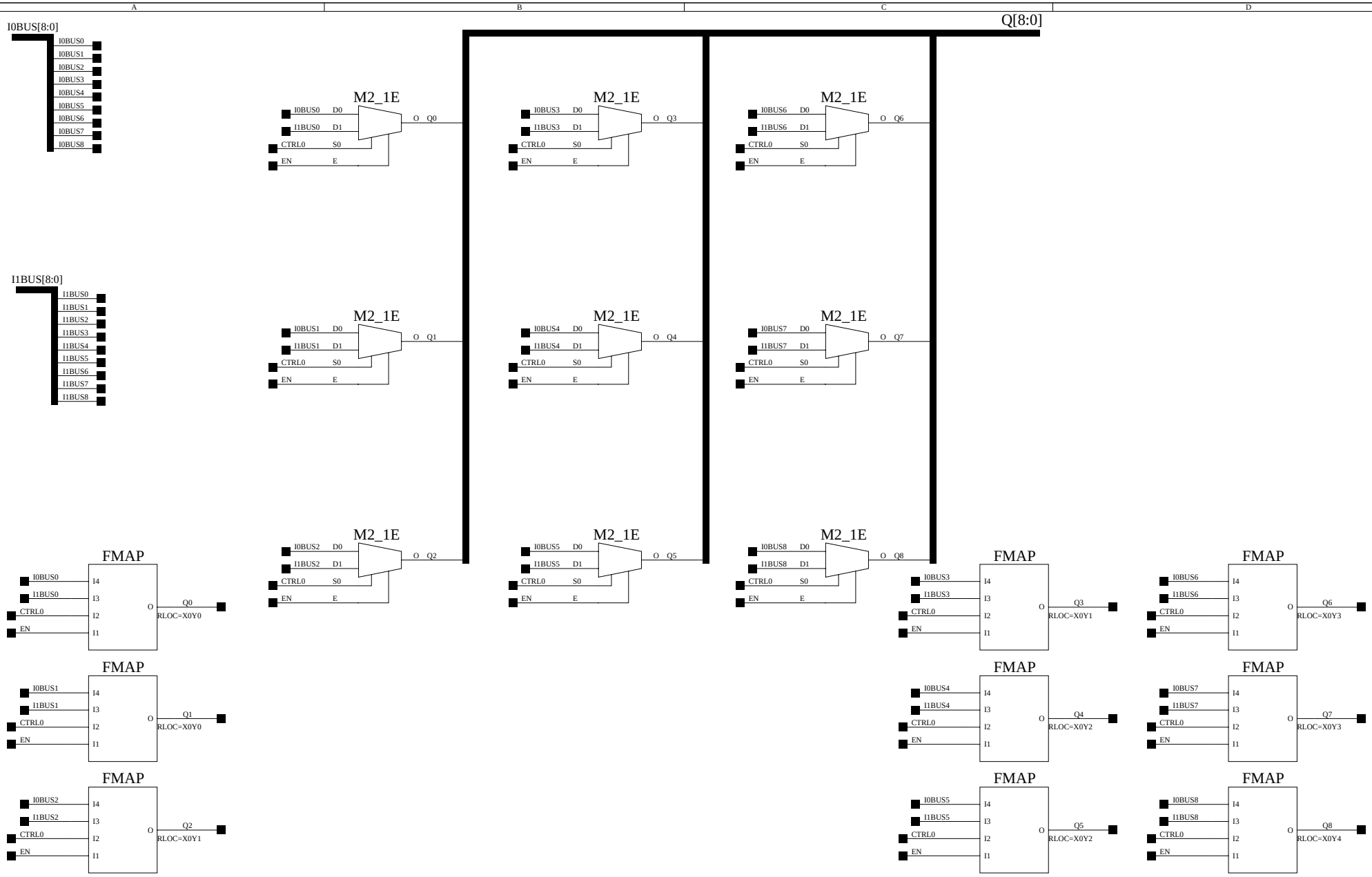
drawn by KS

XILINX JRG

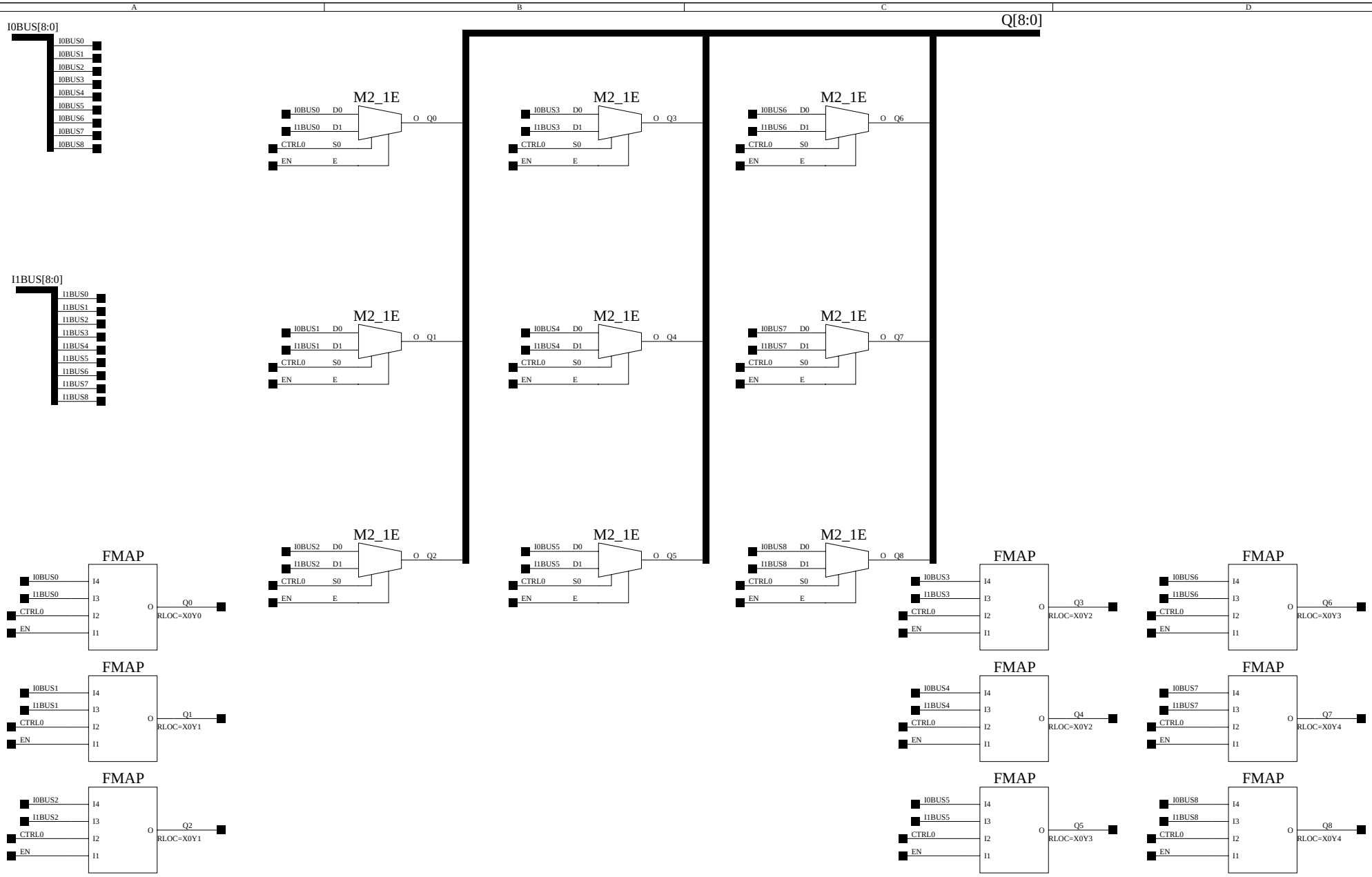
Title:	VIRTEX Family M4_1E_RPM Macro		
Comments:	4-to-1 Multiplexer with Enable		
Date:	31st October 2003	Ver:	1
Sheet Size: A		Rev:	B



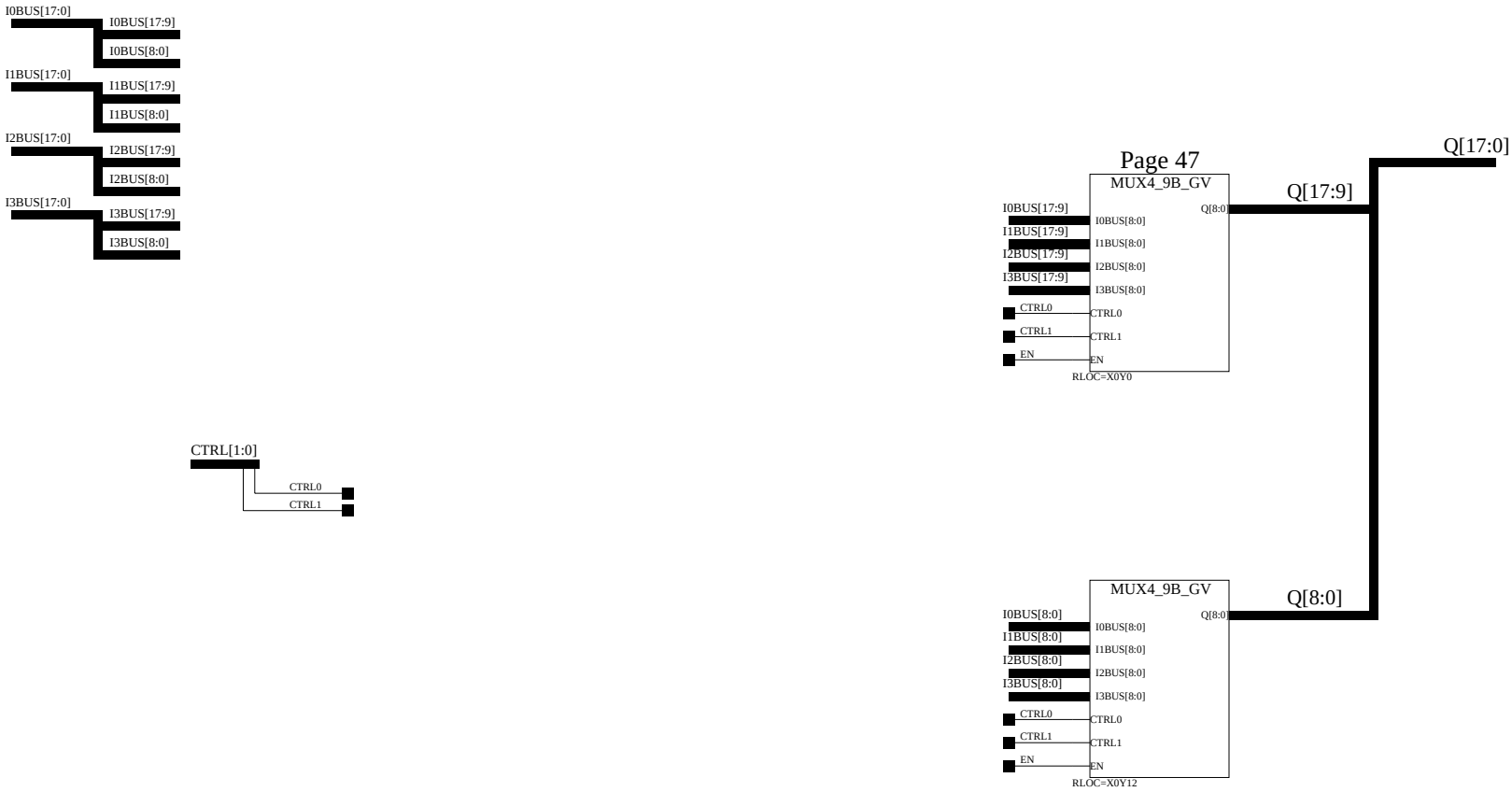
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Registered 18-bit MUX for 2 18-bit Inputs, w/Enable, RLOC=GRID Virtex MUX logic CMS CSC Electronics	BY JRG	PARENT PAGE 3A, 4A	PROJECT D785D
			DATE 7-18-2005_15:28	FILE MUX2_18B_REG . 1	PAGE 42



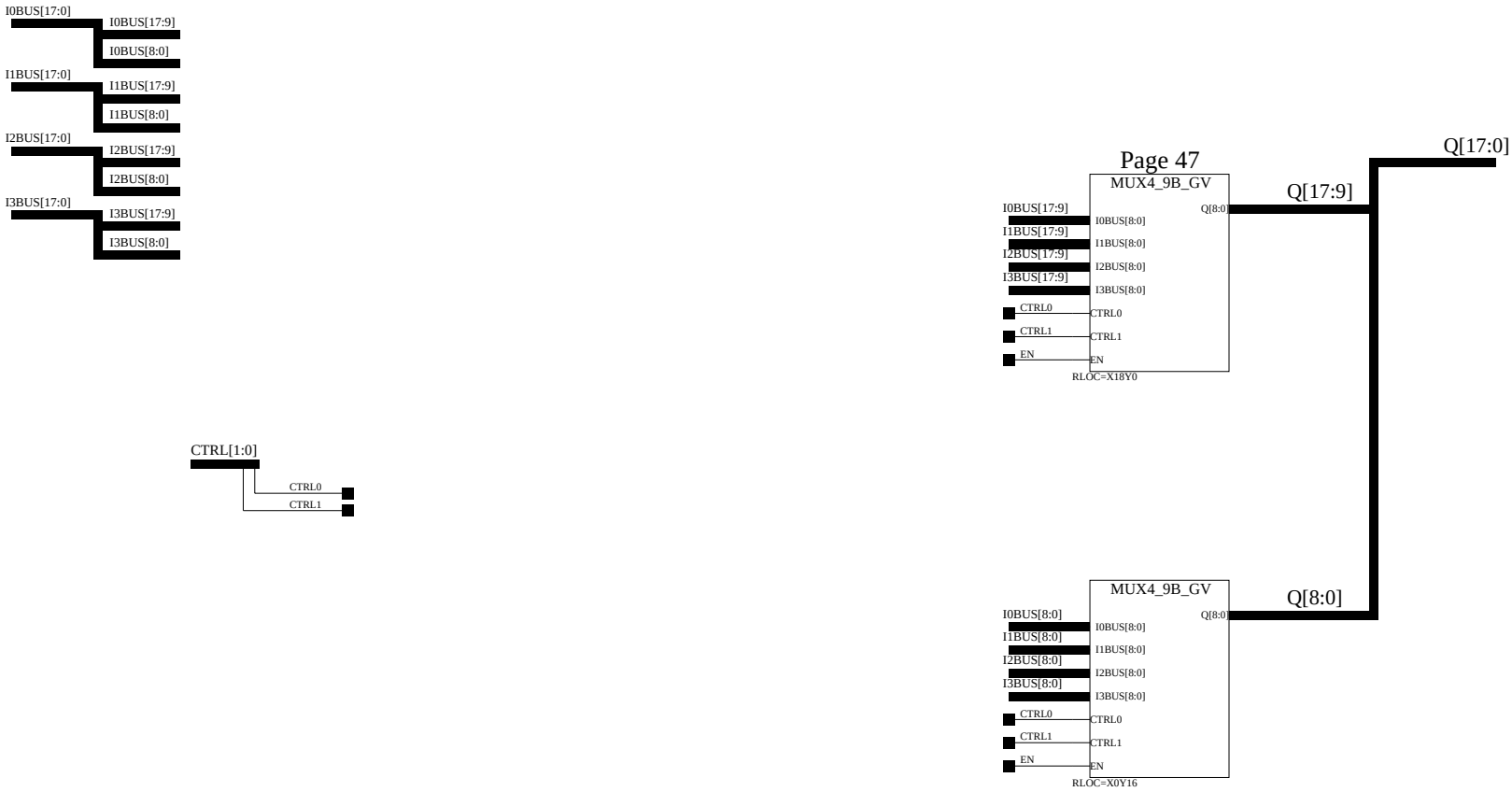
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 9-bit MUX for 2 9-bit Inputs, w/Enable. RLOC=GRID DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 42	PROJECT: D785D
		DATE: 1-27-2005_10:43	FILE: MUX2_9B_G . 1	PAGE: 43



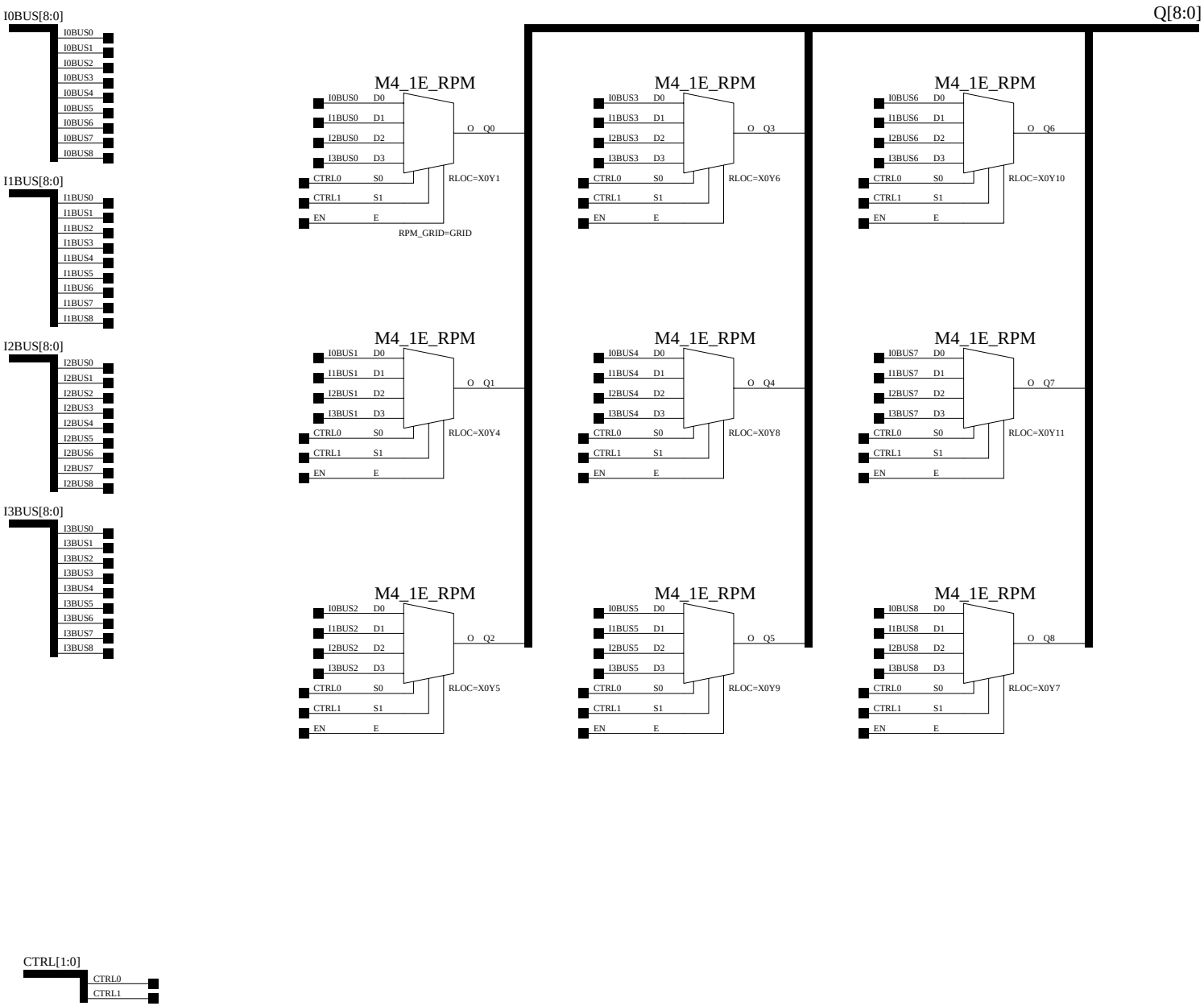
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 9-bit MUX for 2 9-bit Inputs, w/Enable. RLOC=GRID DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 42	PROJECT: D785D
		DATE: 1-27-2005_10:43	FILE: MUX2_9B_G2 . 1	PAGE: 44



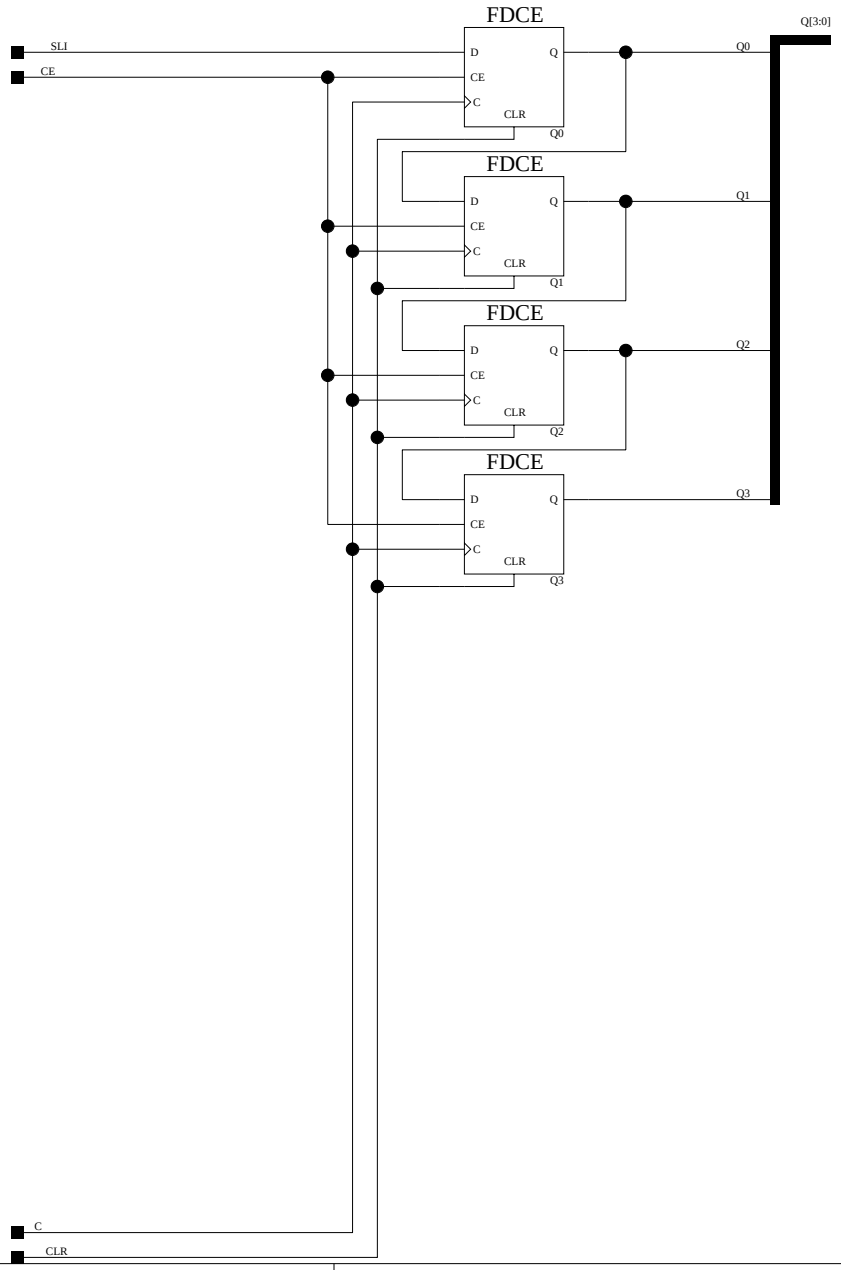
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 18-bit MUX for 4 18-bit Inputs, w/Enable Virtex MUX logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 9	PROJECT: D785D
		DATE: 7-18-2005_15:24	FILE: MUX4_18B . 1	PAGE: 45



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 18-bit MUX *DIAGONAL* for 4 18-bit Inputs, w/Enable Virtex MUX logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_15:25	PARENT PAGE: 10 FILE: MUX4D18B . 1	PROJECT: D785D PAGE: 46

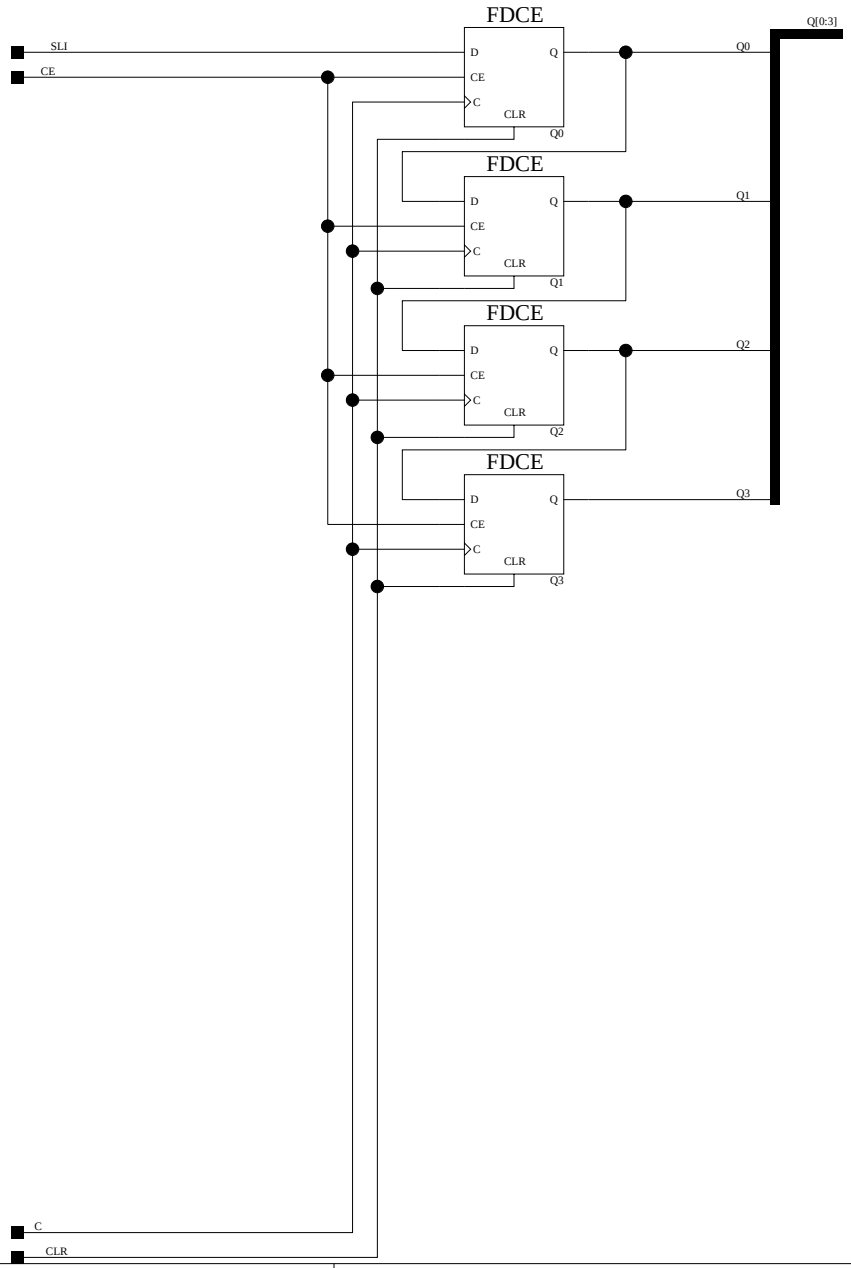


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 9-bit MUX for 4 9-bit Inputs, w/Enable. RPM_GRID, Vertical. Virtex MUX logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 45, 46	PROJECT: D785D
		DATE: 1-27-2005_14:28	FILE: MUX4_9B_GV . 1	PAGE: 47



XILINX		JRG
Title:	VIRTEX Family SR4CE Macro	
Comments:	4-bit Serial-In Parallel-Out Shift Register w/ Enable and Async Clr	
Date:	3rd October 2003	Ver: 1
Sheet Size: B		Rev: A

drawn by KS



Title:	VIRTEX Family SR4CE_R Macro		JRG
Comments:	4-bit Serial-In Parallel-Out, REVERSED ORDER on OUTPUT BUS! Shift Register w/ Enable and Async Clr		
Date:	3rd October 2003	Ver:	1
Sheet Size: B		Rev:	A