DDU5CTRL (file DDUctrl)

CMS CSC DDU5, Central Control FPGA

v39: 64bit err reset on BOE, TrgWC now uses all 9 bits, CloseL1A range now 1usec, BIG L1Afifo w/better Warn/Busy Logic
r2: add hysteresis for L1A_AF/Busy state, tune DAQovfl logic, tune SysRdy/BUSY logic. r3: tune L1pipe/StuckData logic
-r4: tune CRC Cnt Err monitor logic; r5: tune SCAovfl Reset & CountSample timing
v40: DMB & Trig.CRCs use MUX to load Zeroes (not Tbufs), change DDUfb reset
-r2: add time constraint to DDUFB reg to eliminate DDUFCRC logic lag. r3: tune BuffOvfl & EthLim logic
v41: SCA_Ovfl separated from DMB_Err & SomethingBad. r2: tune KillFiber glitch

Set All I/O to 3.3V

PART=XC2VP7-6-FF672
PROM=2*XC18V04-VQ44 (PARALLEL)

1: Mode Bit 0 LED0 on top, pins on away-side from LEDs
2: Mode Bit 1 RST_1=Asynchronous Reset for FPGA1 and ALL FIFOs
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GBE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/BXR/ECR if SW8 is off
8: FPGA version on LEDs

PROGRAM takes < 55 ms (31ms this FPGA)

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DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070, 240560 Bytes
-^ Ignores TMB Data"^ GBE.ByteCount = 8*DDU WordCount 8 TS assumed
DDUCTRL -- Project History

v1-2: from ddu4ctrl v28, FIFO Full JTAG Reg is 16-bits
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SlkWaiten from VMEct
v15-16: fix DMBwarn, add VME FakeLinenable; put DMBlive[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG Trail_Err resets, FOV=
v17-18: tune DMB Full, Inst, EndTimeRst, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 bytes
v19: Require SlkWaiten for CFEB L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--rev2: SLOW3
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In Time Out go to BOE Stat
v22: add VME_reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDD

Good! rev3: tune PDMBlive_EN & RST_STRT logic
v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisable

Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/1
v25: tune L1err & InErr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critical
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB. v27: tune CFEB L1er, 8/16 sample flag. WarnMon & BX offset
v28: add Big debug reg. on F21, Timeout reg. on F28 use LnextFIFO, replace LLLREN w/LFOE for TimeoutReg, make ERA-St/End-TO perm
v29: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV=
v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logic

v31: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L1A
v32: change CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4), modified ERB13 for perm DDU_DLL_err
v33: change SourceID=760=2F8h for TF-DDU  v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!*

v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic split

v36: non-TF DDUs have SrcID==BrdID, NoLiveFibers now readout on L1A. r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFDM

v37: diagnostic changes....Tune DMBl1err(notALCTerr), BadCtrl(notMissTrg), Lie(addMissTrg)

v38: DMBCritErr=Err7, improve Htmb/alc time/code-err goes to InMmxtReg, InTimeout goes to EndTimeBusReg

r2-3, removed redundant RdyIn2 requirement for SEN bits. r3-4, OSyncRst on ~clk0, tune OIFO Mon, req. VMEctrv17+ & InCtrlv22r3

New Ideas: Store & check DMB source id's from each fiber?

Default Startup Order:

4) DONE
5) En. Outputs
6) Release WE

DDU WordCount (64-bit words) for "No Data" event: 0x0006.
DDU WordCount for one DMB (only one CFEB): 00D2 = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=4): 49h = 144 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Ah = 814 dec, 6532 Bytes
DDU WordCount = (6 + 25*Ns*nCFEB + 4*nDMB) < 30970, 24560 Bytes

**Ignore TMB Data**

Gbe_LogicCount = 8*DDU_WordCount

---

TST Clock BUFGMUX
0P 2clk 3clk 4clk 5clk 6clk 7clk 8clk 9clk 10clk 11clk 12clk 13clk
01 23 45 67 89 01 23 45 67 89 01 23 45
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13
DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to-on Era15, XtraTrgTrails on Era5+13,DMBffm 3-bits held Reset until SystemRd
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFO
r3: add DMB-TO/FIFOfull to TMB/ALCTerr Regs, adjust their time to L2DMBrd; TrgWC only Comp 8 bits, A-T-Switch Req. NoSpwdE

r3: DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to-on Era15, XtraTrgTrails on Era5+13,DMBffm 3-bits held Reset until SystemRd
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFO

r2: moved redundant RdyIn2 requirement for SEN bits. r3-4, OSyncRst on ~clk0, tune OIFO Mon, req. VMEctrv17+ & InCtrlv22r3

DDU WC, 2 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes
DMB Full signal detected by an InFPGA InUnit

Add BXR/BX0 control to BXN counter
Add Trig/Evt Type to L1A FIFO
Mask DMBs with critical error until they're Reset
--- report to DAQ and Trigger
Resets between DMBs on same FIFO?

This event is garbage!
Set error bit in SLINK...
Inc. MultiTrigL1 err check?
Tell FMM...

Tell TTS to slow down...

Special occurrence warning
SINGLE WARNING
SLINK_WT_EN enables DCC/SLINK_WAIT and CFEB_DAVLCT checking from DMB.

DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal, then DDU Stops on DCC ~PAF signal.

Was like SLINK, now is DCC ~FF or ~PAF?

S-Link Ready  S-Link ~Full

Try MaxDelay=5ns here?

Page 16

OUT_GBE

DO[65:32]

Link Ready

DO[31:0]

S-Link ~Full

DCC_FULL

~FF or ~PAF?

~FF

~PAF
Soft Reset All: ~0x23 (0x23 is CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
use w/DCC VME FDC!
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
use w/DCC VME FDC!

Start Data Taking: ~0x39 (57dec) = 0x09
Stop Data Taking: ~0x38 (56dec) = 0x07

CCB Code: ~0x38 (56dec) = 0x07
Stop CCB Code: ~0x39 (57dec) = 0x09

Fiber Inputs frozen until ~98X after Reset is gone
Sync. Reset All: ~0x39 (57dec) = 0x09

Sync. Reset All: ~0x39 (57dec) = 0x09

Clock 40 MHz

**Removal**

---

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**JRG** 1
DATE 12-7-2006 14:24
**D785C** 2G

**DDU CCB Command Decode**
**DDU Controller Logic**
**CMS CSC Electronics**

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**JRG** 1
DATE 12-7-2006 14:24
**D785C** 2G

**DDU CCB Command Decode**
**DDU Controller Logic**
**CMS CSC Electronics**
Use these busses for CFEB CRC and Special Word checks.

Use NEW DMB E-codes only (next-to-last word bits).

Covered RDAT bits synchronized to falling edge of CLK.

Covered RDAT bits synchronized to falling edge of CLK.

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Covered RDAT bits synchronized to falling edge of CLK.
Note that DONE means Last FIFO_REN is done!

Use LFF and SLINK READY to delay START of next event?

DONE

RST DONE

FDRE

DONE-1

RST

FDCE

START

BUSY

LIA POP

LFOK[3:0]

DFE

RST DONE

FDCE

RST DONE

FDCE

RST DONE

FDCE

RST DONE

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FDCE
Check for DMB Error Word and consistency:

FDONE & RENOE-0 in-time with LGoodLW, next-to-last word (E-codes) on DAT

2-logic-step delay
synched w/GoodDat

"FILL Flag"

LOW means FIFO REN+OE are unconditionally Enabled

Check consistency of the four "Special Word" bits:

"FDONE" indicates "LGooLW" was received: waiting for the final NotEmpty word from FIFO

-----> "RENOE-0" holds REN enabled until "FDONE" goes false

"FIFOdone set at E-codeDone & LRENtrue^^^"
Control Bit List:

0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 [2 or more out of 4]
3: Latched Voted Special Bit 13 [2 or more out of 4]
4: Latched Voted Special Bit 14 [2 or more out of 4]
5: Latched Voted Special Bit 15 [2 or more out of 4]
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE->>OETrail)

Event accumulation of valid DMB-path-Xmit errors

XMIT_ERRORS[14:0] synched w/GoodDat+1

Event accumulation of valid DMB-path-Xmit errors

permanent accumulation of DMB-path-Xmit errors

Permanent accumulation of DMB-path-Xmit errors

Watches for multiple DMB-FIFO-path errors on current path

FIFO Done Timeout: 132 usec = 5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another* 4 for 4 CSCs: 38914 (972 usec)

25ns clock period here

FIFO Done Timeout: 132 usec = 5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another* 4 for 4 CSCs: 38914 (972 usec)
Read the 60 28-bit counts for CSC board occupancies. 4 high Adr bits tell DDU input, 2 low Adr bits specify Board Type:

Always add 1 if board is present (use FastCarry input) -->

Reset counter to 0 after 59 (60 good addresses)

Only operate on CSCs with DAV, skip non-DAV addresses but wait for CSCs w/ DAV then get BrdDAVs from DMB Hdr.

Each Brd requires one CLK to Read prev. value, then one more for Adr+1 and WEN:

So Read on EVEN cycles, Write on Odd cycles (CB4CE below):

Then get BrdDAVs from DMB Hdr.
Use DMB_RD to determine which FIBER we're currently reading

Stop READ cycle on DCC Near Full
How to "not stop" in case we only have one word left to read? Not possible to do well...
Pipe all L1As for 1000ns, if more than 1 then set CloseL1A bit.^^^ Finally, perform BX-40 to correct BXN and store CloseL1A as BXN bit-12. Then use SBXN12 output (Close_L1A ) for Stage2 DMB checks: 1000+ ns L1As means that first 2 CFEB samples should always have good L1A#.

Event START timeout 3.2usec: 128=1000/0000=0x80...

Calibration START timeout 7.2usec: 288=0x0120.

LHC BXN cycles from 0 to 3563
Set to BX=0 one cycle after BX_LIM: 3563=1101/1110/1011=0xDEB

SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

---

**Title**: L1A Proximity Tracker: 1000ns Close L1A Monitor closer than 950ns is Tricky for DMBs

---

**Diagram**: L1A Proximity Tracker diagram with various components and connections.

---

**Notes**:
- Set to BX=0 one cycle after BX_LIM: 3563=1101/1110/1011=0xDEB
- SPS BXN cycle from 0 to 923: CLR after 923=0x39B.
Access FIBEROK from JTAG as a fiber check.
--- > RESET required after fiber status change for now...
Change in FIBEROK is BAD! Set error code.
...notify FMM and maybe set STATUS bit, but
...data is OK until FIFO read time-out occurs.
...but how to know WHEN the bad-data comes out?
--- > timeout will probably occur for that event

MASK fiber on Start/End TIMEOUT? Kill it in LFOK...
Lowest 9 "Q" nibbles synched to falling edge of CLK

All "QS" nibbles synched to rising edge of CLK

FAST10B1
Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND
similar to: OR of 4 AND2 .AND. AND2B1

15th October 2003
JRG
EN low drives Q high
I0/I1 get Inverted at Q
Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits

DDU Controller
CMS CSC Electronics
Check for ALL bits set, ANY bits set and NOTALL bits set

DDU Controller
CMS CSC Electronics

ANY

NOTALL
The lowest 13-bits of every 16 go into the CFEB CRC (but reverse them!): 52-bits of data --> 15-bit CRC
Only the lowest 12-bits of every 16 go into the Special Word Decode (un-reverse these!)

Note: GOODDAT == GOLDDAT here!

Control Bit List:
0: Gold Data (this FIFO has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 [2 or more out of 4]
3: Latched Voted Special Bit 13 [2 or more out of 4]
4: Latched Voted Special Bit 14 [2 or more out of 4]
5: Latched Voted Special Bit 15 [2 or more out of 4]
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB FIFO Data)
8: End of Event (DONE --> OETrail)
Critical DMB Monitoring Information (Production DMB) UPDATE!
See http://www.physics.ohio-state.edu/~cms/dmb/dmbdatafmt.html

Within each time sample: word100[15:0] = dummy = 0x7FFF <<-----What about SCA Over-Written Event error?
word97[14:0] = CRC15 result

word98[9] = CFEB L1A_FIFO Full error

Header5 = TMB/ALCT DAV bits, 3 repeats
Header1,5[4:0] = CFEB_DAV[CFEB5:1], 2 repeats
Header1,5[9] = CFEB_CLCT[CFEB5:1], 1 repeat
L1AN[23:0] = HDR3[11:0],HDR2[11:0]

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Verifies that the 3rd-to-last GoodData word from each FIFO is a CRC Check and the check is OK.

This CFEB CRC result is a STAGE3 Function!!

This CFEB CRC result is a STAGE3 Function!!

COUNT_SAMP 

Load Zero on CRC when LWC loads ONE

CFEB CRC Checks Done for this FIFO? Last non-control word S.B. CRC check. Verify that multiple of 8/16 CRC Checks are done if CFEB data present.

The last LGoodDat-A from each DMB (just before DMBEND) should be a CheckCRC unless there was no CFEB data. Otherwise set CRC Error.
Need to deserialize b13 in 1st sample for *EACH CFEB* and compare to Hdr2d!

ON for CFEB LWC = 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24:

Set/Reset at LWC = 25 or LVB15

Recheck Later-->
May need a programmable offset...

only check L1A for 1st 2 samples

DISABLED! -->

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Stage 2 Logic: CFEB Status Decode
DDU Controller
CMS CSC Electronics

JRG D785C
9-13-2006, 16:38
STAGE2 .4

 Ensode to 3 bits + Phase (0), compare to Hdr2d[11-8], can be +/- 1?
Then what if 2 LCTs are set (overlap)? Encode the lowest bit or SKIP IT.

known for DDUtr-1

DISABLED! -->
Check for Problems in DMB header/trailer & set DMBerr register

- **Stage 3**
  - **DMB RD[14:0]**
  - **FD15CE**
  - **LDMD RD[14:0]**
  - **FD15CE**
  - **L2DMB RD[14:0]**

- **Stage 4**
  - **DMB MOVLP[4:0]**
  - **DMB MOVLP[0:4]**
  - **SUM-DMB-ERR**
  - **SUM-DMB-ERR-0**
  - **SUM-DMB-ERR-1**

- **Stage 5**
  - **DMB_CFEBLCT[4:0]**
  - **DMB_CFEBLCT[4:0]**
  - **DMB_CFEB_SYNC_ERR**
  - **LVDAV-LCT-ERR**
  - **LDMB_CRC_ERR**

- **Stage 6**
  - **DMB_L1A_TR[7:0]**
  - **DMB AFUL**
  - **DMB_MOVLP**
  - **DMB_AFUL[7:0]**
  - **DMB AFUL[7:0]**

- **Stage 7**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**

- **Stage 8**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**
  - **DMB AFUL[7:0]**

**Notes:**
- **Good up to & including E-code @STAGE2**
- **Known for E-code+1**
- **Known for DDUtr-1**
- **Known for DDUtr-2**
- **Known for E-code**
- **Known for DDUtr-2**
- **Not voted so not critical**
Trigger CRC Check Control: assume that TMB comes after ALCT!

 affects L1A check: DoTMB, 1st_TMB/1st_ALCT

may be also Miss-ALCT! at TMB-TRG

Check for "wrong" or missed trg board end:

Reset at BOE?

Determine if Trig Trail is ALCT or TMB

Load TCRC with ZERO on ALCT/TMB trail

Compare ALCT/TMB trail to this CRC

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Stage 2 Logic: Trigger Board Flags
DDU Controller
CMS CSC Electronics
Trigger Comparisons and Error Checks

TRG WC counts 16-bit words: div 4!  This result is a STAGE3 Function!!
DDU Timing Info
DDUctrl to In_FIFO signals: 2" - 4", .3ns - .8ns
4-FG: 0.60 6-FG: 0.32
IRCLK has 4 loads, may slow signal by 0.1 - 0.3ns
FD set/hold: 0/0.14  Clk to Q: 0.38
PPD due to rst setup: 0.60
Sync. pre-clr to Q: 1.25

FPGA I/O Delays (lvcmos33, ns)
IBUF: 0.92 IFD set/hold: 0.92/0.12  Clk to Q: 0.65

OFBUF: 2.33 OFD set/hold: 0.26/0.14  Clk to Q: 2.11

*modifiers for drive/slew settings:
6mA: add 2.60 for Slow, 1.26 for Fast
8mA: add 1.68 for Slow, 0.68 for Fast
12mA: add 1.18 for Slow, 0.26 for Fast
16mA: add 0.52 for Slow, 0.02 for Fast
24mA: +0.44 for Slow, -0.08 for Fast

DDU CRC Logic for SLINK/C.D.F. Compatibility
JRG 2 D785C
CMS CSC Electronics

DDU Status/Error 32
DDUSyncErr-- FiberErr-- NoLiveFiber-- CriticalErr-- SingleErr-- L1Aerr--
DDUCRC[15:0]OD[63:0]

FIFO I/O Delays (ns)
RCLK to Empty (low state) Vcc: 3.38V 3.94V
Max: 3.5  Min: 2.5 3.02 - 3.18 3.29 - 3.29
Vcc to Not Empty (high state) 3.22 - 3.34 3.23 - 3.31

RCLK to Q11 False (low state) Max: 4.3  Min: 2.5 3.32 - 3.62 3.40 - 3.64
RCLK to Q11 True (high state) 3.31 - 3.87 3.51 - 4.06
Check for Track Finder signal, record TF errors
CRC-16 Primitive Polynomial: $X^{16}+X^{15}+X^{2}+1$, same as USB standard
Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.

--- Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.
IDLEOUT needs local control logic.
Custom Logic for DDU

similar to: AND12B10 with an OR2 (allows ON to override)

JRG
Send 2 Idle bytes:
K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050 (time-ordered)
= 0xBC50 (in parallel)
Read in 16-bit data from FIFO, convert to 64-bit, process as 8-bit, then transmit to GT as 16-bit.
Find a better way to set ElimThresh bits!

HalfFull is Default
VIRTEX Family FD8-16CE Macro
8-16-Bit Bus Matching Register with Asynchronous Clear and Chip Enable

Title:
VIRTEX Family FD8-16CE Macro

Rev.:
A

4th February 2004

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HDR=8 header + 4 destination bytes.
TR=2 tail + 2 idle bytes.

12 RCLK Sync minimum here.

StateMachine Reset=RRST2
Sync's STATE0 start with RCLK rising edge

Output Options:
sync, header, data, CRC, trailer, idle
release of RESET on rising RCLK edge
Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.
Send 2 Idle bytes: 
K28.5(10111100)+D16.2(01010000) 
= 0x1BC + 0x050
Send 4 Sync bytes:
K28.5(10111100)+D21.5(010110101) +K28.5(10111100)+D2.2(001000010) = 0x1BC + 0xB5 + 0x1BC + 0x42
Title: VIRTEX Family 4-AND3COMI Macro
Comments: 4-AND3 Bus Gate plus 1 common bit

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drawn by KS
1st October 2003

Page 27
Load/Read BXN Orbit LOGIC

Default=924 BX per Orbit

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FD12B3563

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

DDU Load/Read BX per Orbit Register
DDU Controller
CMS CSC Electronics
15-bit JTAG Register Read out (on DVCENB)
16-bit JTAG Register Read out (on DVCENB)
def=923=39Bh=11.1001.1011

```
A
B
C
D
D8
D7
D6
D5
D4
D3
D2
D1
D0

PRE
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
CLR
CE
CE
CE
CE
CE
CE
CE
CE
CE
CE

D[11:0]
```

Q[11:0]
FOK LED
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED
--LIT == Active Data Xmit
--OFF == No data to Xmit
Load ZERO to kill readout path
ONES are alive
[14:0] == Enable DMB input fibers
[15] == Enable 'Check Disable' below:
[16] == ALCT
[17] == TM
[18] == CFE
[19] == DMB (for TF)

^^^Glitch Protection for F14^^^
VIRTEX Family SR4CE Macro
4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset

Q[3:0] Q1 Q3 Q2 Q0
CLR CE SLI

Title: VIRTEX Family SR4CE Macro
Summary: 4-bit Serial-In Parallel-Out
Shift Register w/ Enable, loads a single "one" on Sync Reset
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drawn by KS
Check Status LOGIC (F3), shift test (F2)
DDU Controller
CMS CSC Electronics

INT0
INT1
INT2

VOTE

AND3
AND3
AND3
AND3
DDU Controller
CMS CSC Electronics

Vote 2 out of 3, PLUS common AND and OR bits