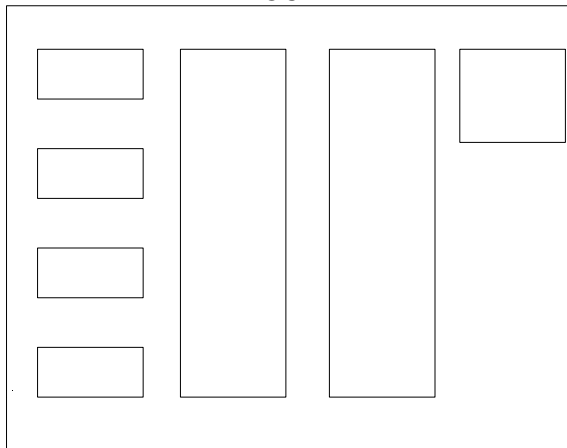


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D785T

CMS CSC DDU VERSION 6

BLOCK



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UPDATES TO D785N

80 MHz Clock Terminations

/BE on FIFO SET #3

PCB Layout Copper PIN Clearance

ADD 1N5817 Diode between powers

Add IAKOUT

IRQ (open collector)

IACK

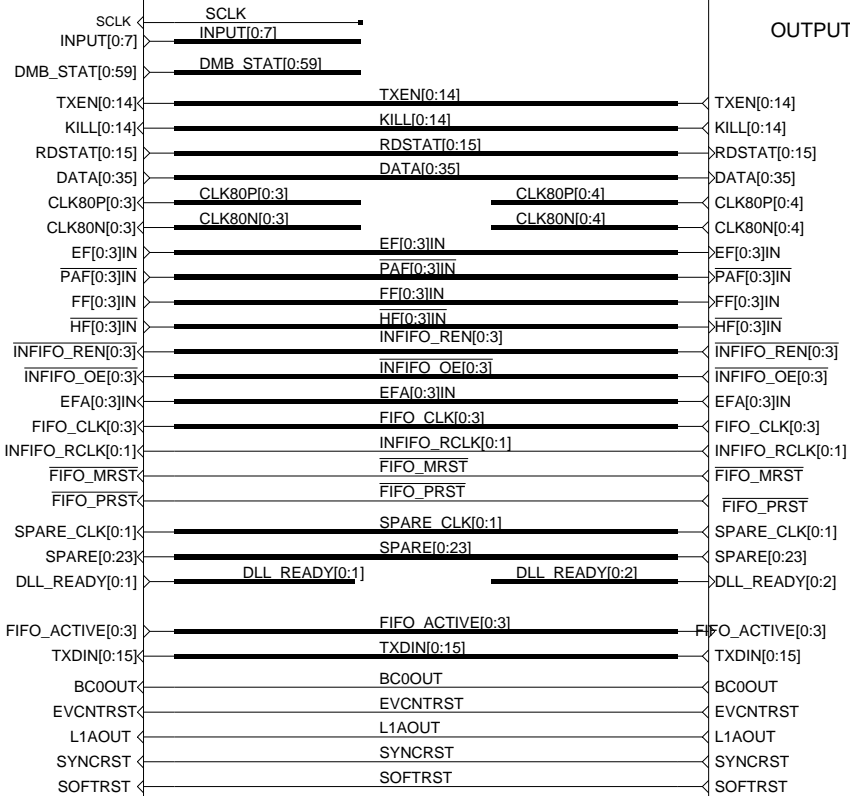
Fix cap/resistor space on bottom side of PCB

Emergency VME Logic. Add /AS

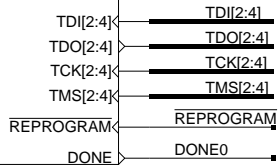
add logic for dtack. To keep the light on if stuck low.

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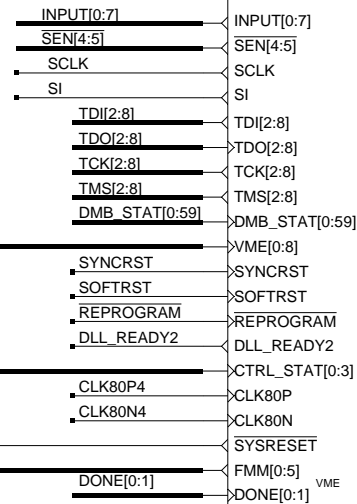
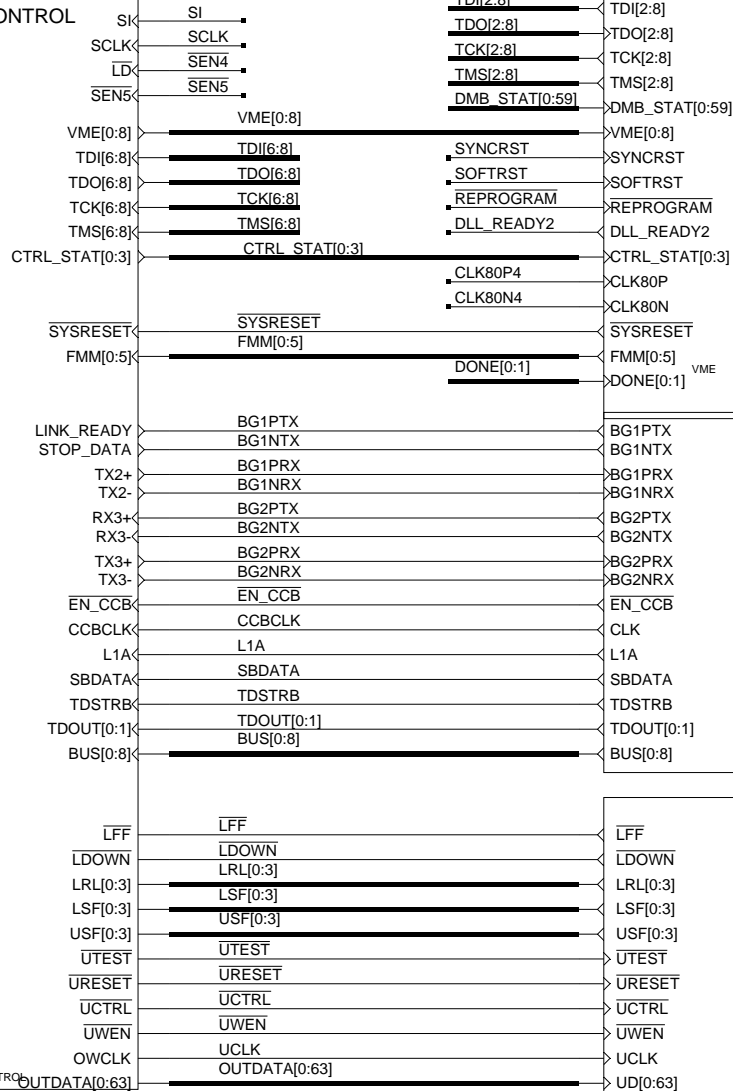
OPTICAL INPUTS & FIFOS



GLINKS



OUTPUT CONTROL



VME

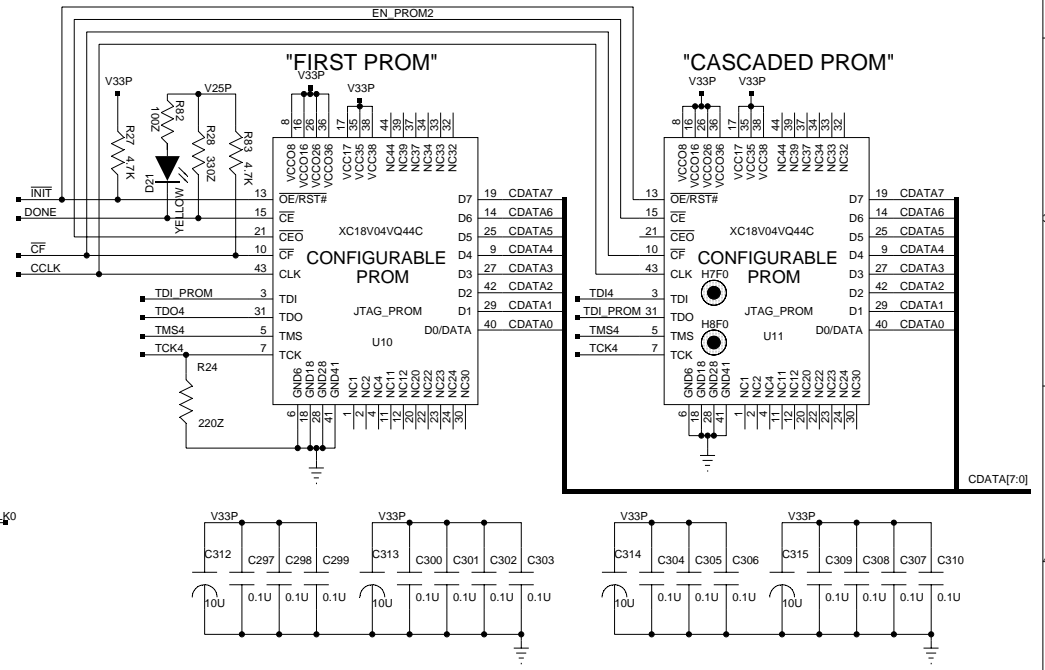
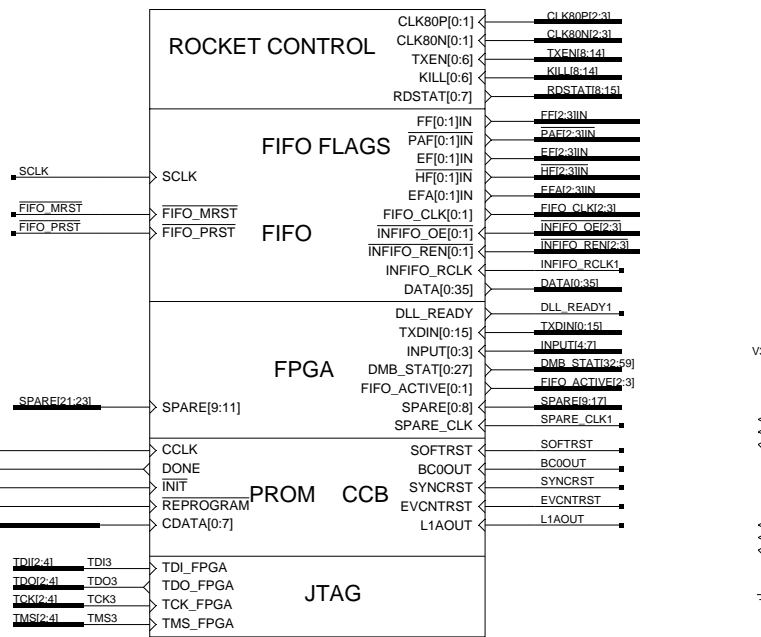
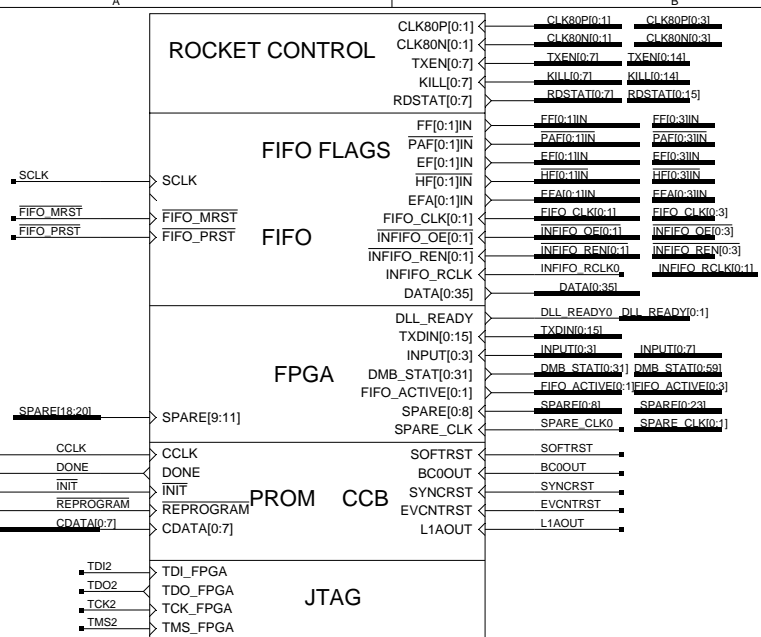
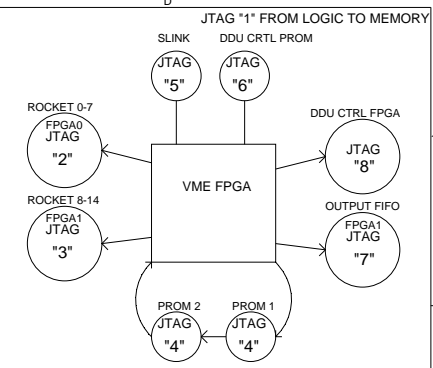
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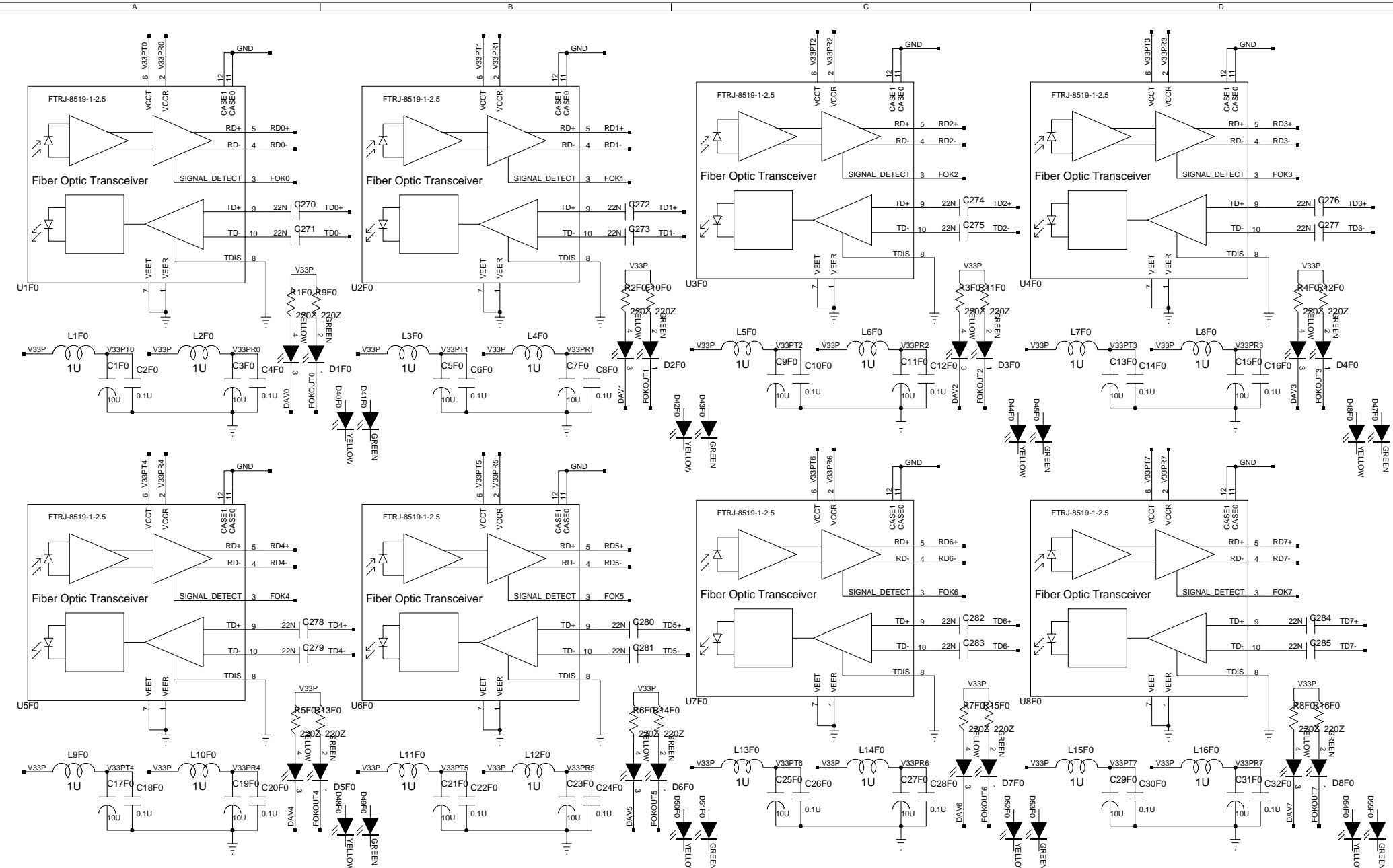
REPROGRAM REPROGRAM

SLINK

TDI TDI5
TDO TDO5
TMS TMS5
TCK TCK5

FPGA_ID PIN C25 ON INPUT FPGA'S CHANNELS 0-7 FPGA ID = '0'
CHANNELS 8-15 FPGA ID = '1'





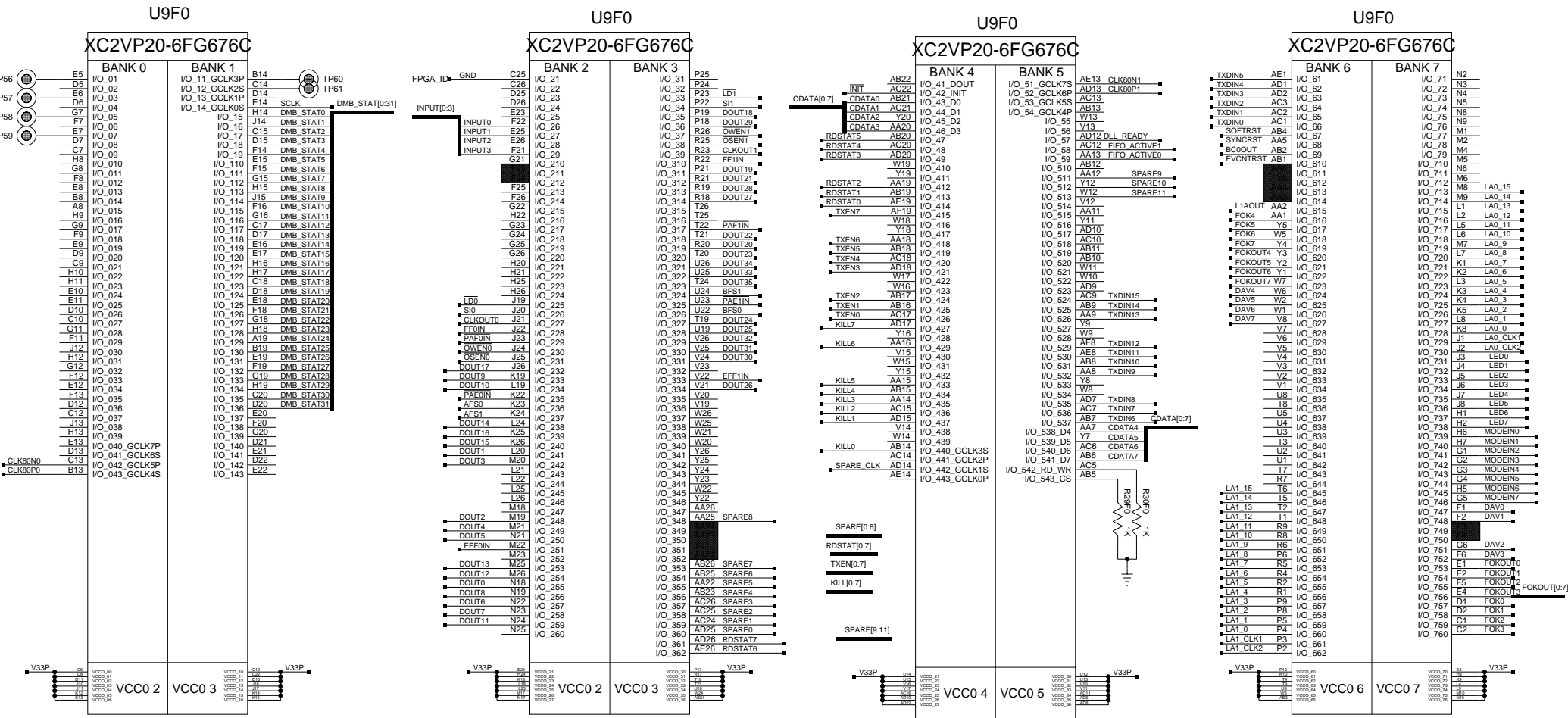
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 174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE
OPTICAL TRANSCIVERS AND ROCKET I/O
 FULL DDU
 CMS CSC ELECTRONICS

BY
 DCH
 DATE
 6-8-2005_7:51

PROJECT
D785T
 FILE
 INPUTF0 . 1 PAGE
 2A

XC2VP20-5FG676C LOGIC = D785B

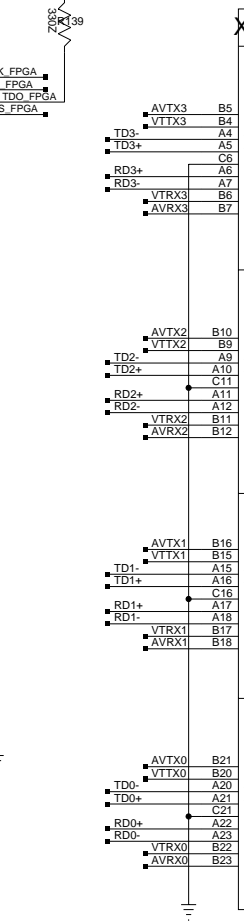
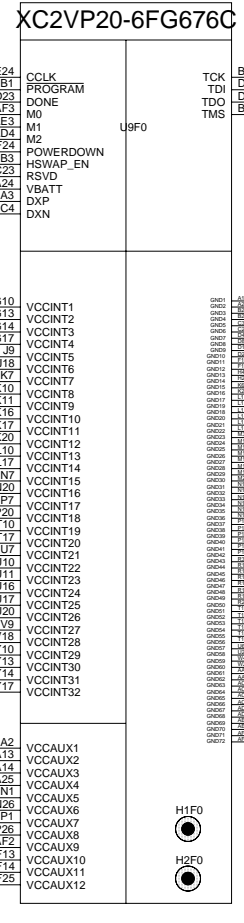
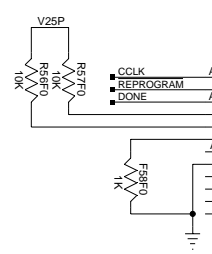
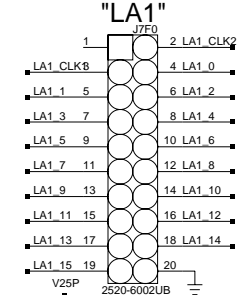
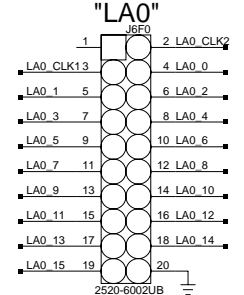
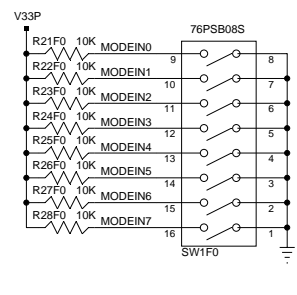
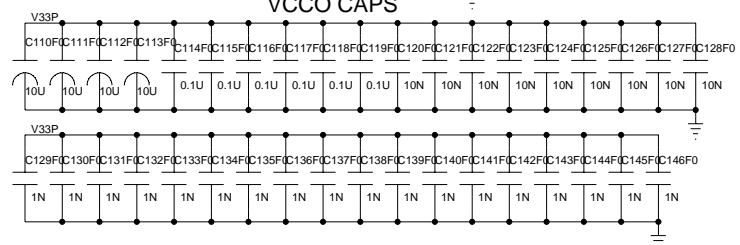
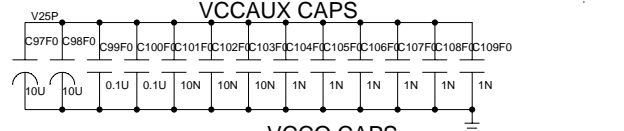
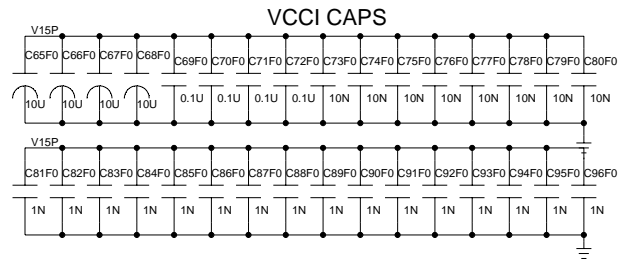
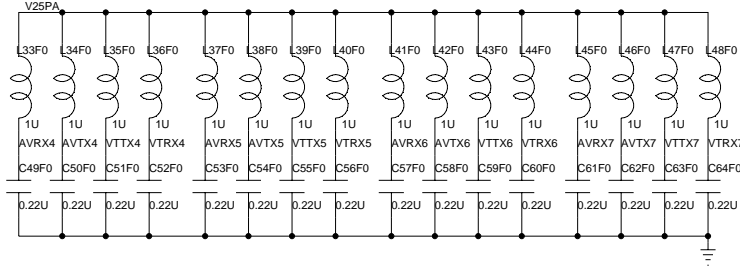
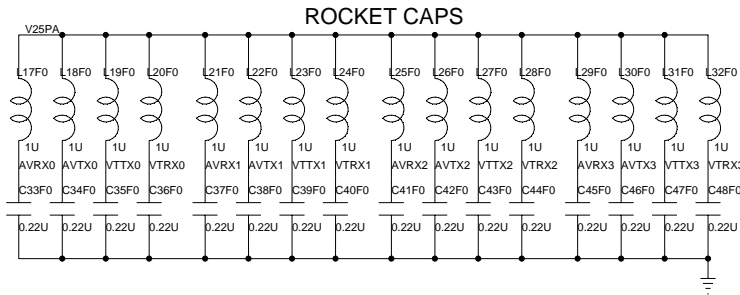


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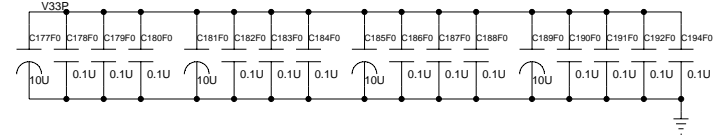
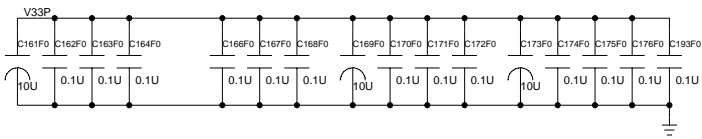
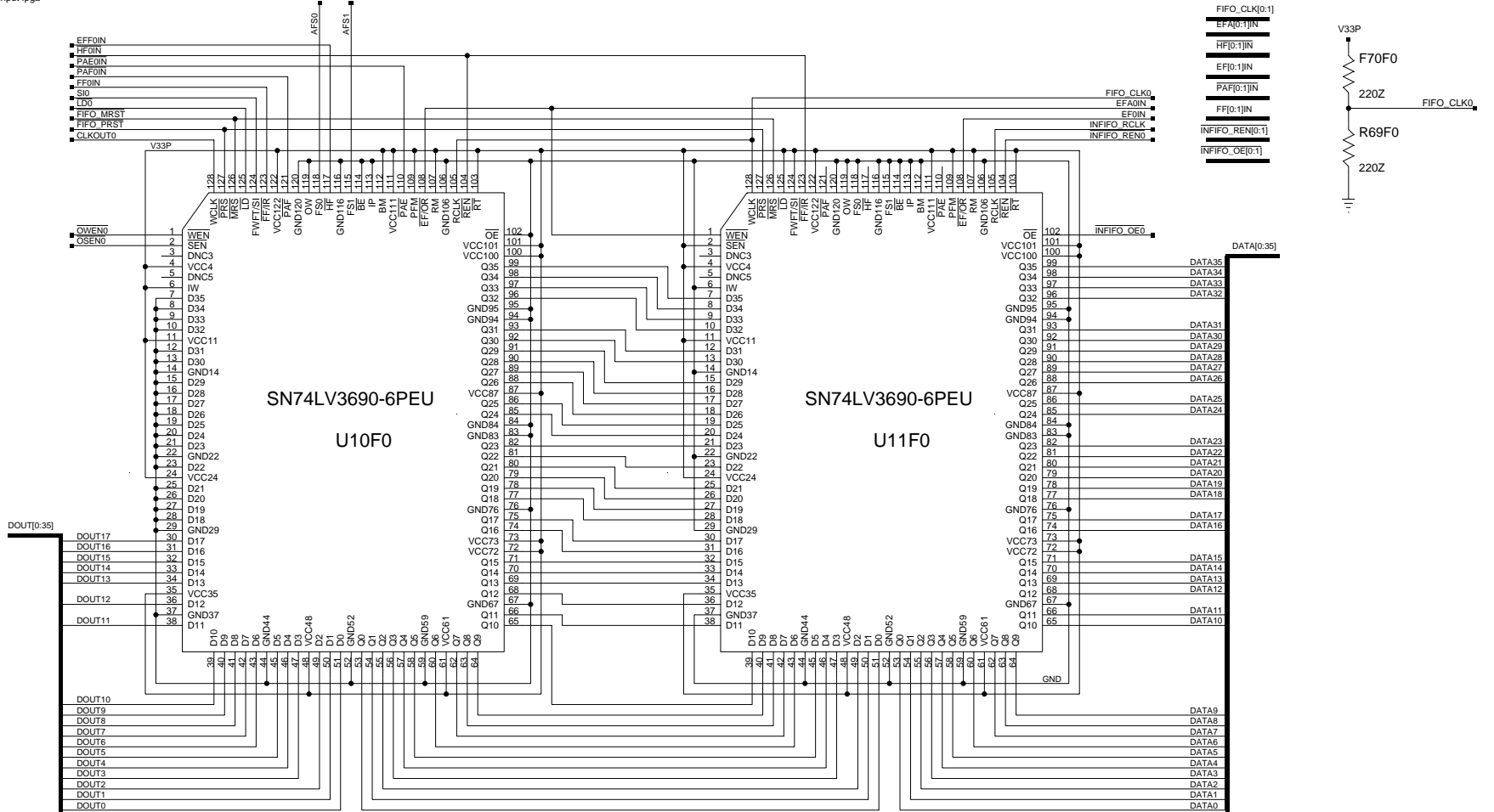
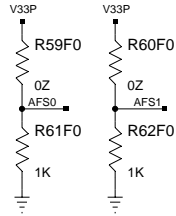
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OPTICAL TRANSCEIVERS AND ROCKET I/O
FULL DDU
CMS CSC ELECTRONICS

BY
DCH
DATE
6-2-2005_14:04

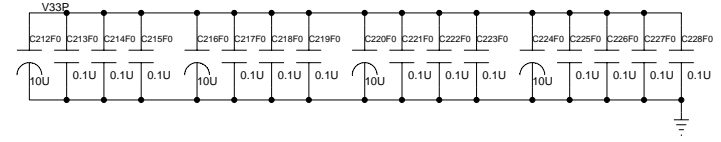
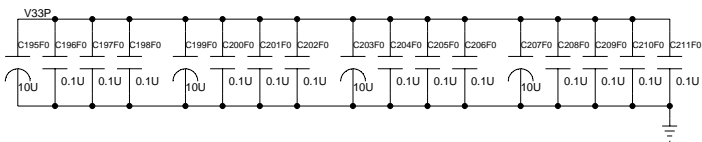
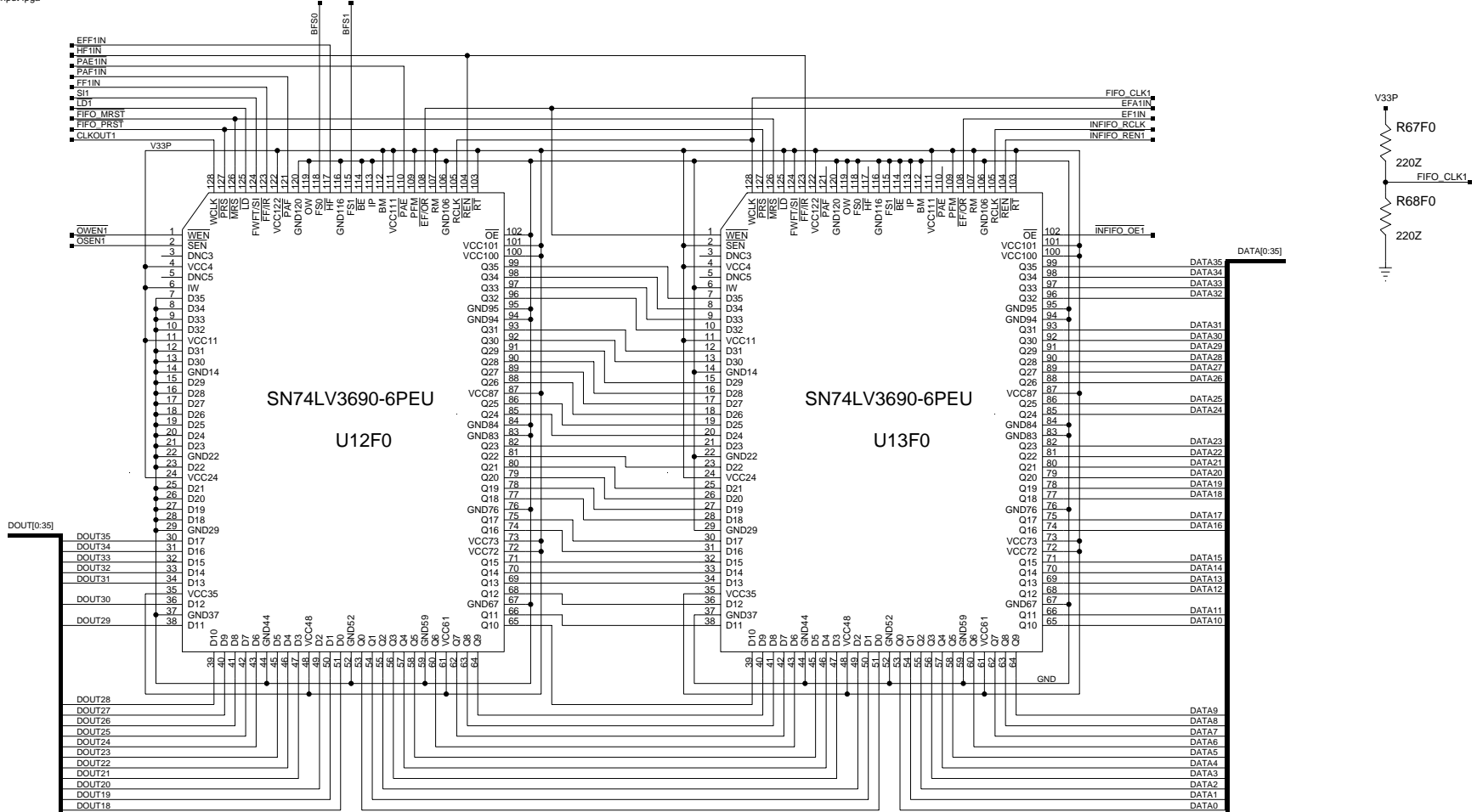
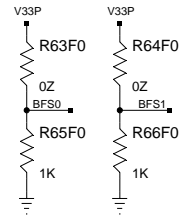
PARENT PAGE
PROJECT
D785T
FILE
INPUTF0 . 2
PAGE
2B

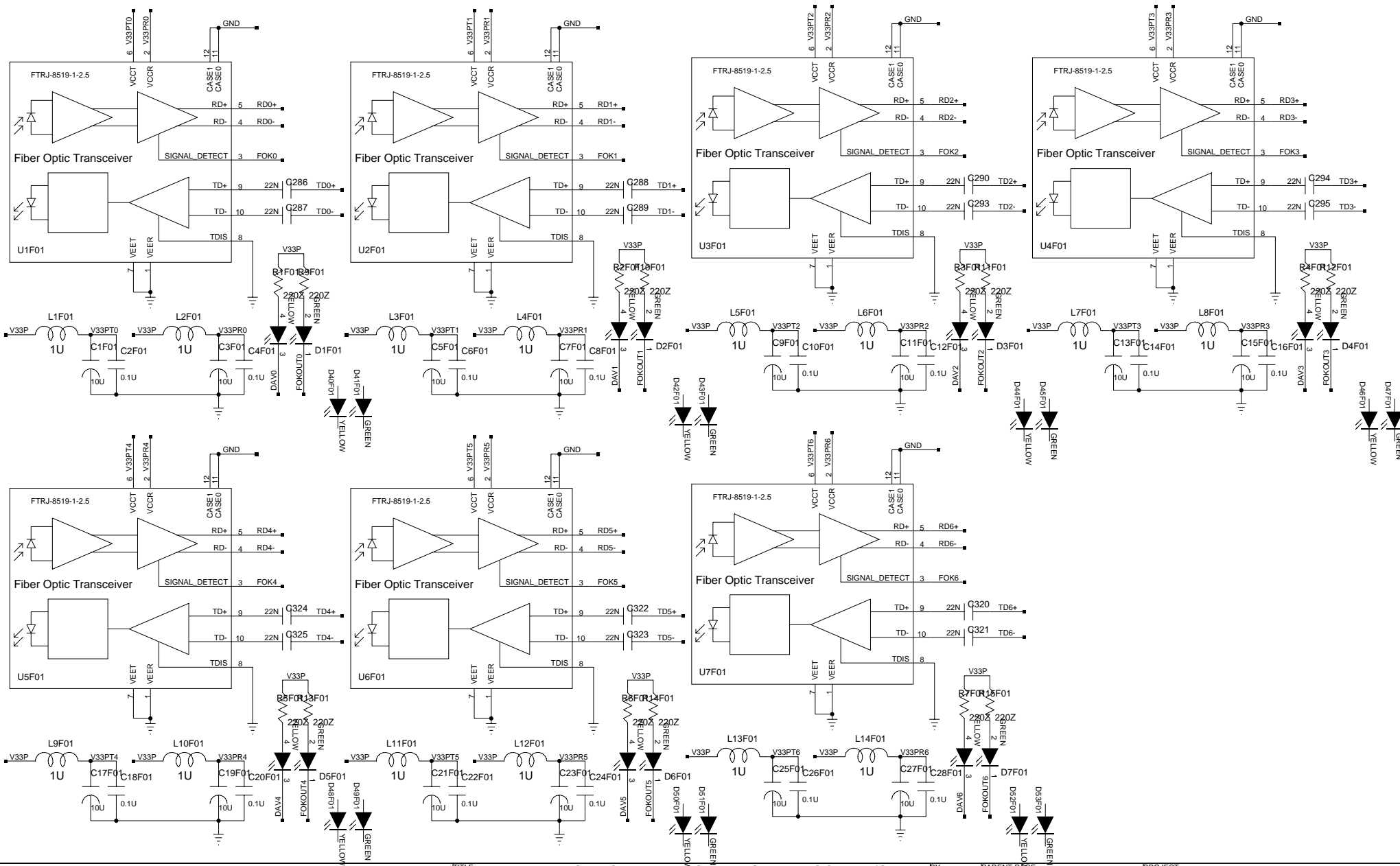


add four interface lines between incrtl and vme / input fpga
input fpga does flag programming control

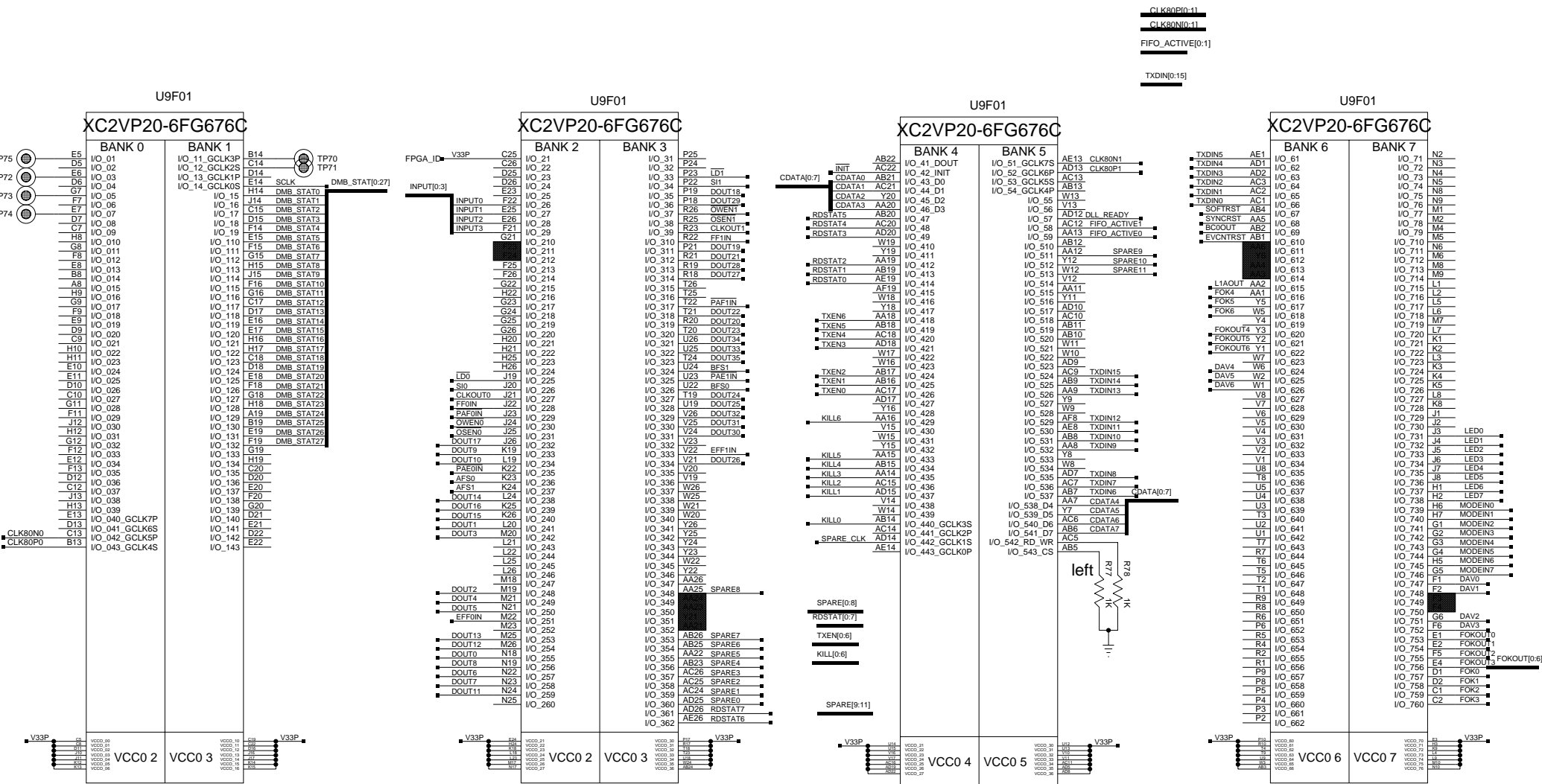


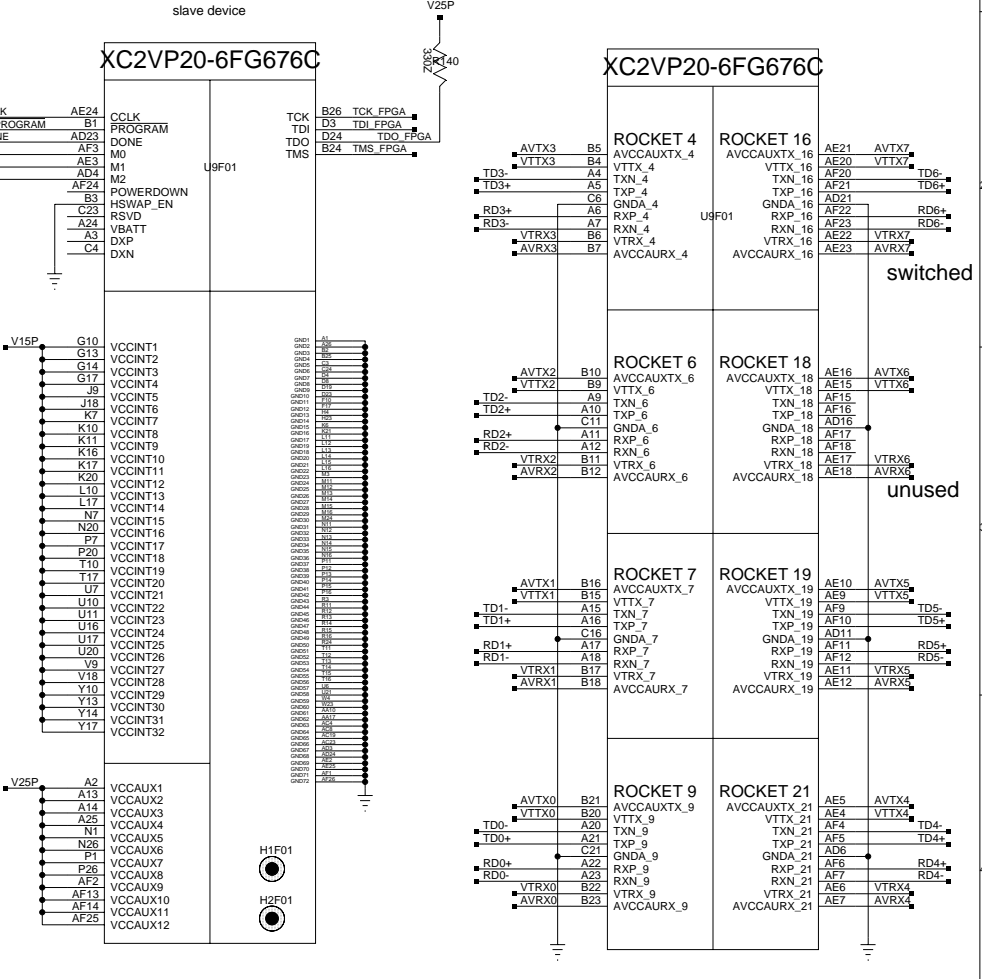
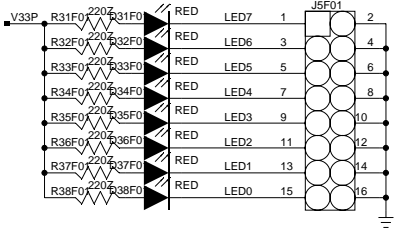
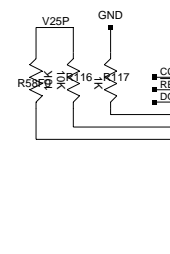
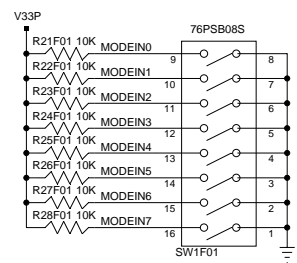
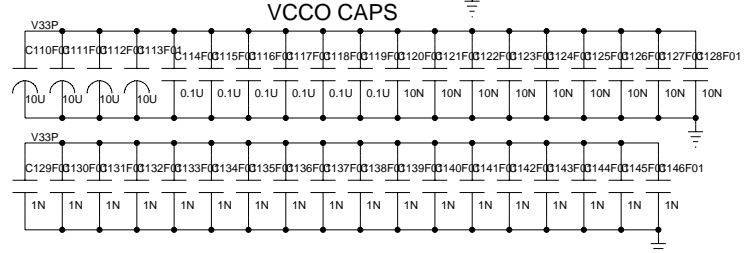
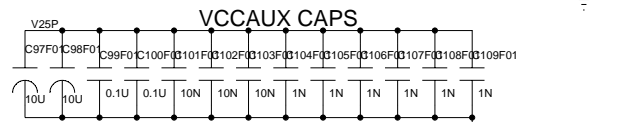
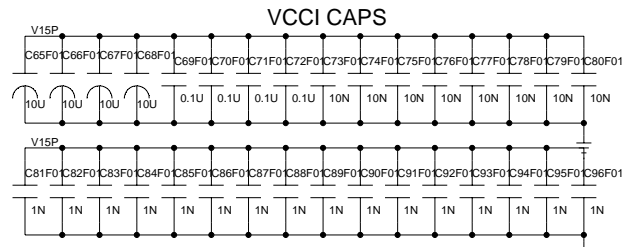
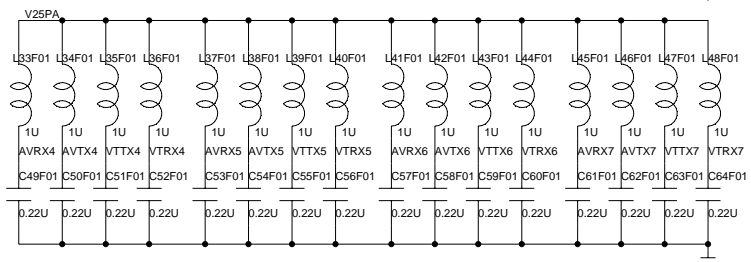
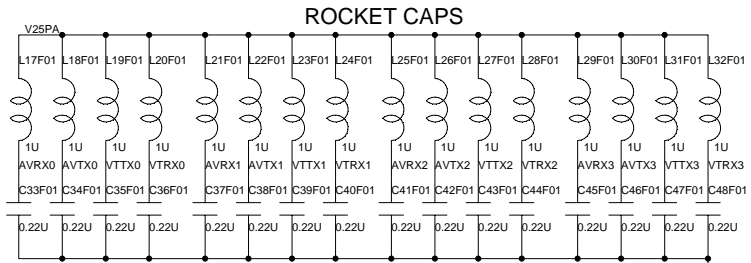
add four interface lines between incrl and vme / input fpga
input fpga does flag programming control

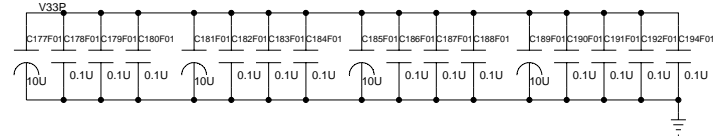
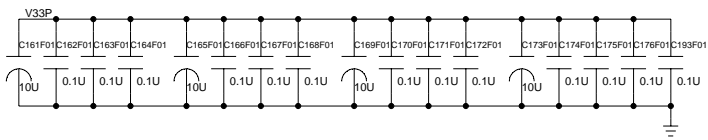
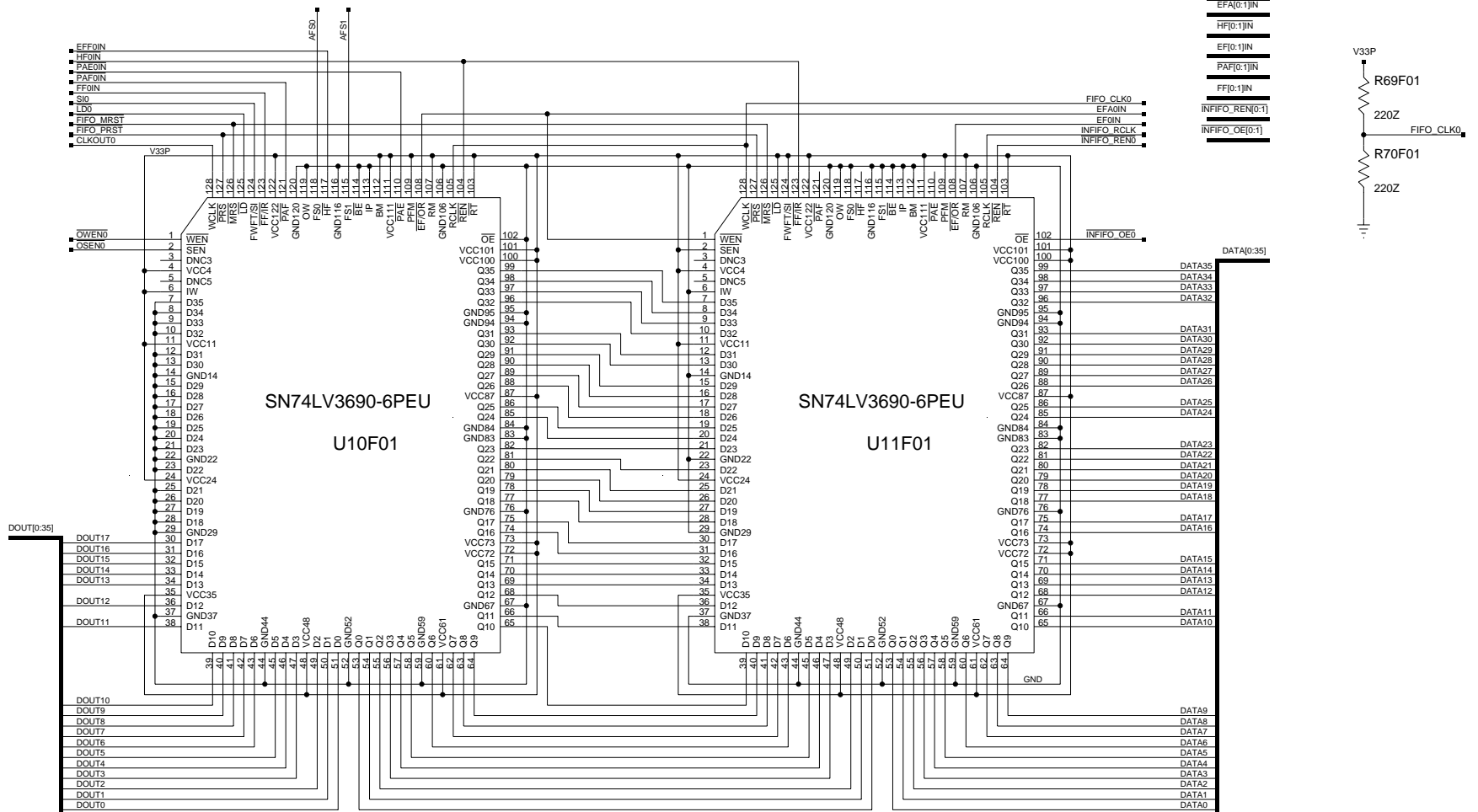
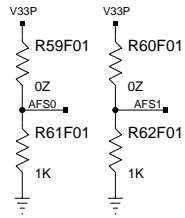




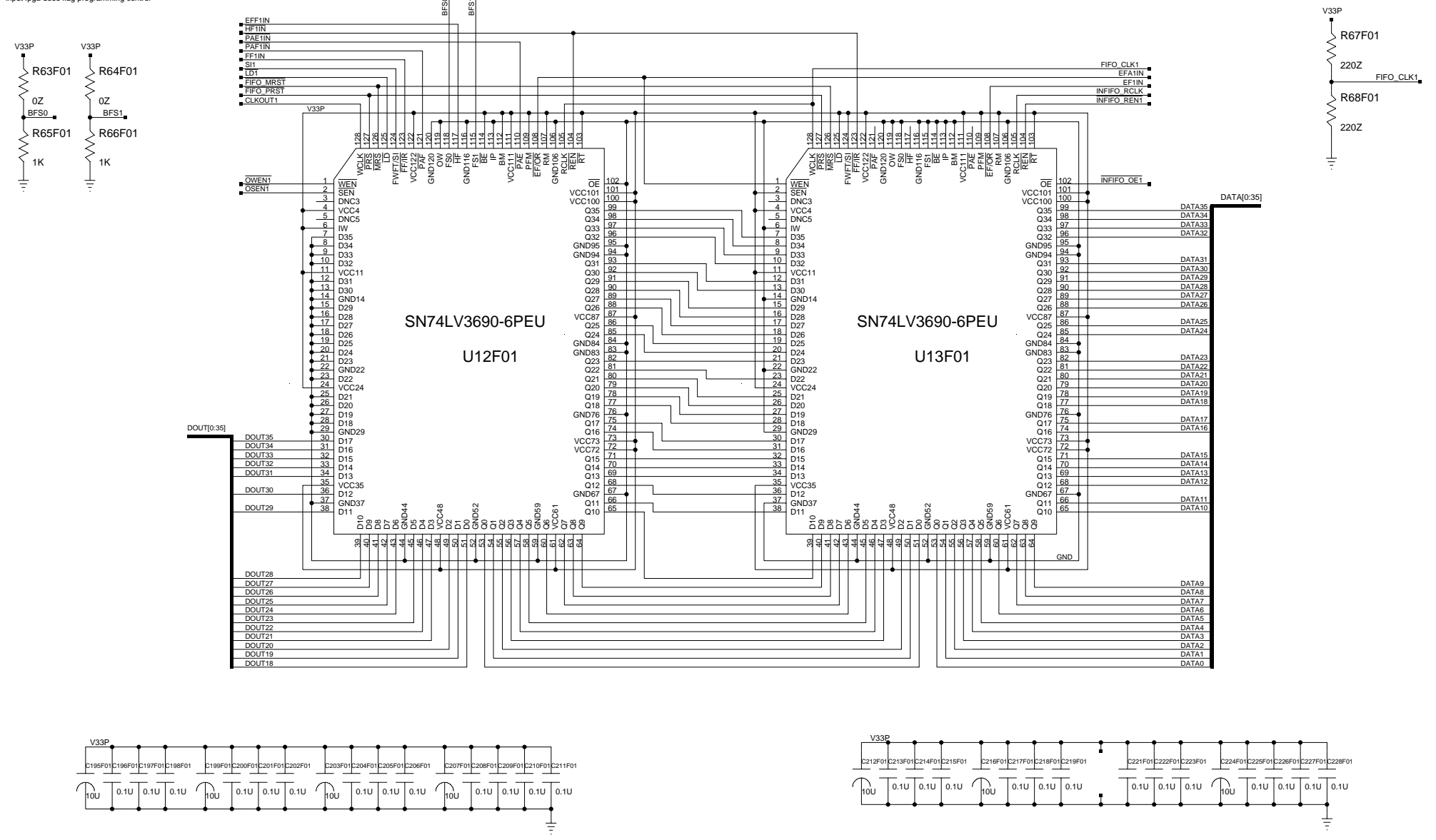
XC2VP20-5FG676C LOGIC = D785B







add four interface lines between incrl and vme / input fpga
input fpga does flag programming control

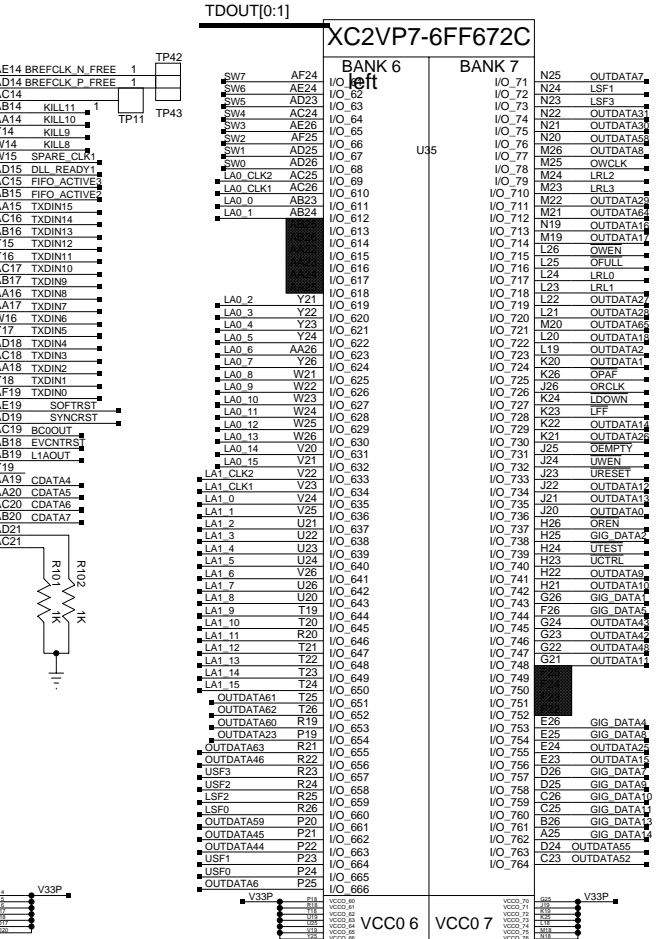
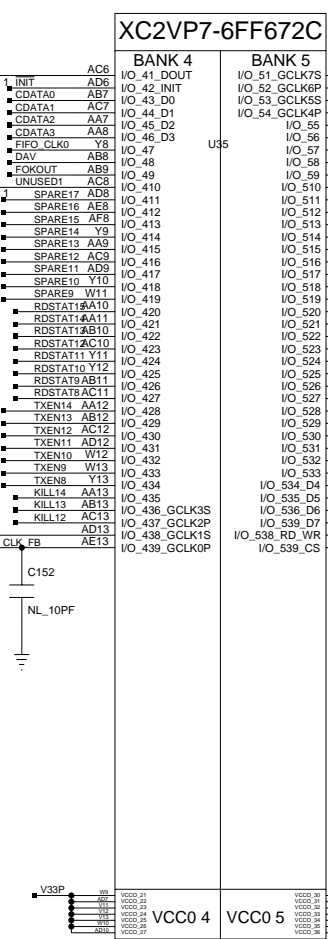
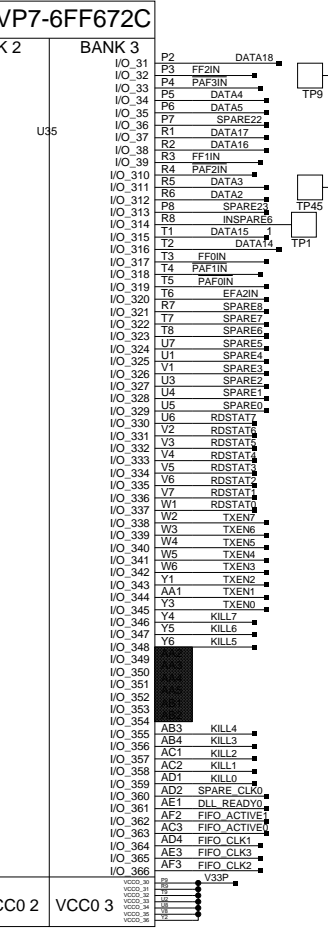
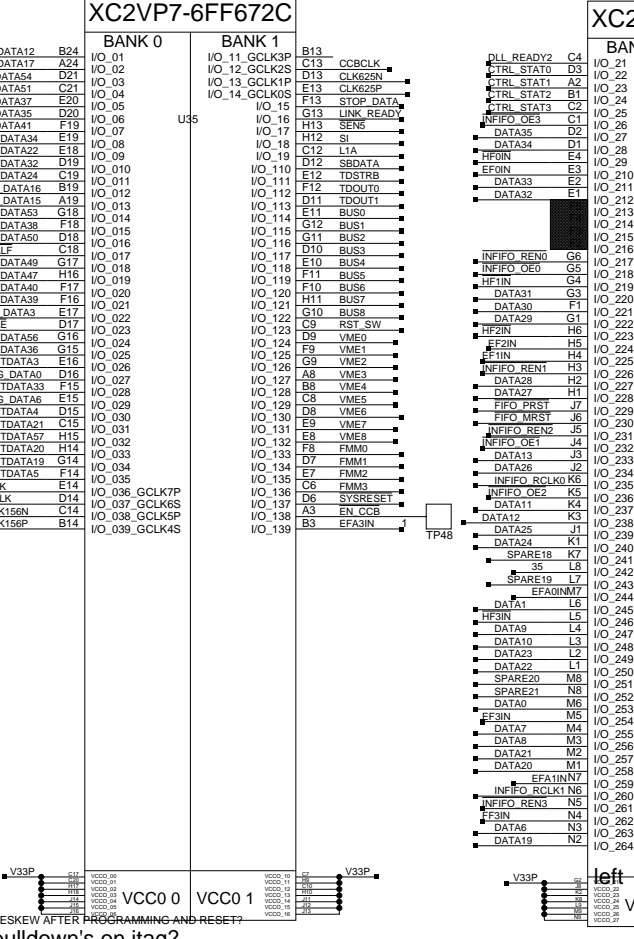
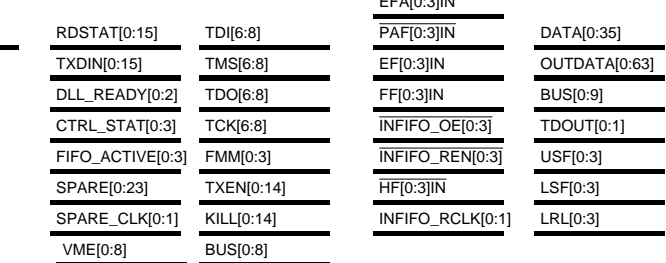
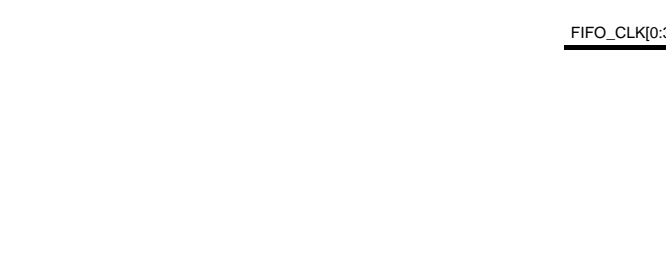
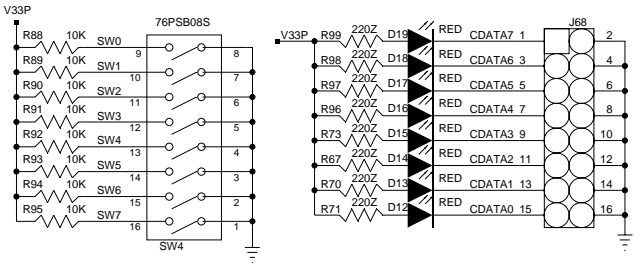


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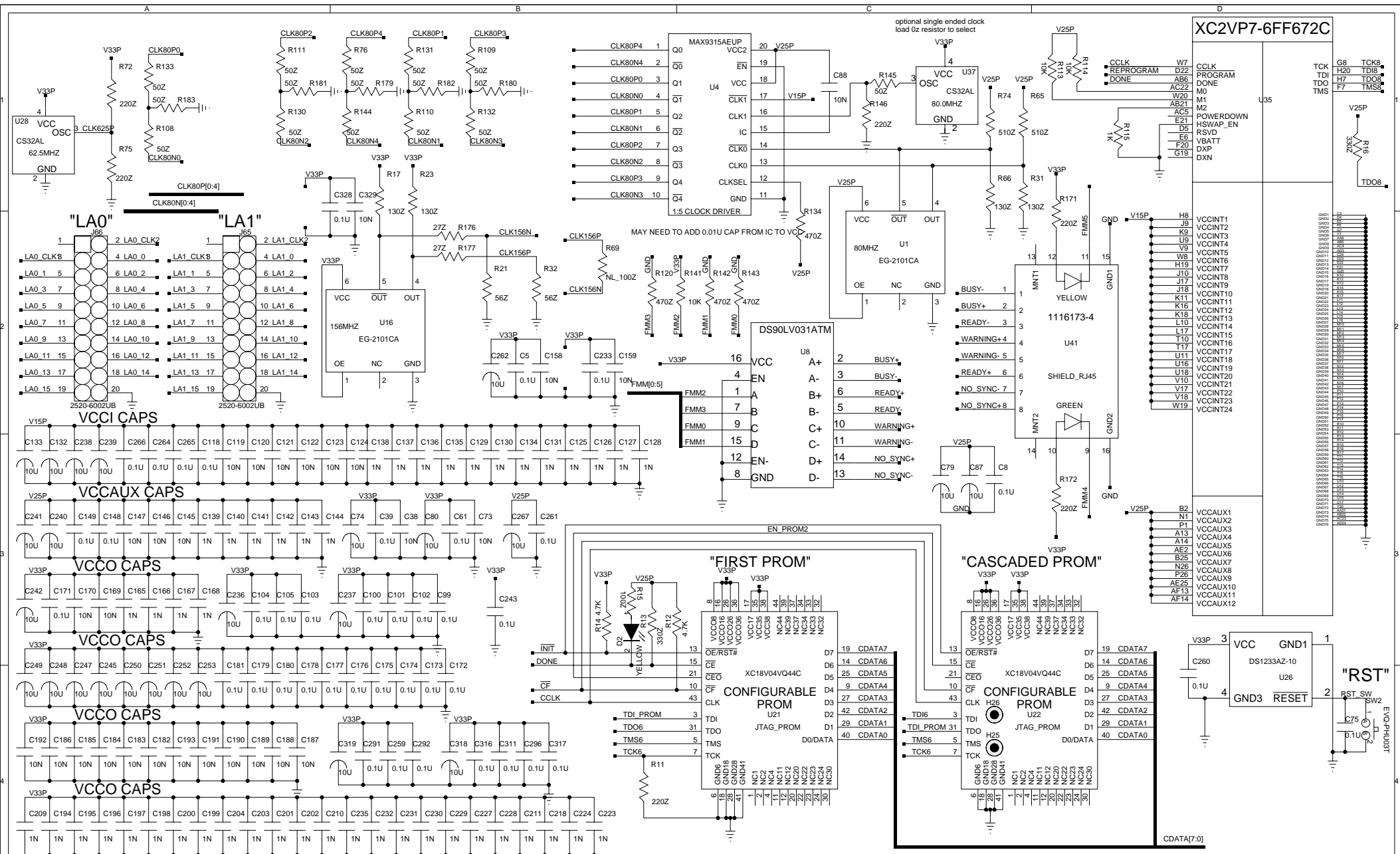
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OPTICAL TRANSCEIVERS AND ROCKET I/O
FULL DDU
CMS CSC ELECTRONICS

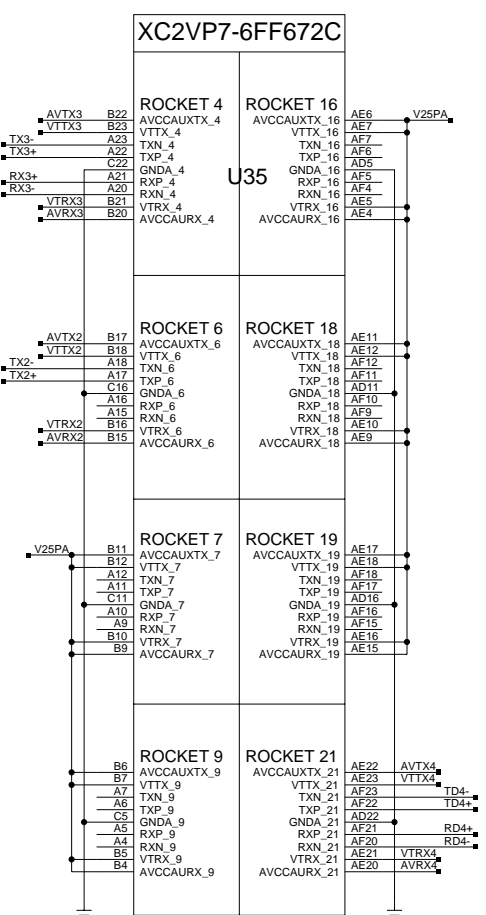
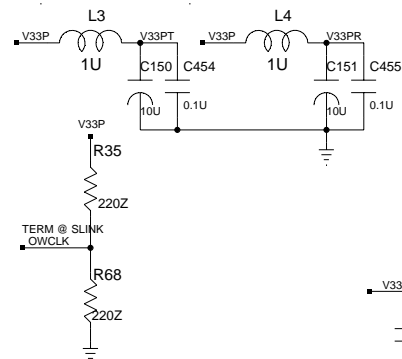
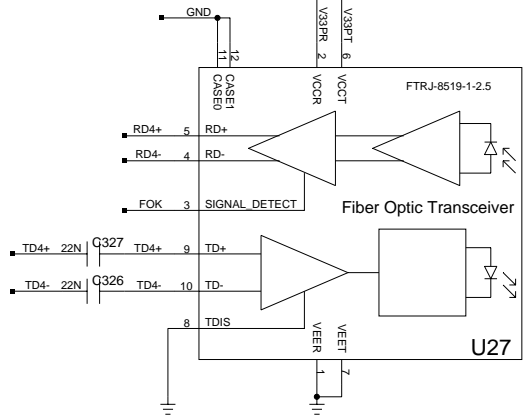
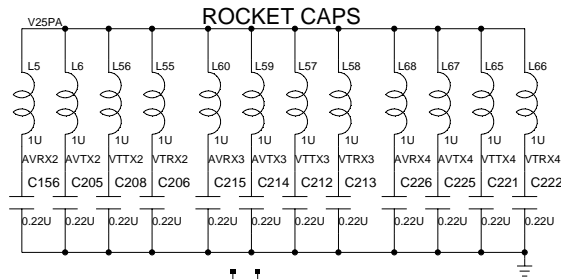
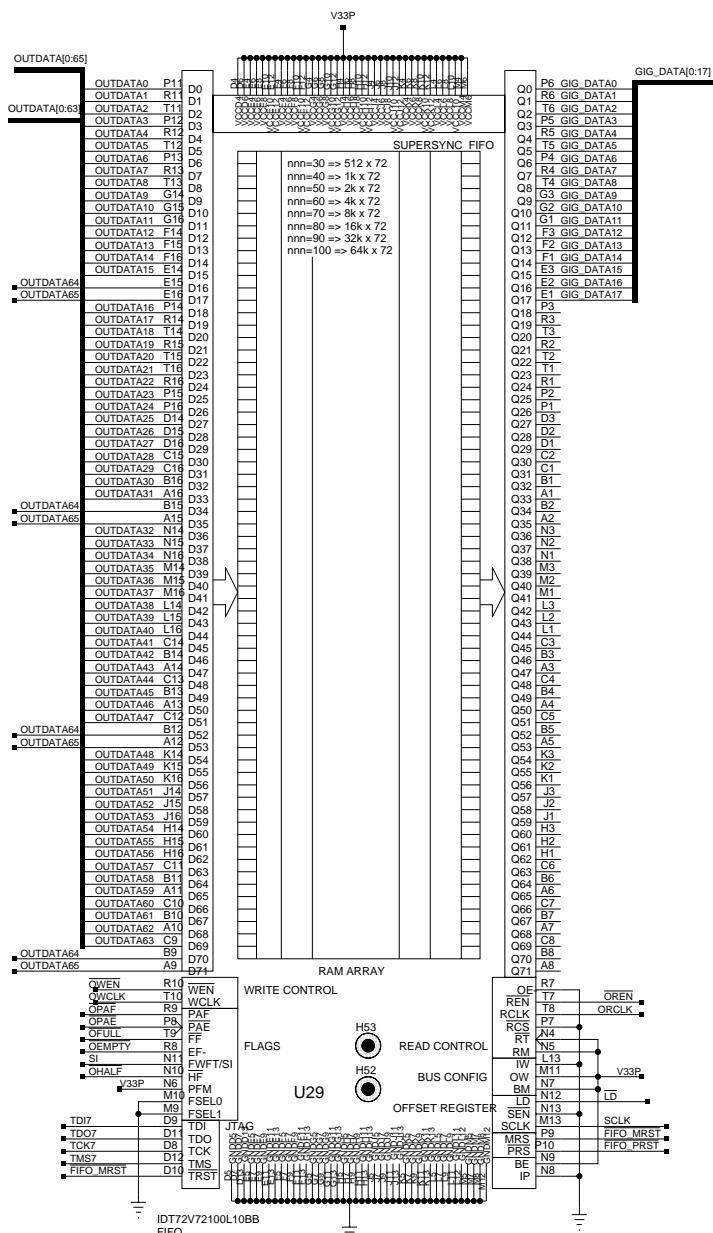
BY DCH
DATE 6-2-2005_14:10

PROJECT D785T
FILE INPUTF01 . 5 PAGE 2J



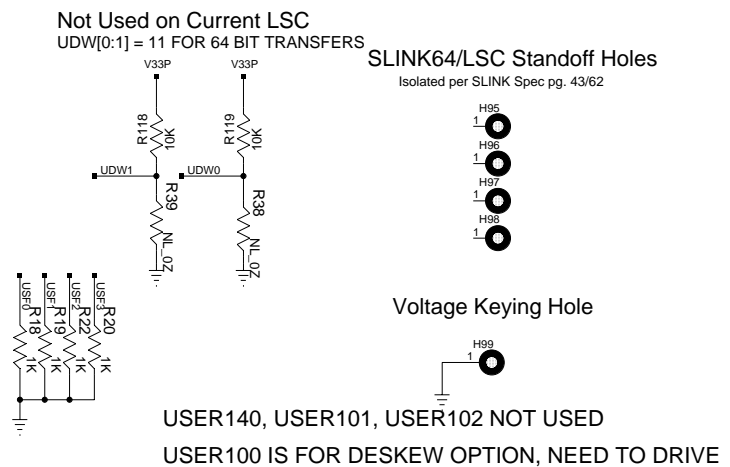
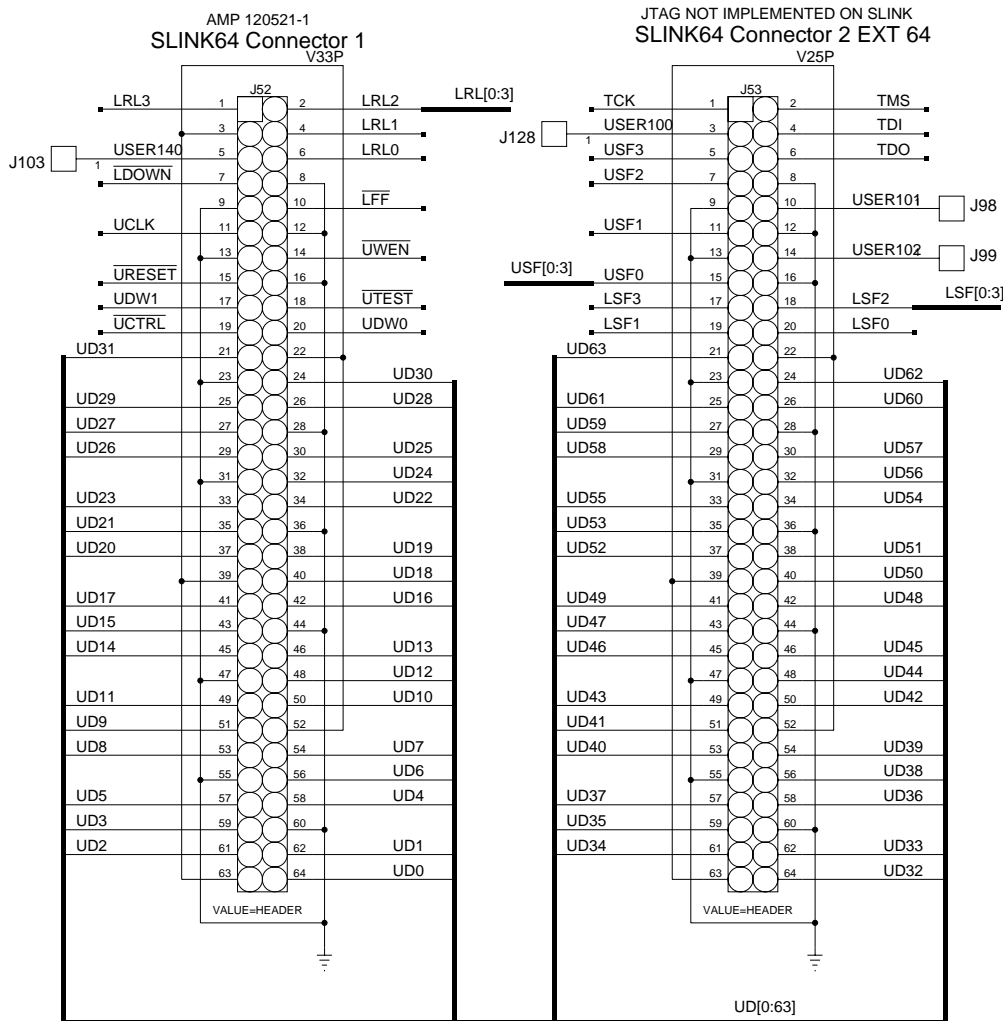
DESKWIP AFTER PROGRAMMING AND RESET?
pull-down's on jtag?

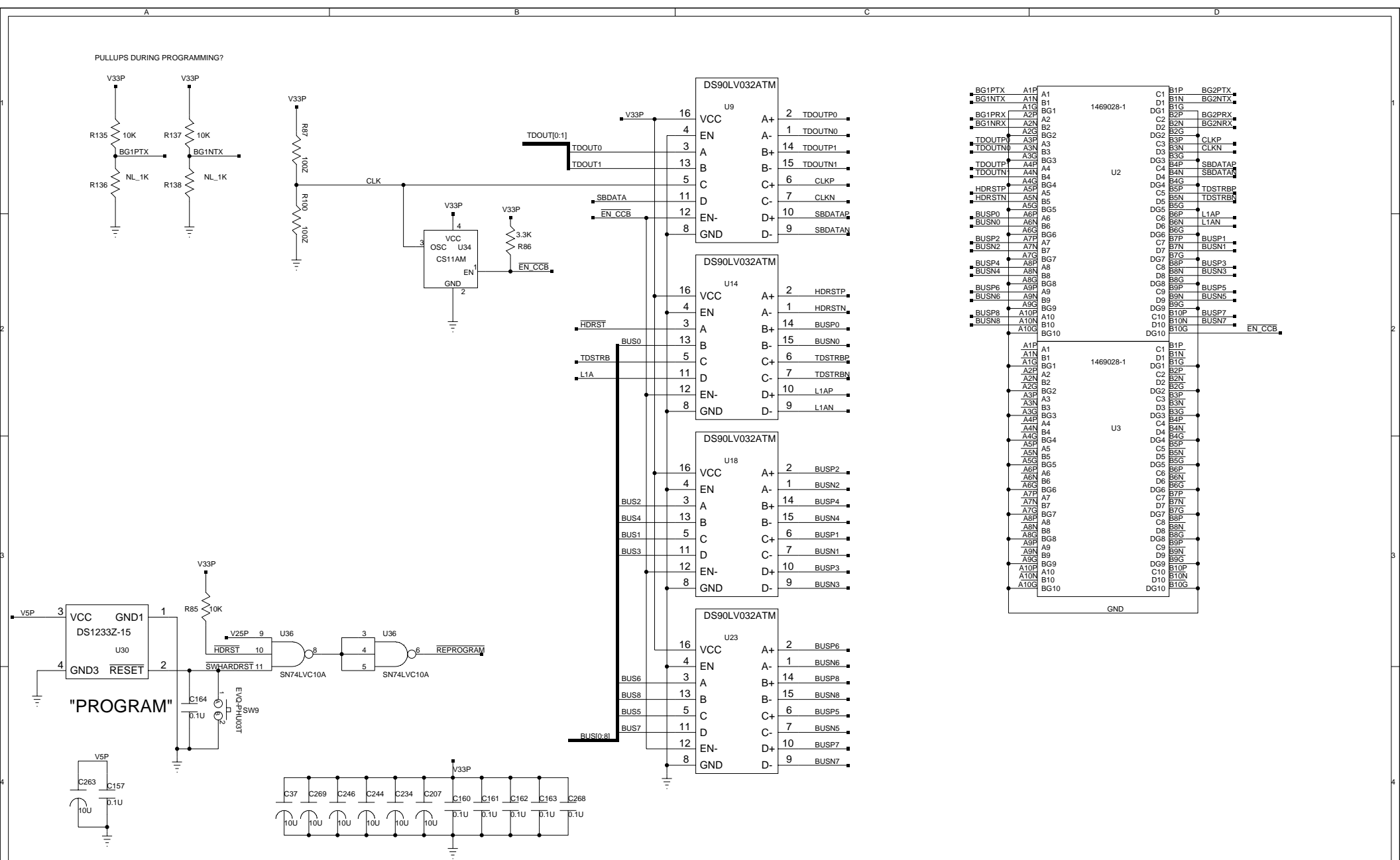


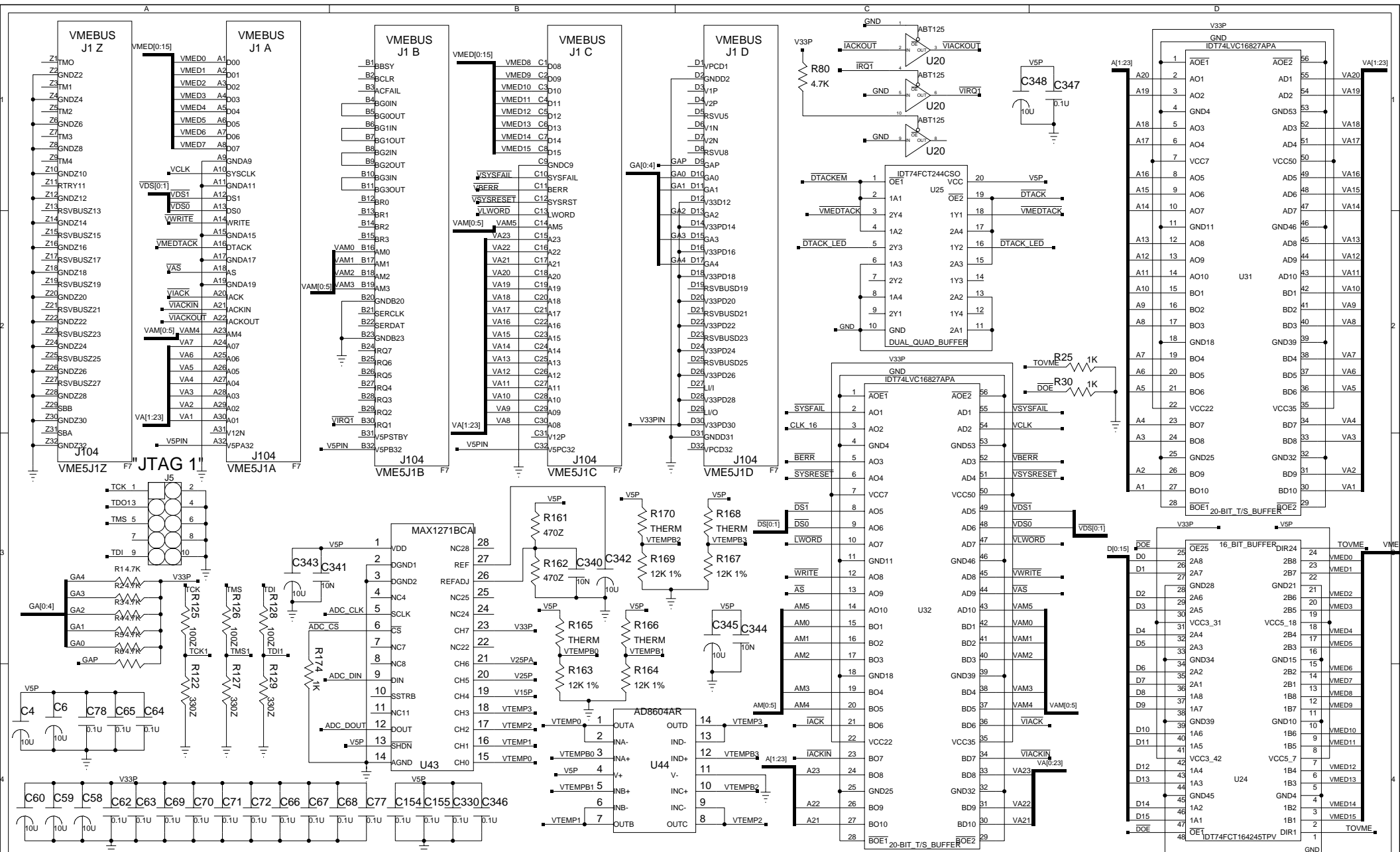


old ethernet had 66 bits. this won't work. add back to fpga 17 bits or remove two input bits.

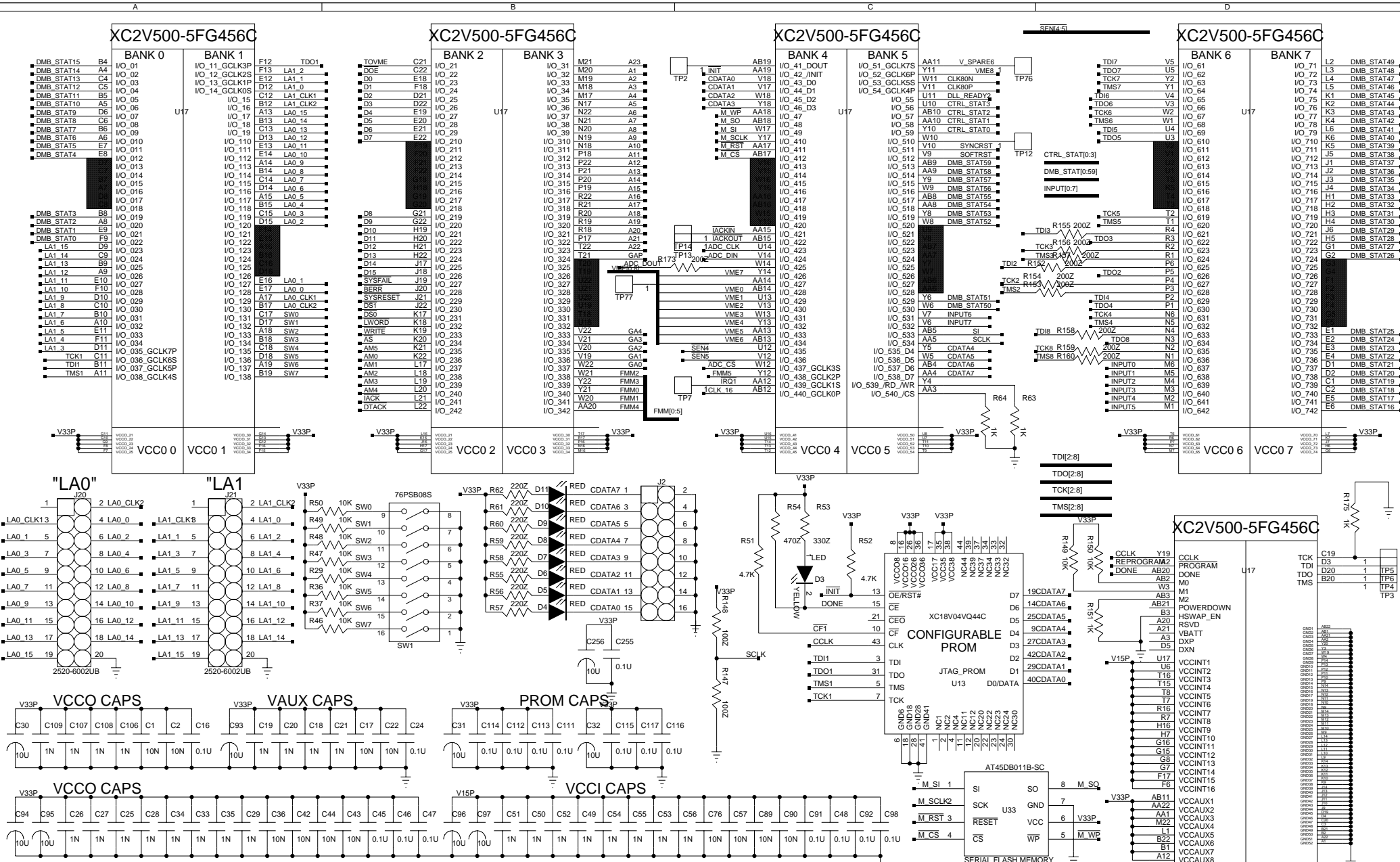
Implement basic S-LINK architecture on DDU board?







XC2V500-5FG6456C LOGIC = D785D



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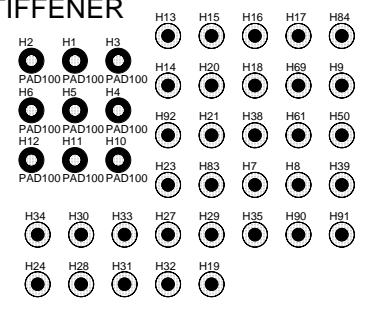
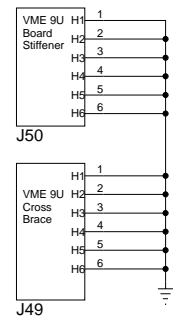
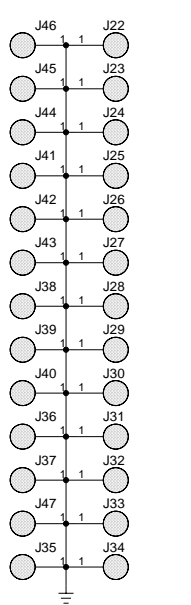
TITLE Power, Ground, stiffener
 Practice Full DDU
 CMS CSC ELECTRONICS

BY DCH
 DATE 6-2-2005, 14:24

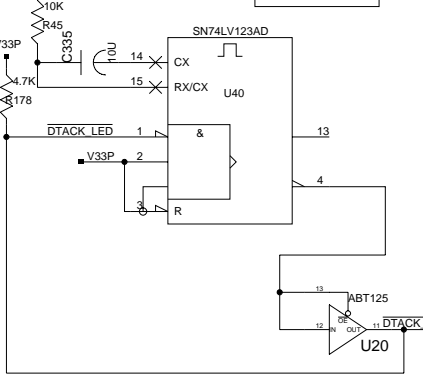
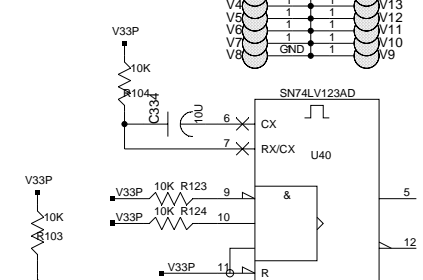
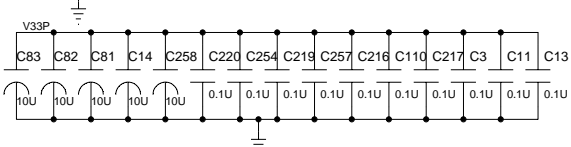
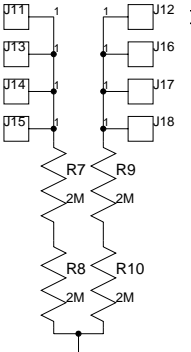
PARENT PAGE 1
 PROJECT D785T
 FILE VME. 2
 PAGE 9

GROUND POINTS BOARD STIFFENER

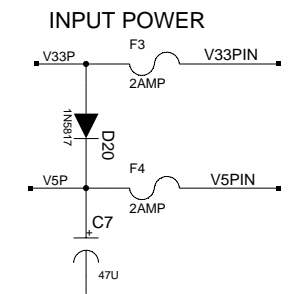
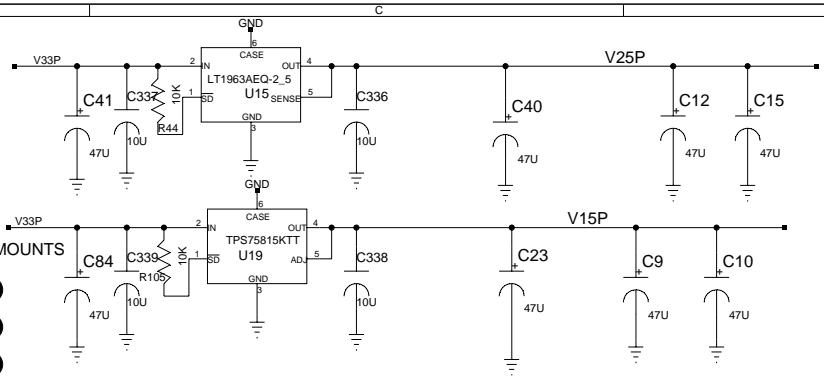
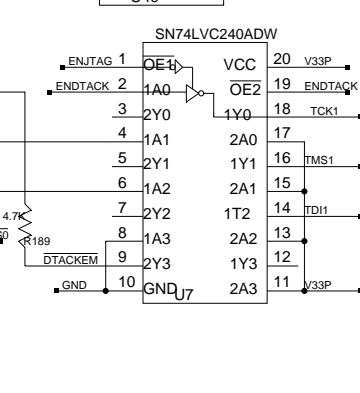
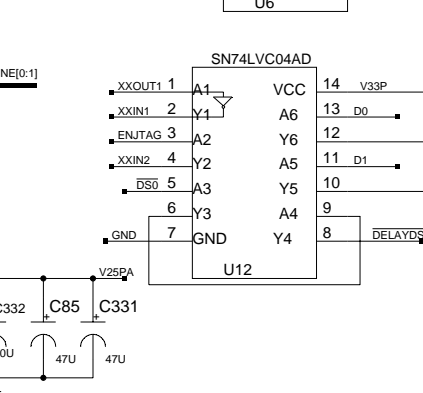
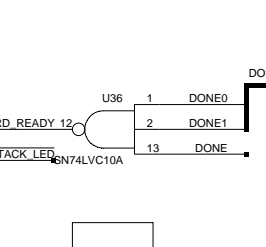
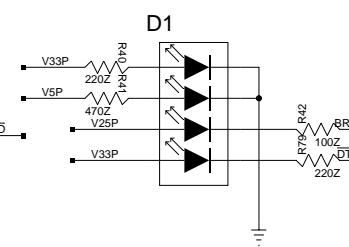
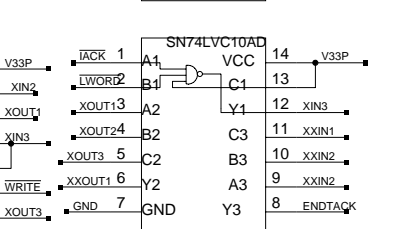
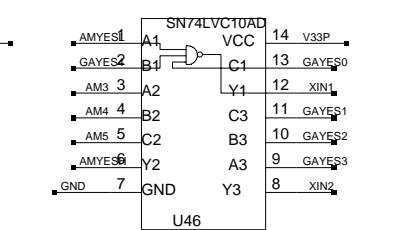
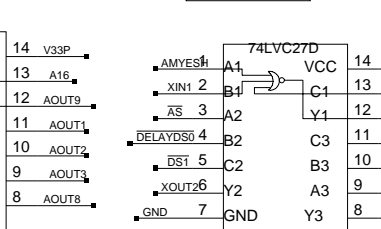
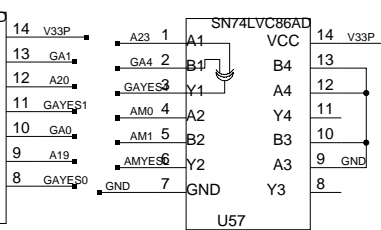
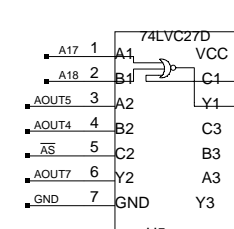
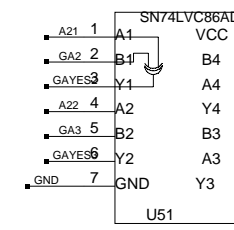
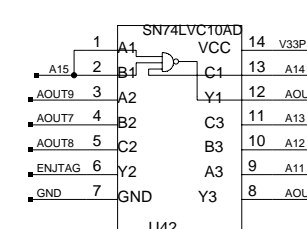
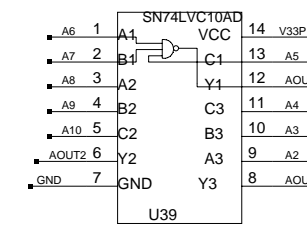
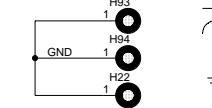
PART FIDUCIALS



DISCHARGE UNIT



FRONT PANEL MOUNTS



Discrete logic to load the VPROM in emergency