D785T

CMS CSC DDU VERSION 6

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210
UPDATES TO D785N

80 MHz Clock Terminations
/BE on FIFO SET #3
PCB Layout Copper PIN Clearance
ADD 1N5817 Diode between powers
Add IAKOUT
IRQ (open collector)
IACK
Fix cap/resistor space on bottom side of PCB
Emergency VME Logic. Add /AS
add logic for dtack. To keep the light on if stuck low.
add four interface lines between inctrl and vme / input fpga
input fpga does flip programming control
old ethernet had 66 bits. this won't work. add back to fpga 17 bits or remove two input bits.
Implement basic S-LINK architecture on DDU board?

SLINK INTERFACE
Practice Full DDU
CMS CSC Electronics

Not Used on Current LSC
UDW[0:1] = 11 FOR 64 BIT TRANSFERS
SLINK64/LSC Standoff Holes
Isolated per SLINK Spec pg. 43/62

Voltage Keying Hole

USER140, USER101, USER102 NOT USED
USER100 IS FOR DESKEW OPTION, NEED TO DRIVE