DDU_04 and DCC Development

- Where are the DDU and DCC
- DDU/DCC crate and backplane
- DDU and DCC Functions
- Prototyping
- Status

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Where are the DDU and DCC

- 540 DMB as inputs (160MB/s)
- 8 SLINK64 as outputs (800MB/s)
- Expected data rate 1.2 GB/s
DDU/DCC Crate

- Four 9U Crates
  9U X 220mm Board
- Data Concentration:
  15 DMB to 1 DDU
  9 DDU to 1 DCC
  1 DCC to 2 SLINK64
  9 DDU per SLINK (4)
  4/5 DDU per SLINK (8)
  2/3 DDU per SLINK (16)
  1 DDU per SLINK (36)
  36 DDU, 4/8 DCC needed

Base-line design Optional
DDU/DCC custom backplane

- VME P3 spaces
- 6.4 Gbps rated connector
- Data from DDU to DCC
- TTC control bus (clock, L1A, command/data)
DDU-04 Function

- Collect data from 15 DMB (15*160MB/s), Send data to DCC (640MB/s)
- Check data, Detect error, send to FMM
- Spy data by Gigabit Ethernet
- Capable of SLINK64

Improvements over DDU-02:
- Earlier error detection
- Better PCB timing
- More reliable
- Higher effective data bandwidth
DCC Function

- Merge data from 10 DDU (10*640MB/s), send to CMS DAQ SLINK64 (2*800MB/s)
- Receive and fan out TTC fast control for the crate
- Spy data by two Gigabit Ethernet links
- Expected:
  - Constant 800MB/s on SLINK64
  - >100MHz DDR FIFO
  - extra 1MB buffer for the SLINK64 error detection ability
Prototyping

- With Virtex2 Pro FPGA (XC2VP2-5FG456):
  DMB to FPGA
  FPGA to Gigabit Ethernet
  312MB/s per link with the backplane
  Technology OK

- With DDU-02:
  Error checking
  SLINK64
Status

• PCB layout: Working on
• FPGA firmware: Being Developed
• System will be ready before 2004 slice test

We are confident in the design
We are working hard on the system