EndCap Muon DDU

Summary and Status
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DDU Test Board

Goals:

• Learn PCI
  ◦ AMCC S5933 PCI Controller

• Explore Fiber Optics
  ◦ HP G-Link: 75 MHz/16-bit, i.e. 1.5 Gbaud
  ◦ HP Optical Transceiver
  ◦ Duplex Fiber Link, 125 meters long
Software versus Hardware

• DDU only a buffer between 75 MWord/s Optical and 66 MWord/s (33 MHz) PCI

• No TTC, no error checking; no processing

• Custom Linux device driver also does very little manipulation of data stream

• ‘User’ level routines check
  ◦ integrity of header word information
  ◦ encoded CRC information (CFEB only)

Data Format

• 16-bit “Word” naturally fits into 32/64 bit PCI
• One bit of every word reserved for Control
  ◦ Control Bit = 0: 15-bit data (depends on subcomponent)
  ◦ Control Bit = 1: Special Control Word; 3 more bits reserved for control designator, 12-bit data
System Arrangement

- Intel/Linux System with 32-bit/33 MHz PCI
  - Custom DDU Device Driver
- DDU Prototype (with FIFO buffering and AMCC)
- Duplex 125-meter multi-mode optical fiber
- EMU DAQ Motherboard & Front End Components
Implementation
Implementation

Data Path in Testbeam ‘99 Version

- PCI: AMCC S5933 with built-in 8X32-bit FIFO Interface; Chip level DDU reset, Mailbox status

- Cascaded external IDT SuperSync FIFO (64kX16-bit on receive) – most expensive single component on board

- HP G-Link and transceiver running at 75 MWord/s (1.5 Gbaud) in full duplex mode

Number of Channels, etc.

- Channels/FE Chip: 16
- FE Chips/Front End Board (FEB): 6*
- FEB/DAQ Motherboard: 4-5 Cathode + 3-7 Anode
- DMB/DDU: Maybe 4? Depends on FED
- DDU/RUI: Maybe 4? Depends on DDU & FED

- APPROXIMATE Total (too many chambers?):
  540 Chambers = 612 DMB = ~160 DDU = ~40 RUI

* An alternate AFEB plan is considered, with 1 chip per FEB, but then 18 - 48 AFEB/DMB
Balance Costs and Performance

• Averaged chamber rate of 6 MB/s:
  ◦ Level 1 Trigger rate: 100 kHz
  ◦ CSC Chamber have data 3% of the time
  ◦ Average Event Size is ~ 1 kWord = 2 kB

• Roughly 1/16 DMB are active at any time:
  ◦ 1/30 (3%) DMB have data for each trigger
  ◦ ~20 μs to read typical event on 120 MB/s link
  ◦ 120 MB/s rate matches nominal PCI
  ◦ Perfectly arranged, 16 DDU per PCI bus
  ◦ More likely <8/bus with bus sharing

• Reality: bus arbitration, address cycles
  ◦ At most 4 64-bit/66 MHz 4-DMB DDUs could share one FED carrier board
  ◦ However, (FIFO) width costs more

• Decisions, decisions...
  ◦ What is the FED arrangement? Guidance?