

D785U

CMS CSC Data Concentrator Card (DCC) PCB Schematic

Version 4

MBRD\_BLK

ELECTRONICS LAB  
PHYSICS DEPARTMENT  
THE OHIO STATE UNIVERSITY  
174 WEST 18TH AVE  
COLUMBUS OHIO 43210

## DCC: It Collects 9 DTB data, and sends to CMS main DAQ via one or two S-LINK64 interfaces

June 9, 2003: Initial drawing, June 23, Need more check  
June 26, 2003: Power and ground design  
July 28, 2003: Copy the project from cmspc003:\wvdesign\dccp\ to m:\wv\d785\d785g\  
July 31, 2003: Added six 100 Ohm resistors for clock termination  
Aug. 14, 2003: Add a clock driver MAX9310 for RocketIO reference clock  
Apr. 1, 2004: Modifications according to the ver1 tests  
Apr. 6, 2004: Main FPGA pin re-assignment, and TTC backplane signal switching  
Apr. 7, 2004: Change the hard\_reset logic.  
June 15, 2005: Re-arrange the CMS\_CLK, and L1A distribution,using 74fct20807 buffer  
July 9, 2004: Final check on the schematics, tie FIFO TRST LOW  
Jan. 28, 2005: replace the IDT72T40118 with IDT72V36110, start rev3 DCC  
Feb. 2, 2005: removed the Program data line LEDs (16 in total)  
Feb. 21, 2005: Add buffers for SLINK

Aug. 31, 2005: Added /AS to Emergency Load Logic  
Aug. 31, 2005: Changed FMM LED Power from V3PIO to V33P  
Aug. 31, 2005: Added thevinin terminator to TCMSCLK  
Sept, 6, 2005: Added series LED to V5PRAW Front Panel LED  
Sept, 6, 2005: Changed V5PRAW, SLDONE, RXDONE LED current limiting resistor to 330z  
Sept, 6, 2005: Added (10) 10uF tantalums to the Analog FPGA 2.5V powers  
Sept, 7, 2005: Increased size of P1 Test Port Power Trace  
Sept, 7, 2005: Converted all regulator back to the adjustable type (placement and ordering purposes)  
Sept, 7, 2005: Added (20) 220nF caps to the input FPGA's  
Sept, 7, 2005: Added (7) 220nF caps to the control FPGA

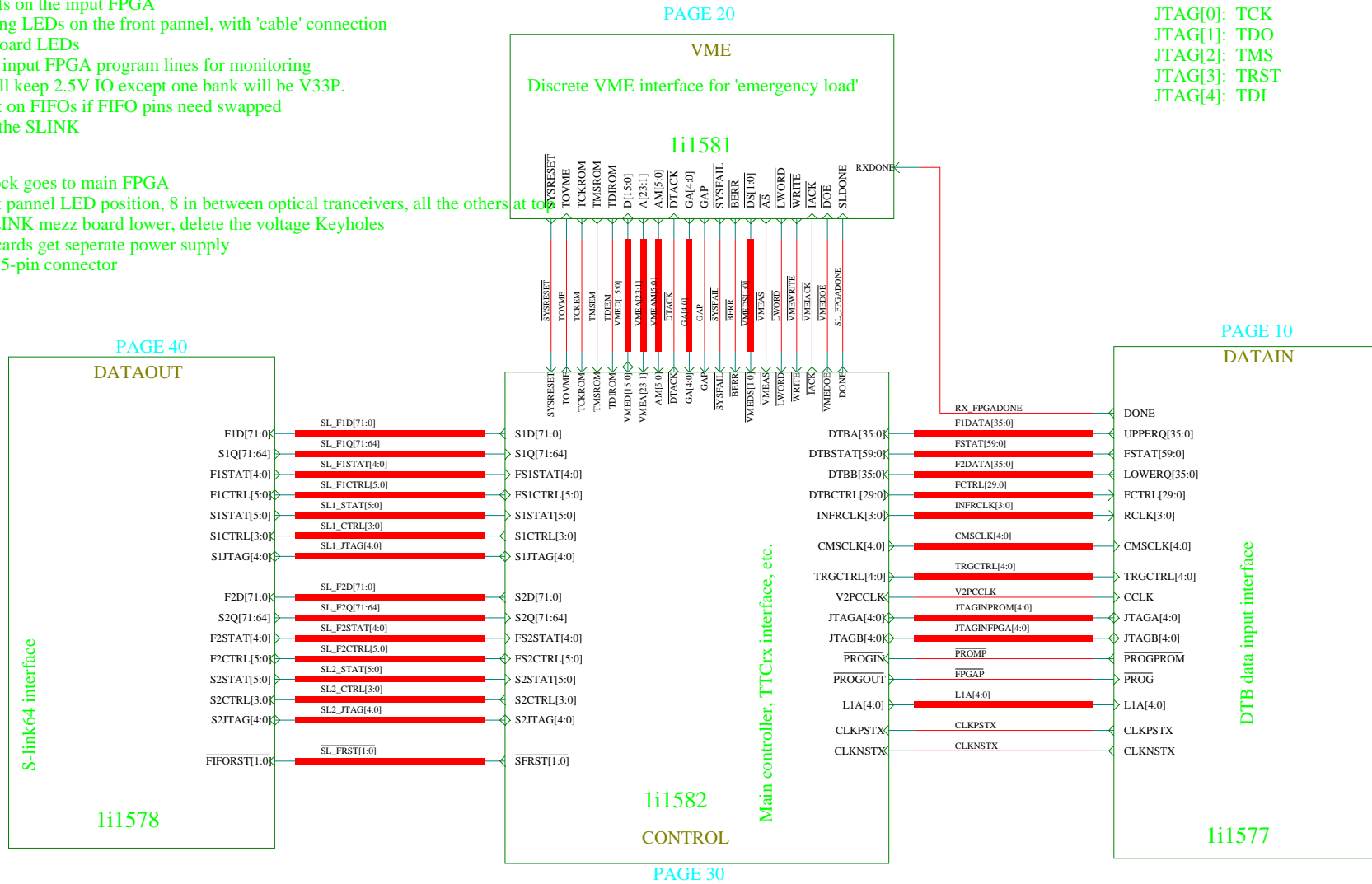
ELECTRONICS LAB  
PHYSICS DEPARTMENT  
THE OHIO STATE UNIVERSITY  
174 WEST 18TH AVE  
COLUMBUS OHIO 43210

Major changes for rev3:

1. Main FPGA uses V3PIO. 3V compatible IOs
2. Use IDT72V36110 FIFOs, remove the IDT72T40118 fifos
3. Add many test points on the input FPGA
4. Add many monitoring LEDs on the front pannel, with 'cable' connection
5. Remove all the in-board LEDs
6. Add a buffer on the input FPGA program lines for monitoring
7. The input FPGA will keep 2.5V IO except one bank will be V33P.
8. Add some aux point on FIFOs if FIFO pins need swapped
9. Add buffers before the SLINK

Minor changes for rev3:

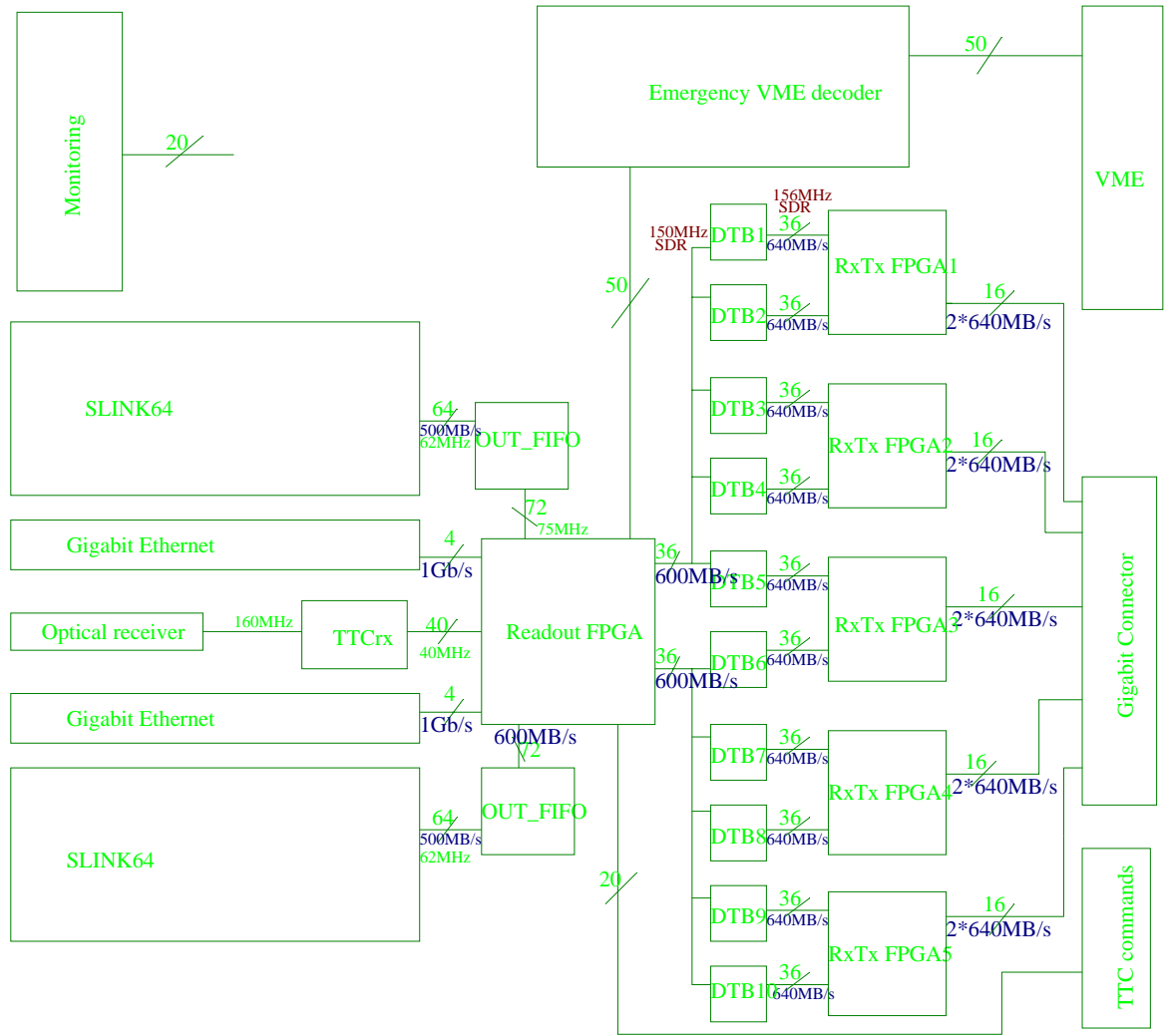
1. the 156.25MHz clock goes to main FPGA
2. Re-arrange the front pannel LED position, 8 in between optical tranceivers, all the others at to
3. Move the upper SLINK mezz board lower, delete the voltage Keyholes
4. The SLINK mezz cards get seperate power supply
5. Add a SLINK Jtag 5-pin connector

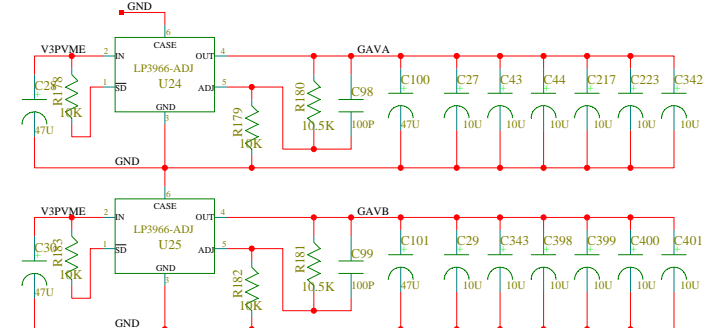
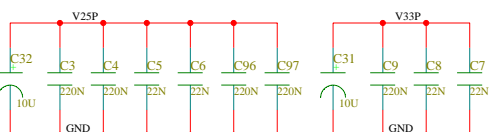
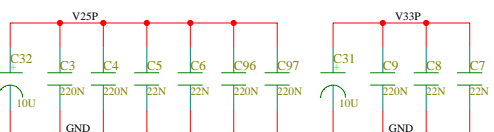
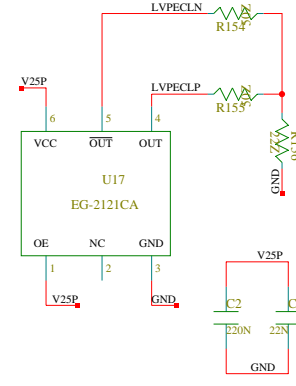
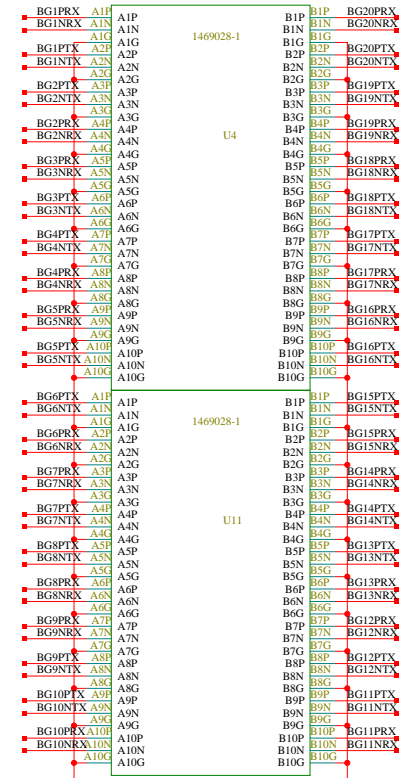
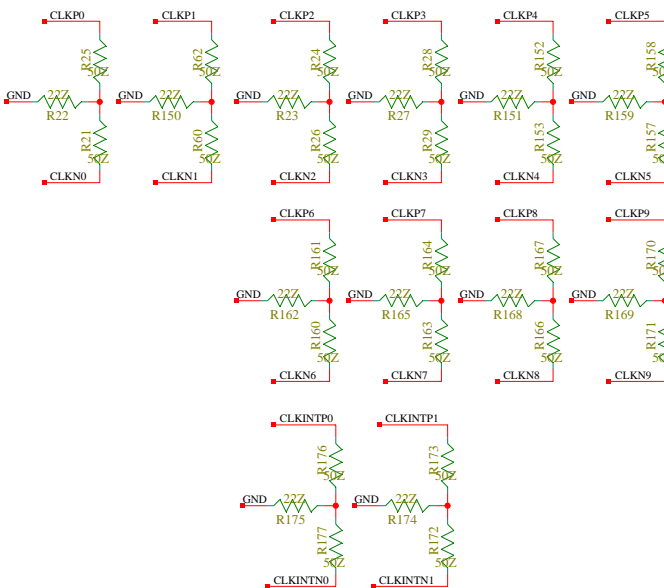
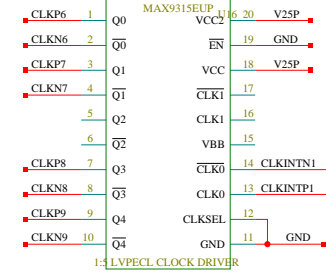
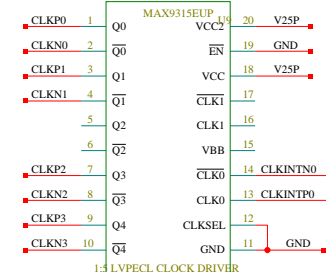
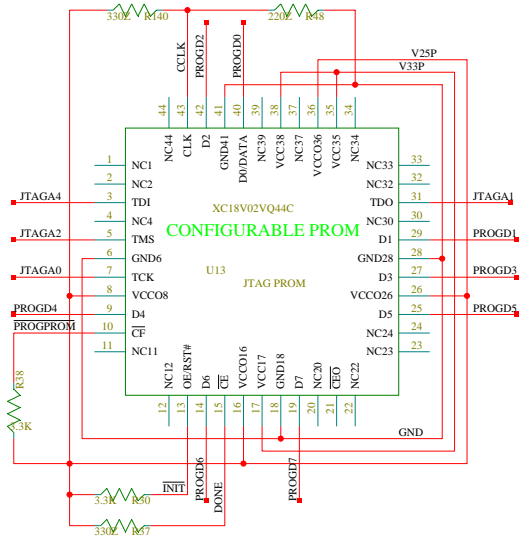
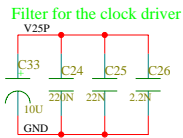
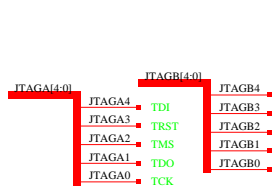


JTAG[0]: TCK  
 JTAG[1]: TDO  
 JTAG[2]: TMS  
 JTAG[3]: TRST  
 JTAG[4]: TDI

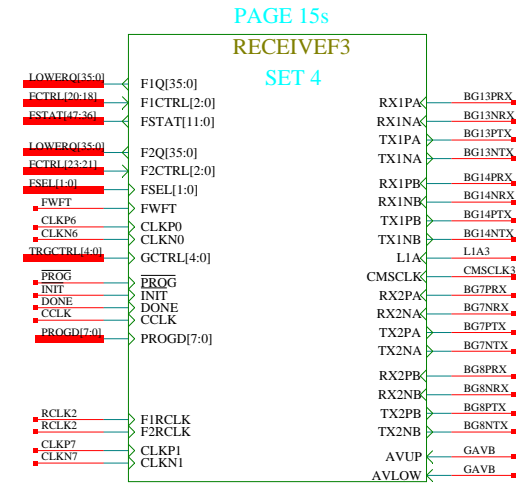
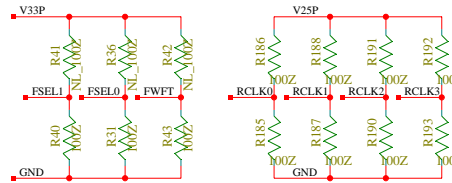
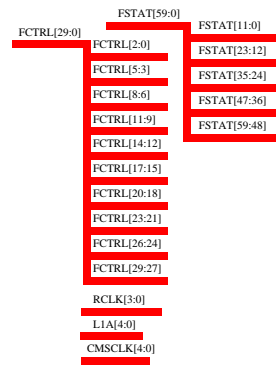
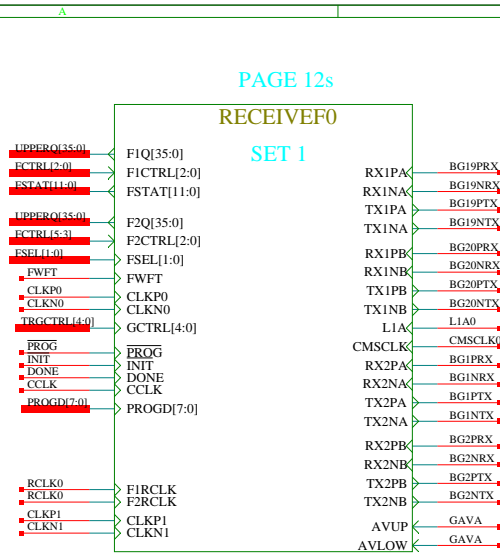
DCC layout and minimum signal required for data flow

DDDDD D DDDDD DDD D DDD  
 TTTTT C TTTTT TTT C TTT  
 BBBBB C BBBBB BBB C BBB

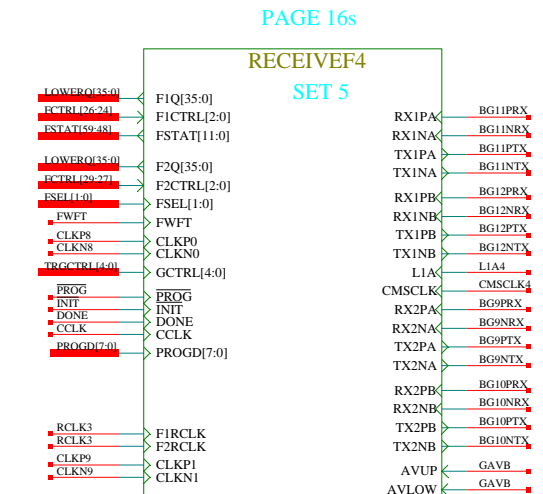
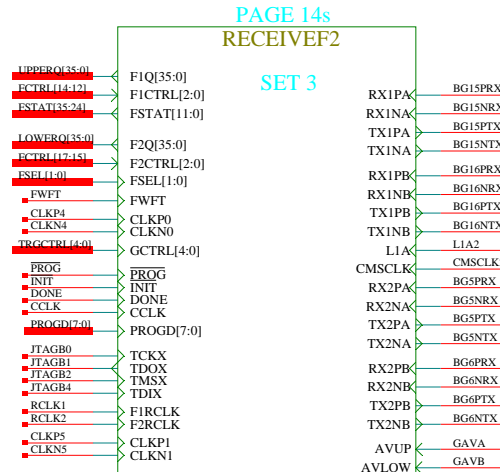
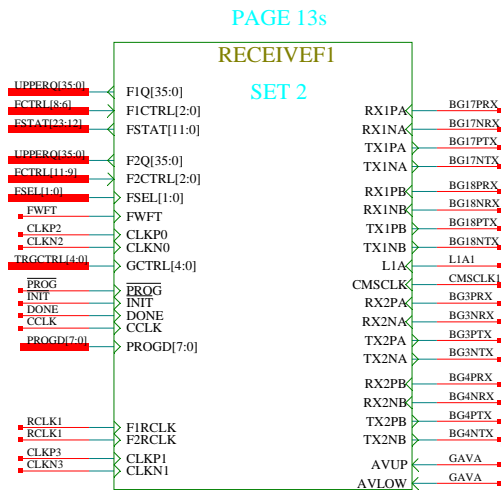




Dan: each regulator supply 2 1/2 FPGA for RocketIO power  
Paralleling the regulator is more complicated



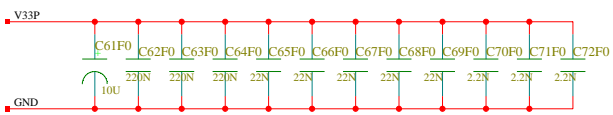
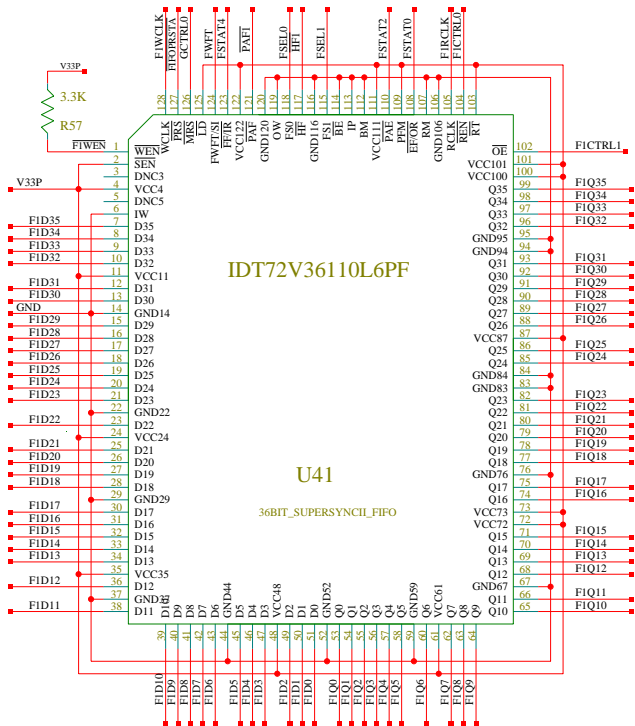
Set one bank on the FPGA to 3.3VIO (V3PIO), all the others remain 2.5V





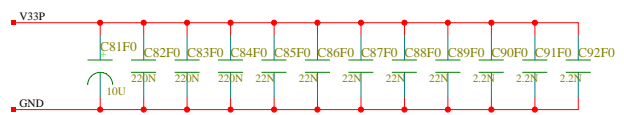
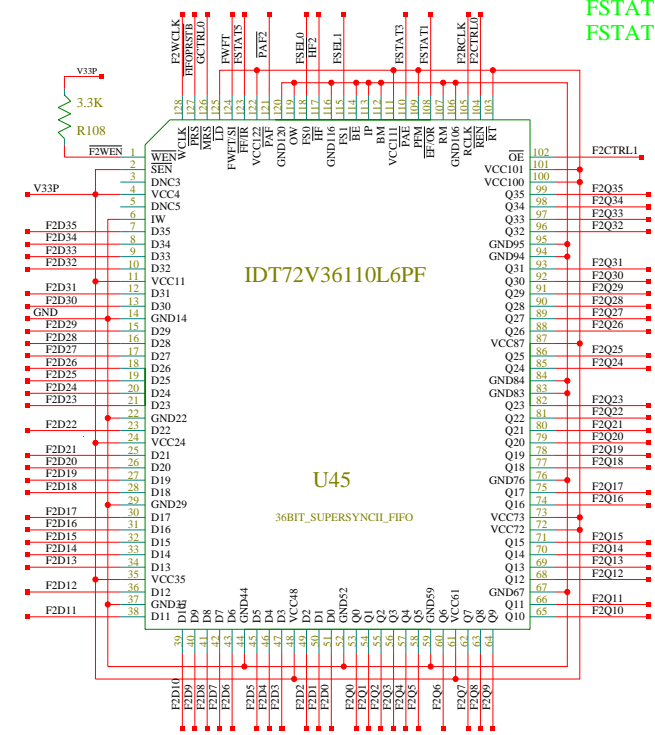


Fifo Setting  
36 bits IN, 36 bits OUT

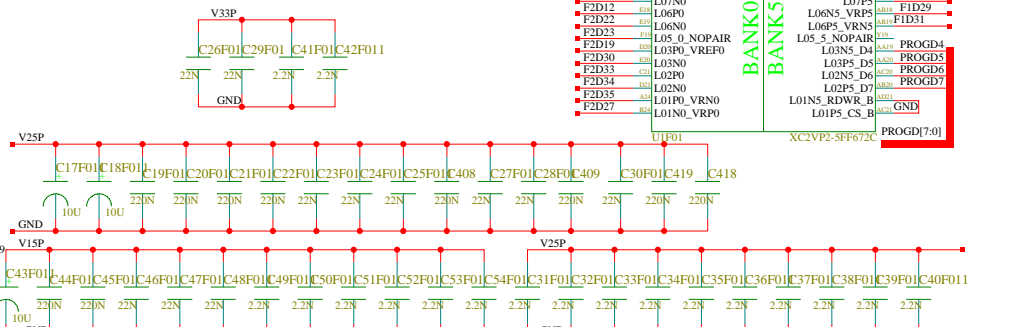
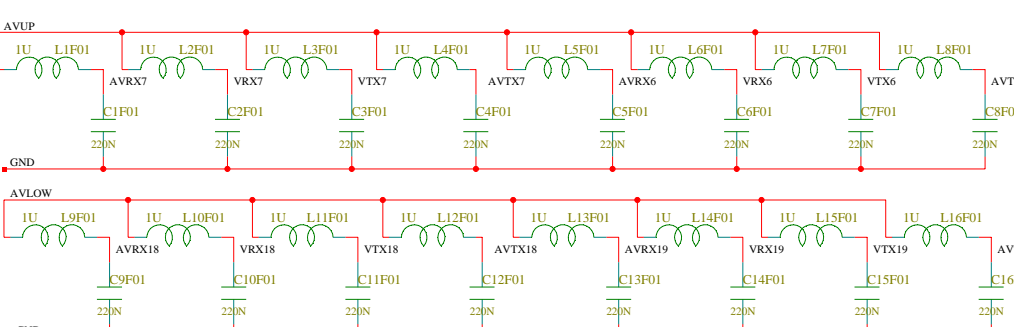
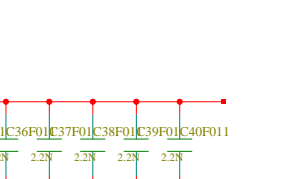
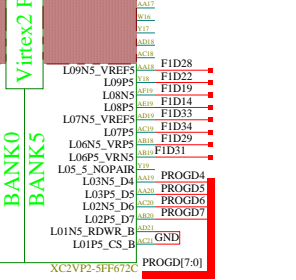
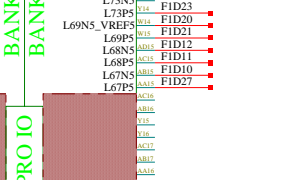
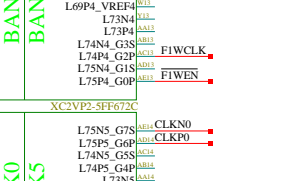
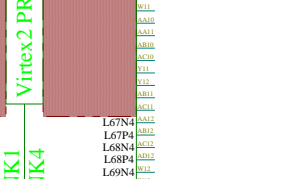
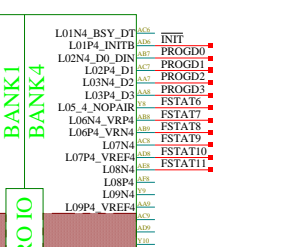
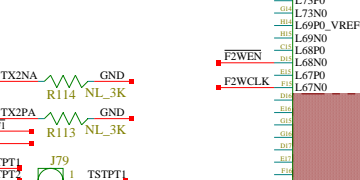
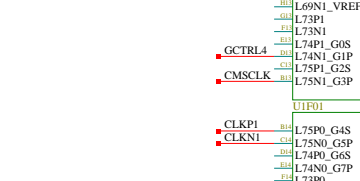
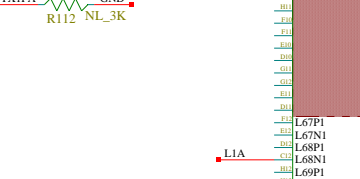
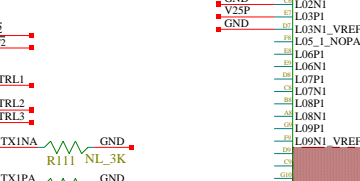
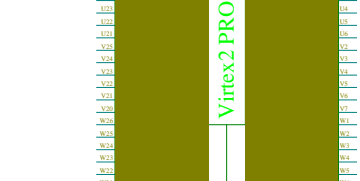
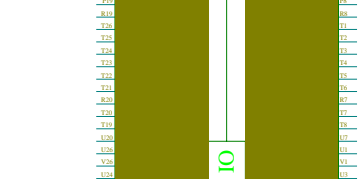
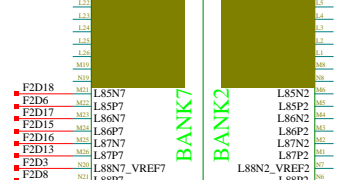
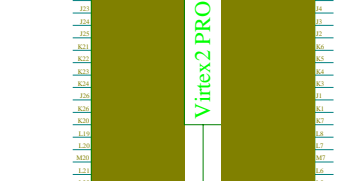
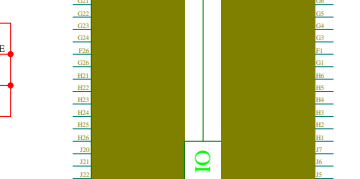
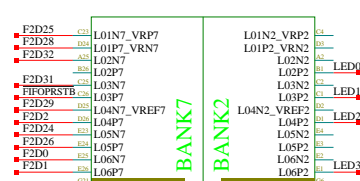
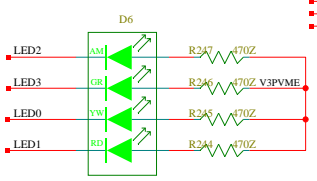
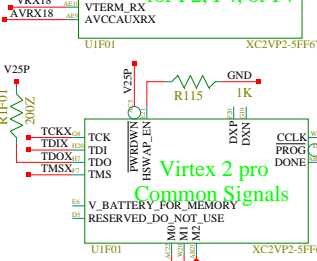
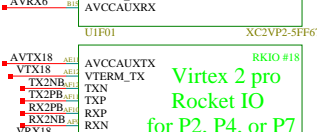
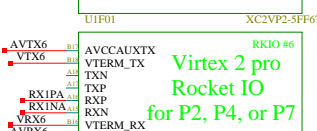
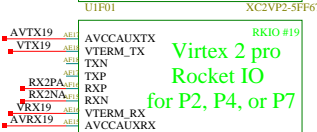
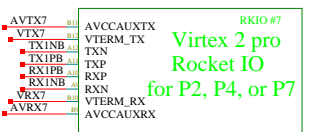


- FSTAT[11:0]
- GCTRL[4:0]
- FICTRL[2:0]
- F2CTRL[2:0]
- FSEL[1:0]
- F2D[35:0]
- F2Q[35:0]
- FID[35:0]
- FIQ[35:0]

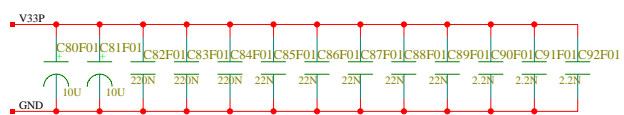
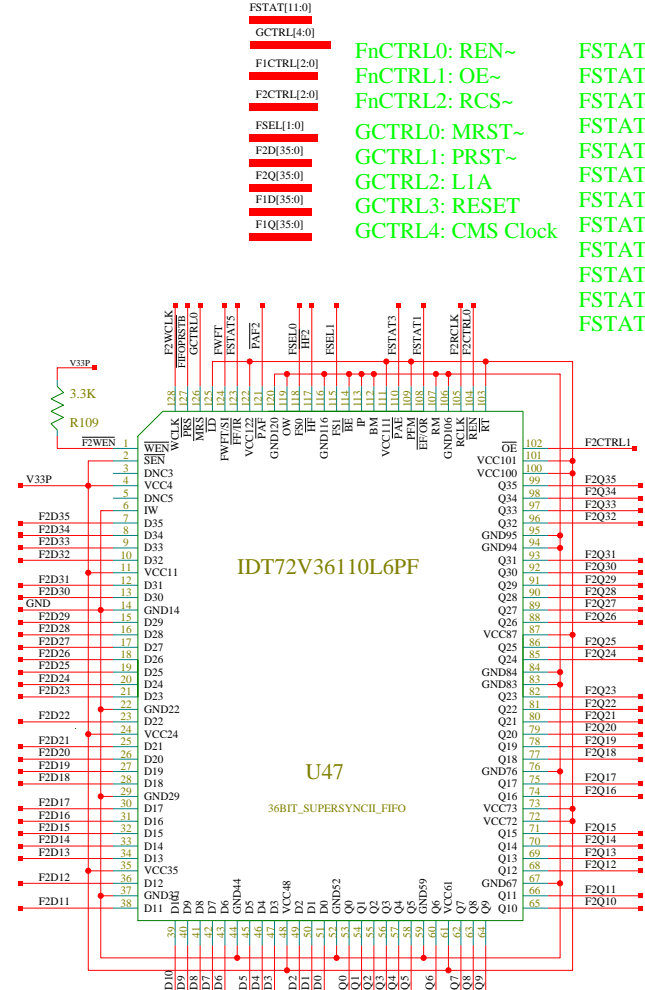
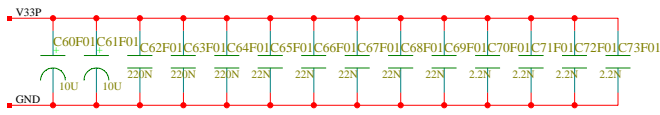
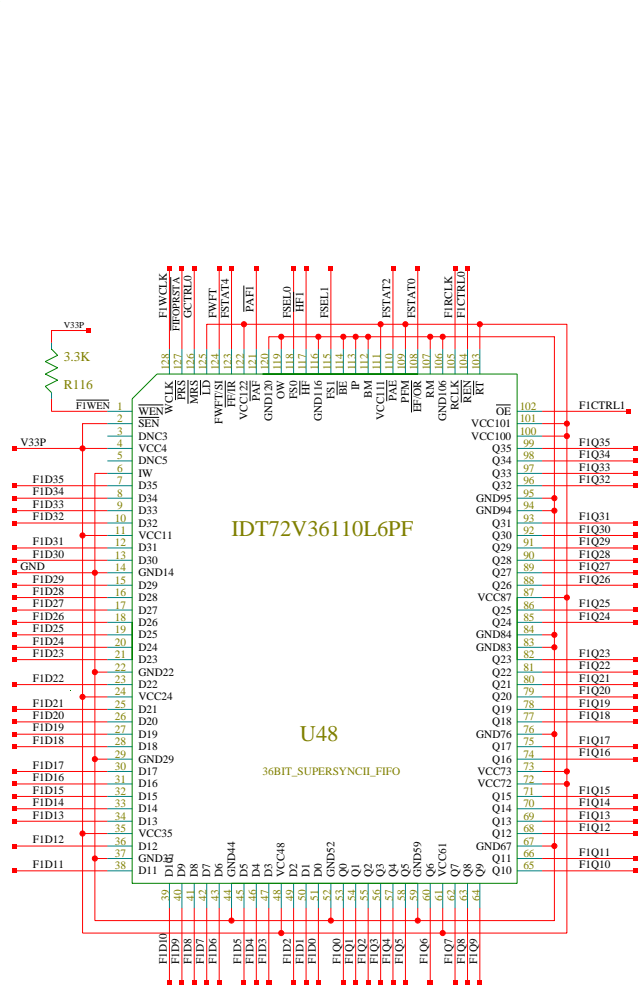
- FnCTRL0: REN~
- FnCTRL1: OE~
- FnCTRL2: RCS~
- GCTRL0: MRST~
- GCTRL1: PRST~
- GCTRL2: L1A
- GCTRL3: RESET
- GCTRL4: CMS Clock
- FSTAT0: F1 Empty~
- FSTAT1: F2 Empty~
- FSTAT2: F1 PAE~
- FSTAT3: F2 PAE~
- FSTAT4: F1 FULL~
- FSTAT5: F2 FULL~
- FSTAT6: FPGA Status
- FSTAT7: FPGA Status
- FSTAT8: FPGA Status
- FSTAT9: FPGA Status
- FSTAT10: FPGA Status
- FSTAT11: FPGA Status



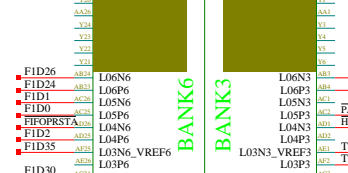
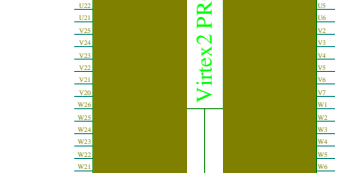
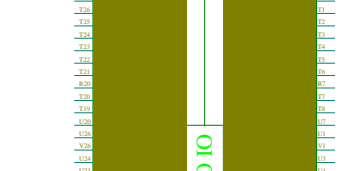
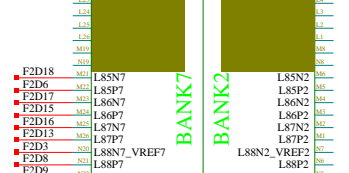
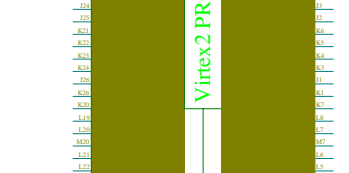
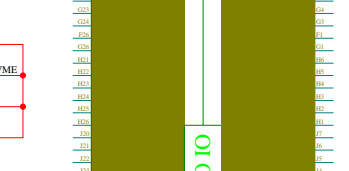
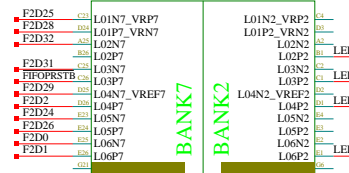
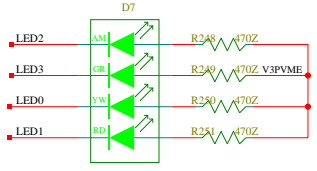
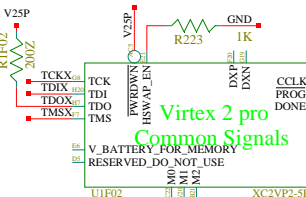
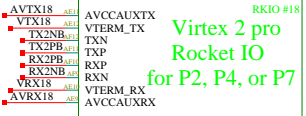
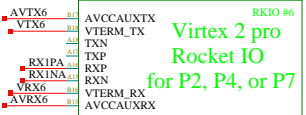
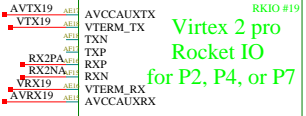
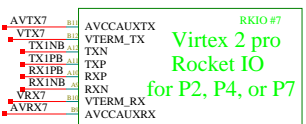
DEVICE ID = 010



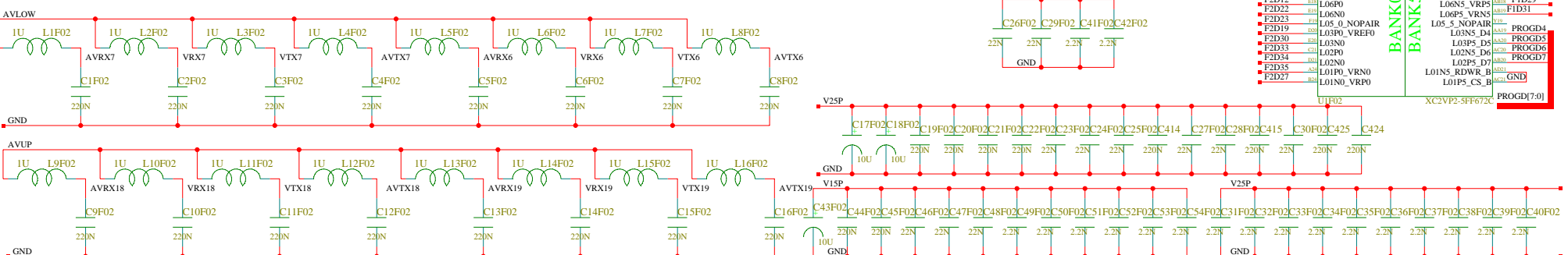
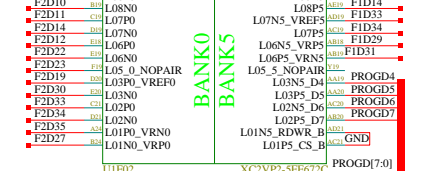
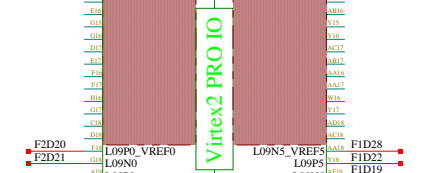
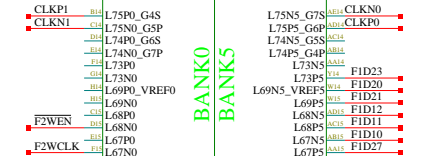
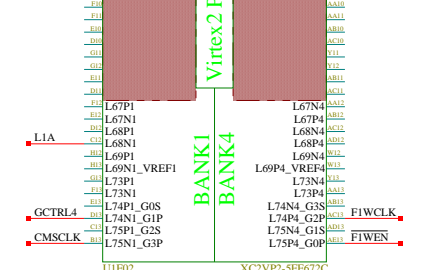
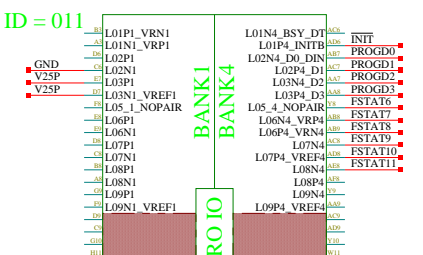
Fifo Setting  
36 bits IN, 36 bits OUT



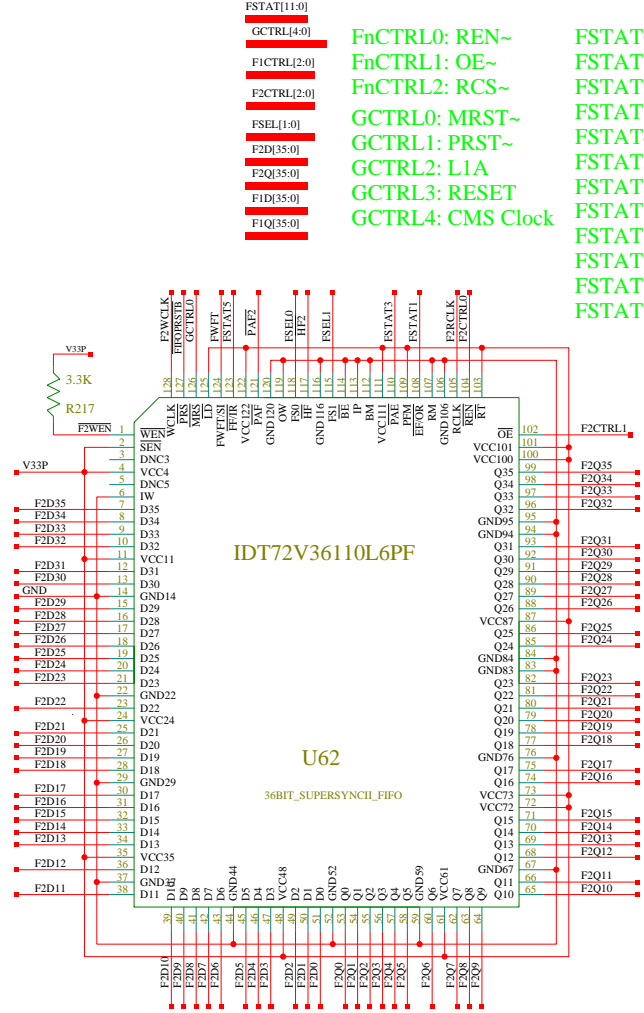
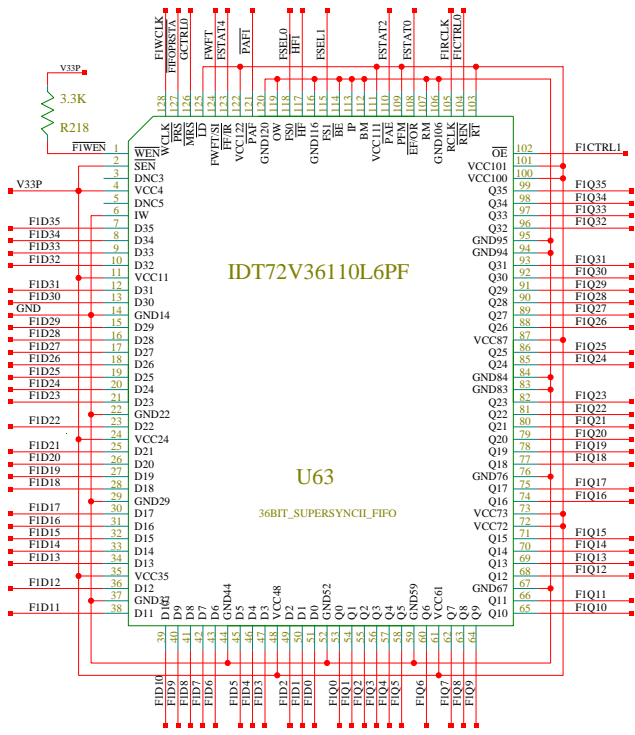
- FSTAT[11:0]
  - GCTRL[4:0]
  - FnCTRL[2:0]
  - F2CTRL[2:0]
  - FSEL[1:0]
  - F2D[35:0]
  - F2Q[35:0]
  - F1D[35:0]
  - F1Q[35:0]
- FnCTRL0:** REN~  
**FnCTRL1:** OE~  
**FnCTRL2:** RCS~  
**GCTRL0:** PRST~  
**GCTRL1:** MRST~  
**GCTRL2:** L1A  
**GCTRL3:** RESET  
**GCTRL4:** CMS Clock
- FSTAT0:** F1 Empty~  
**FSTAT1:** F2 Empty~  
**FSTAT2:** F1 PAE~  
**FSTAT3:** F2 PAE~  
**FSTAT4:** F1 FULL~  
**FSTAT5:** F2 FULL~  
**FSTAT6:** FPGA Status  
**FSTAT7:** FPGA Status  
**FSTAT8:** FPGA Status  
**FSTAT9:** FPGA Status  
**FSTAT10:** FPGA Status  
**FSTAT11:** FPGA Status



DEVICE ID = 011

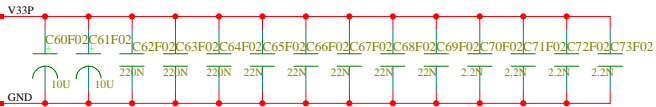


Fifo Setting  
36 bits IN, 36 bits OUT



- FSTAT[11:0]
- GCTRL[4:0]
- F1CTRL[2:0]
- F2CTRL[2:0]
- FSEL[1:0]
- F2D[35:0]
- F2Q[35:0]
- F1D[35:0]
- F1Q[35:0]

- FnCTRL0: REN~
- FnCTRL1: OE~
- FnCTRL2: RCS~
- GCTRL0: MRST~
- GCTRL1: PRST~
- GCTRL2: L1A
- GCTRL3: RESET
- GCTRL4: CMS Clock
- FSTAT0: F1 Empty~
- FSTAT1: F2 Empty~
- FSTAT2: F1 PAE~
- FSTAT3: F2 PAE~
- FSTAT4: F1 FULL~
- FSTAT5: F2 FULL~
- FSTAT6: FPGA Status
- FSTAT7: FPGA Status
- FSTAT8: FPGA Status
- FSTAT9: FPGA Status
- FSTAT10: FPGA Status
- FSTAT11: FPGA Status

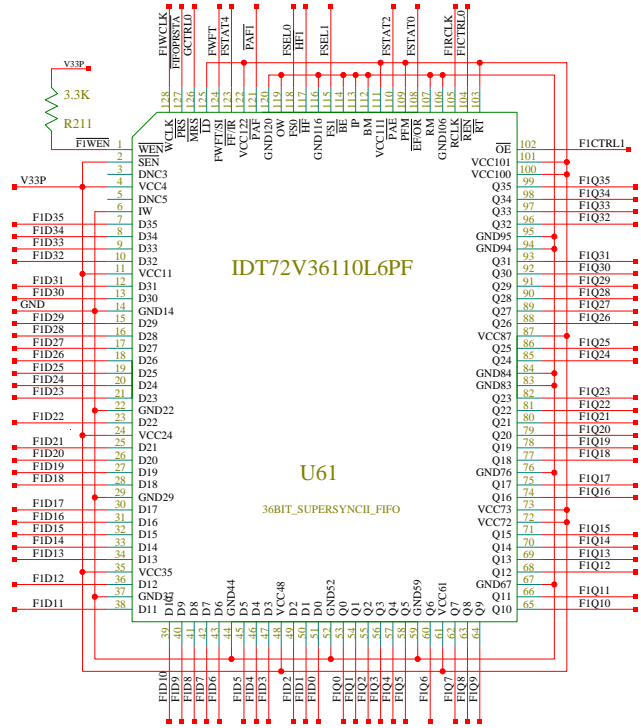








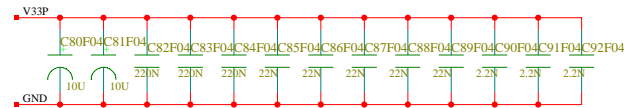
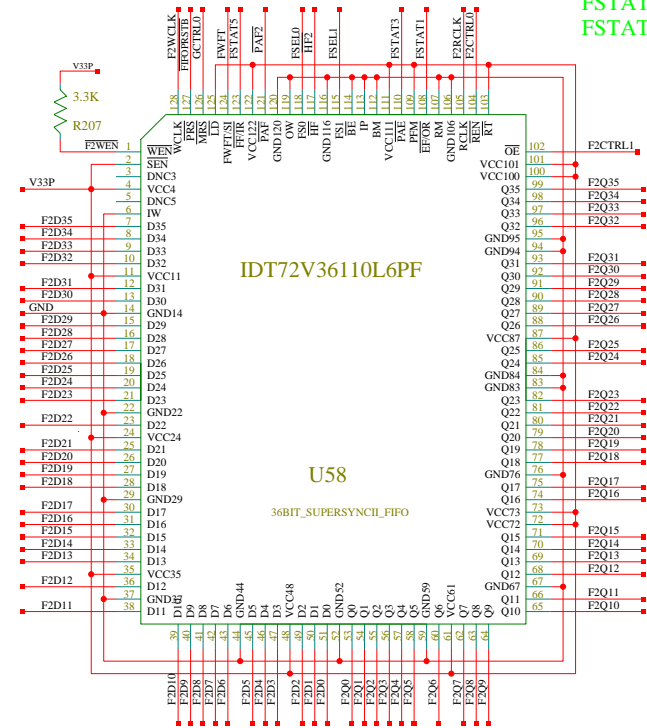
Fifo Setting  
36 bits IN, 36 bits OUT

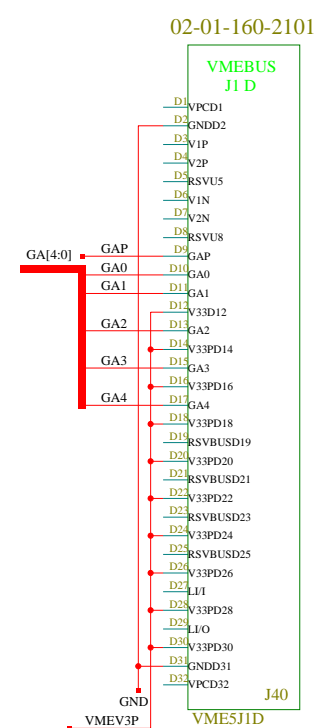
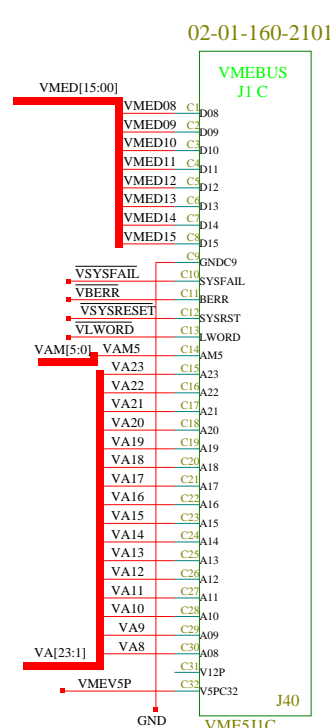
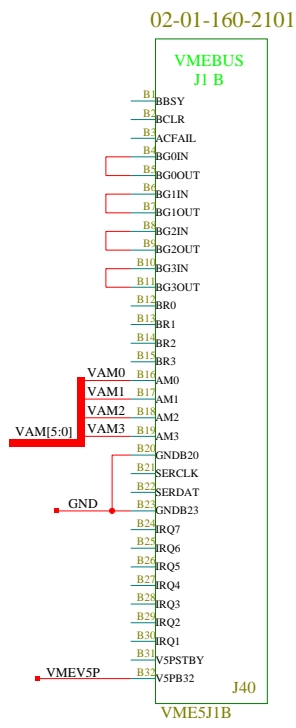
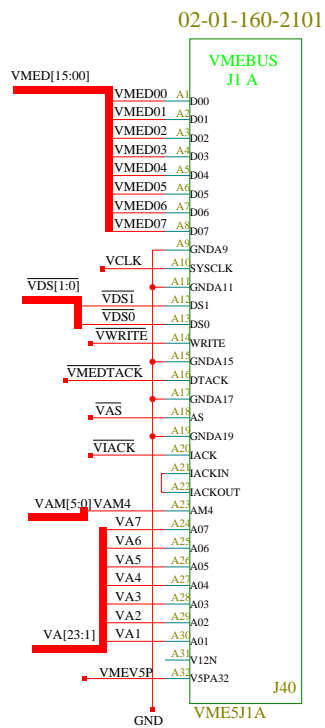
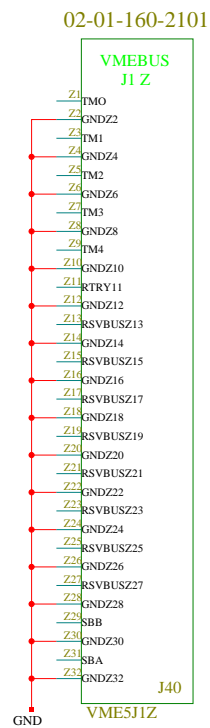


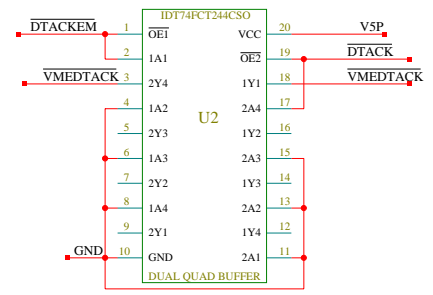
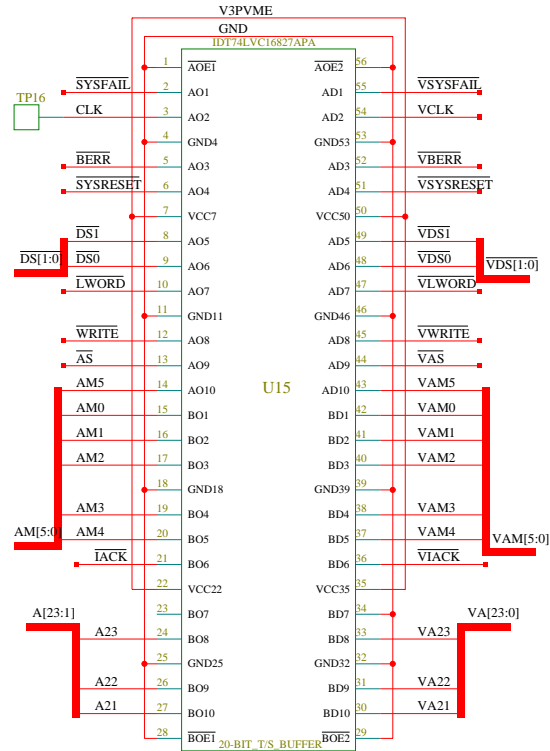
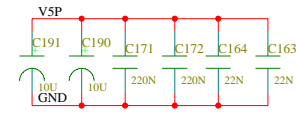
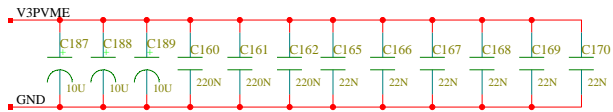
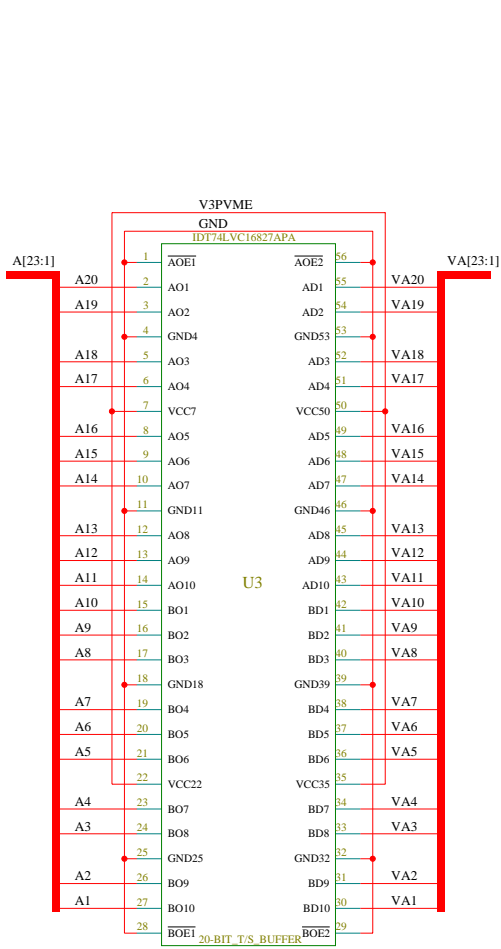
- FSTAT11:0
- GCTRL4:0
- F1CTRL1:2:0
- F2CTRL1:2:0
- FSEL1:1:0
- F2D1:35:0
- F2Q1:35:0
- F1D1:35:0
- F1Q1:35:0

- FnCTRL0: REN~
- FnCTRL1: OE~
- FnCTRL2: RCS~
- GCTRL0: MRST~
- GCTRL1: PRST~
- GCTRL2: L1A
- GCTRL3: RESET
- GCTRL4: CMS Clock

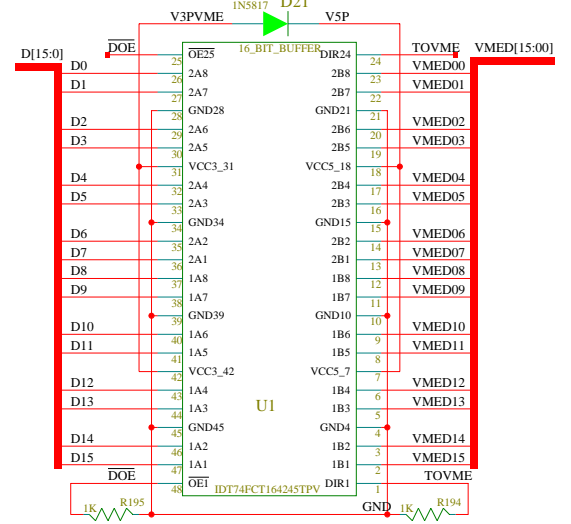
- FSTAT0: F1 Empty~
- FSTAT1: F2 Empty~
- FSTAT2: F1 PAE~
- FSTAT3: F2 PAE~
- FSTAT4: F1 FULL~
- FSTAT5: F2 FULL~
- FSTAT6: FPGA Status
- FSTAT7: FPGA Status
- FSTAT9: FPGA Status
- FSTAT10: FPGA Status
- FSTAT11: FPGA Status



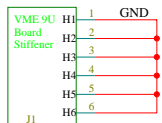
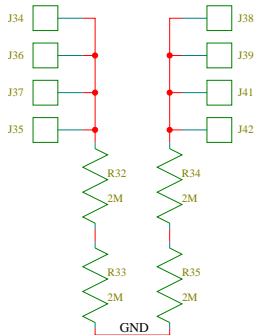
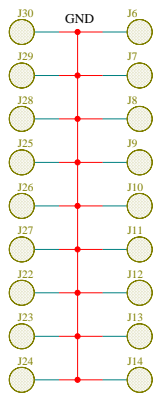




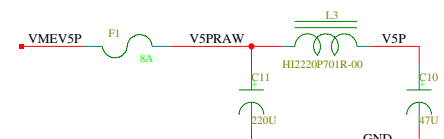
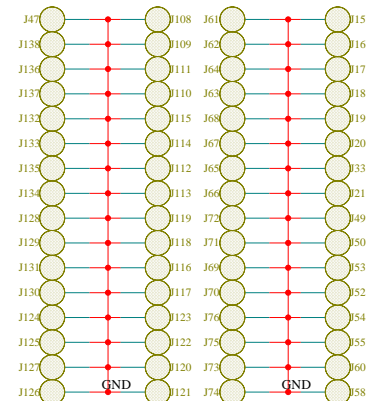
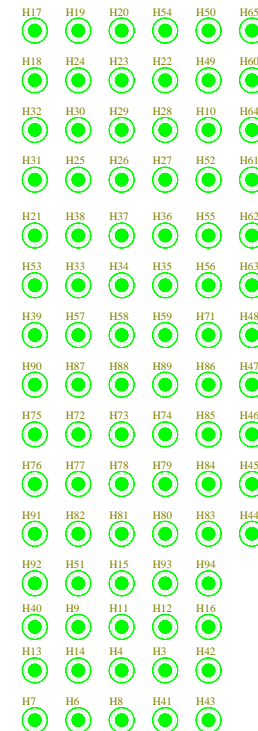
The Diode here to maintain (Vcc5 > Vcc3-0.5V) requirement  
DIR high: BusA->BusB, so TOVME should be positive logic



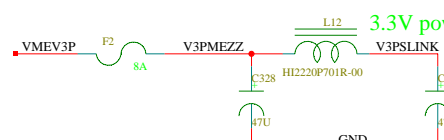
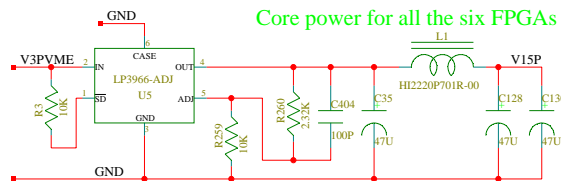
GROUND POINTS DISCHARGE UNIT BOARD STIFFENER FRONT PANEL MOUNTS



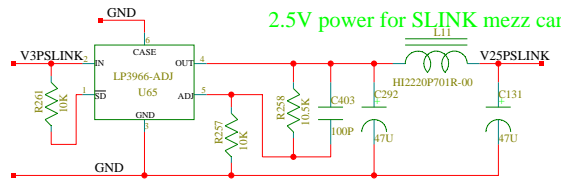
PART FIDUCIALS



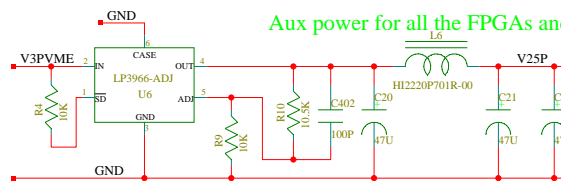
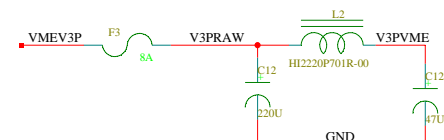
Core power for all the six FPGAs



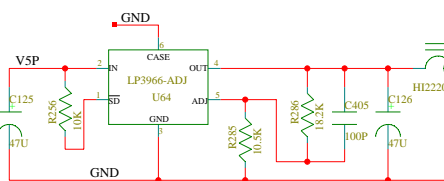
3.3V power for SLINK mezz cards



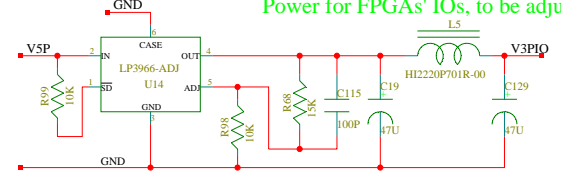
2.5V power for SLINK mezz cards



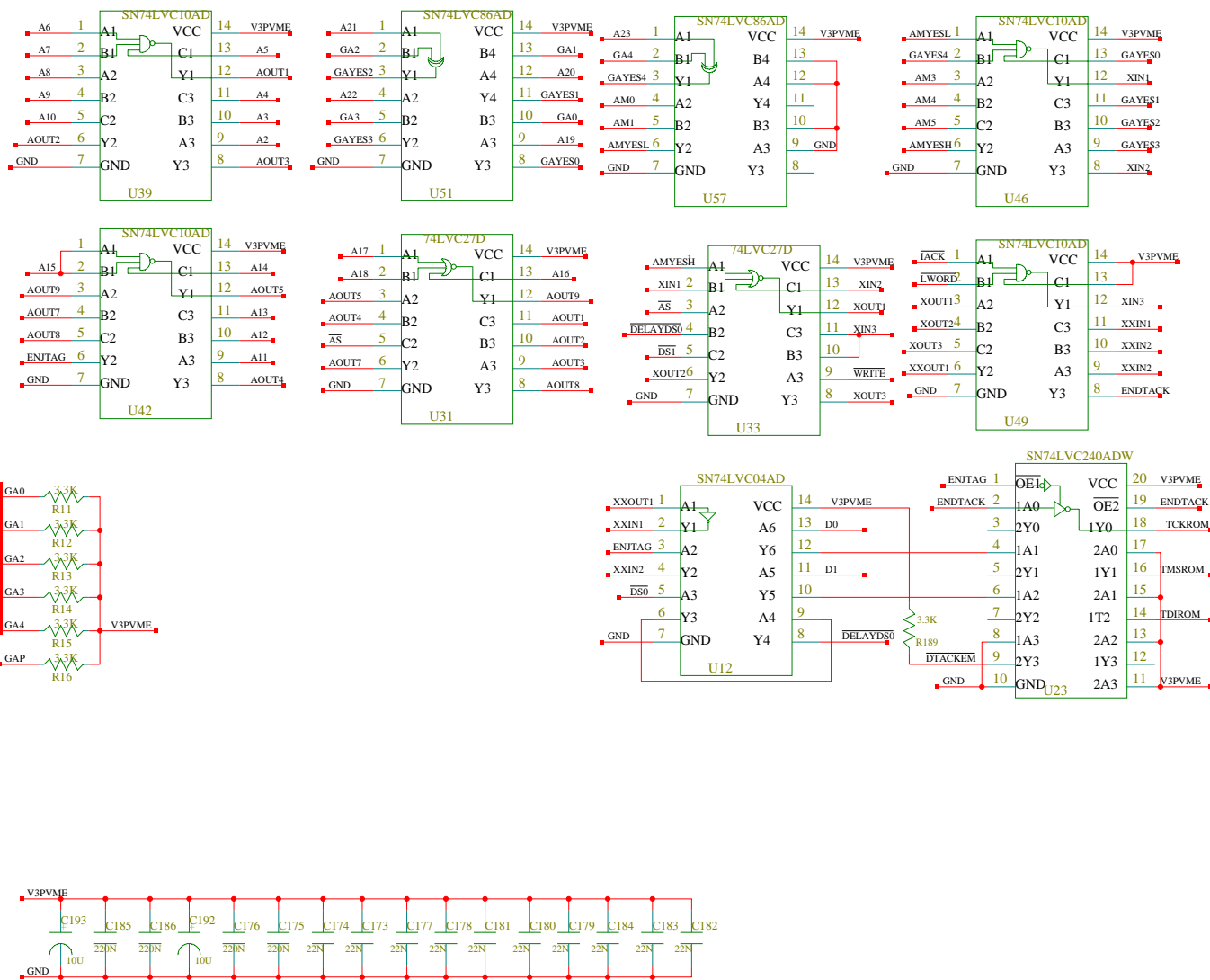
Aux power for all the FPGAs and Slink FIFOs



Power for FPGAs' IOs, to be adjusted at 3.0V

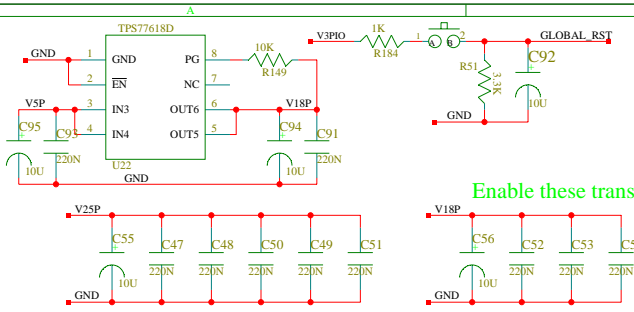


Discrete logic to load the VPROM in emergency

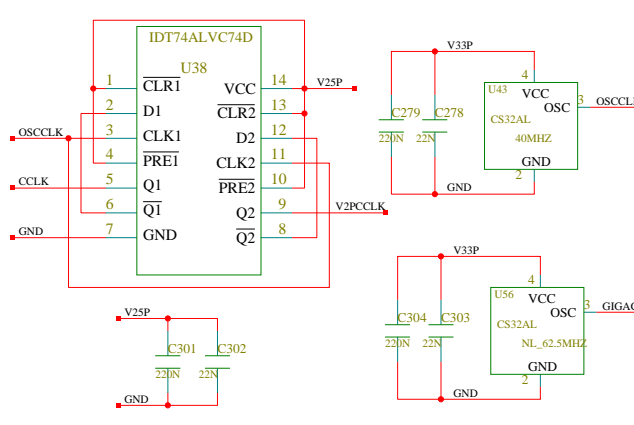
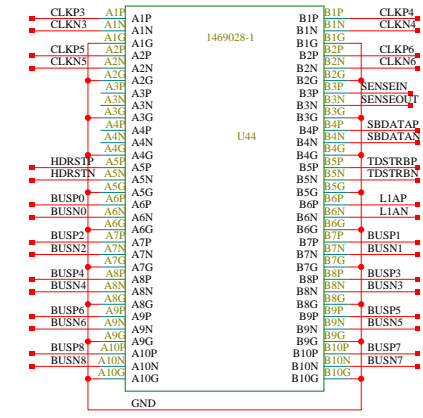
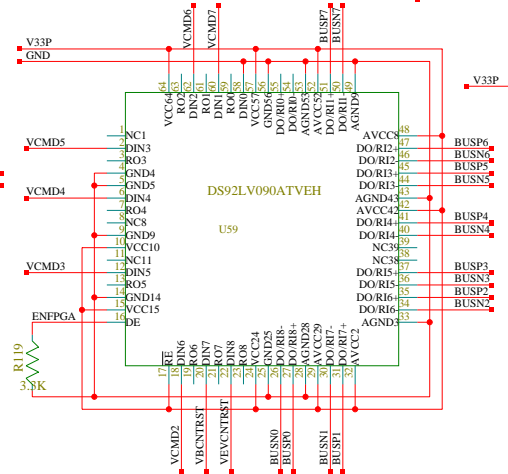
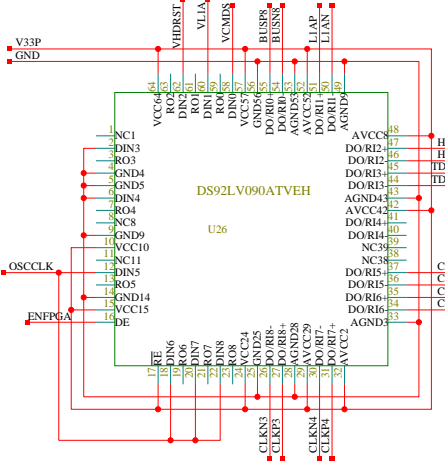
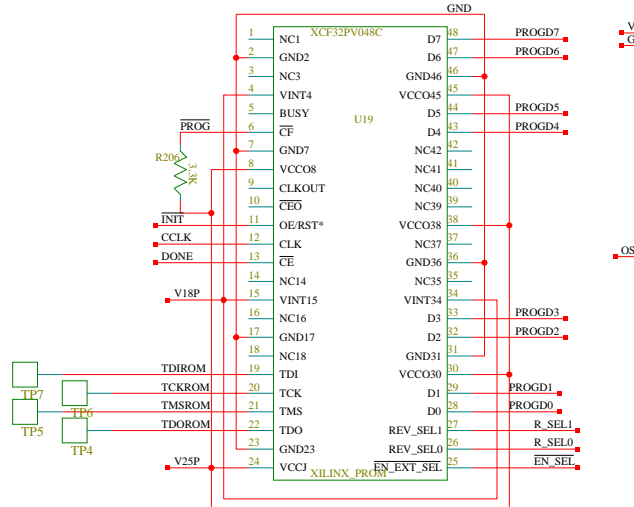
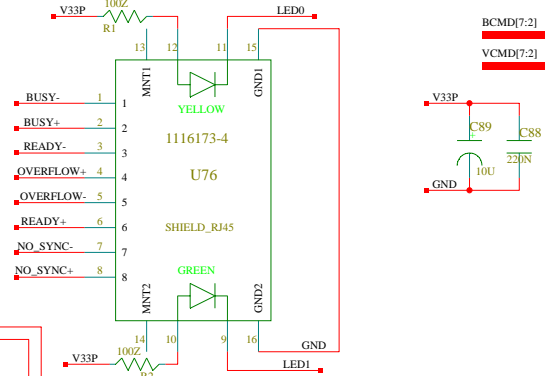
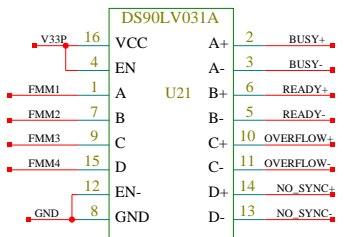




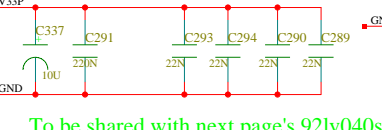




Enable these transceivers when there is no TTC available



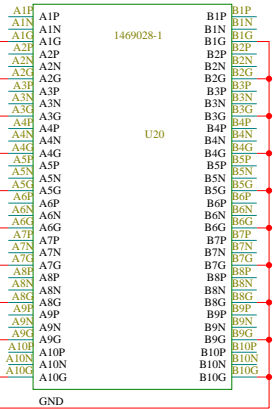
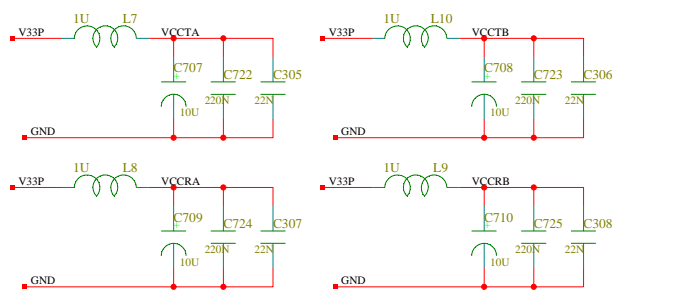
To be shared with next page's 921v040s



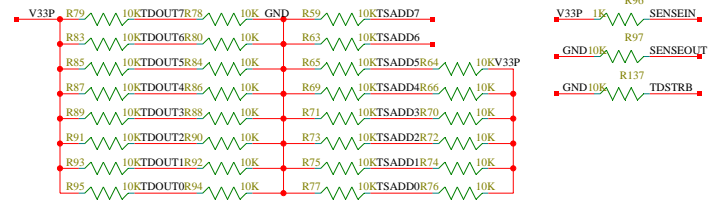
To be shared with next page's 921v040s



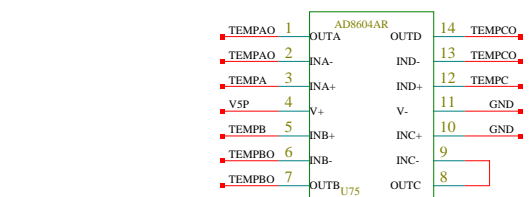
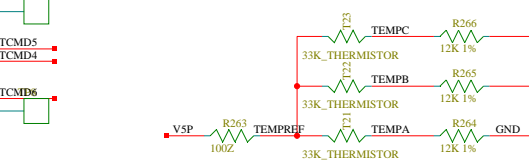
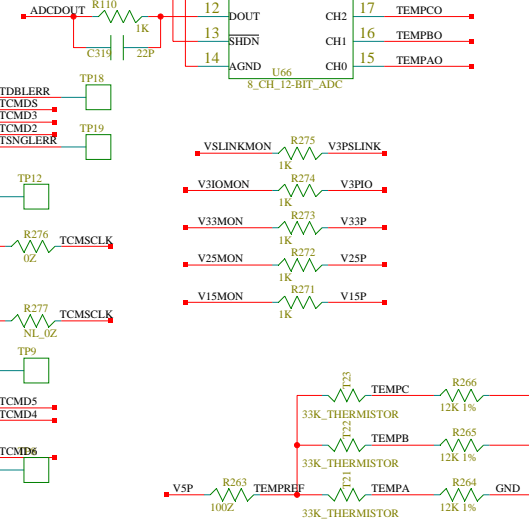
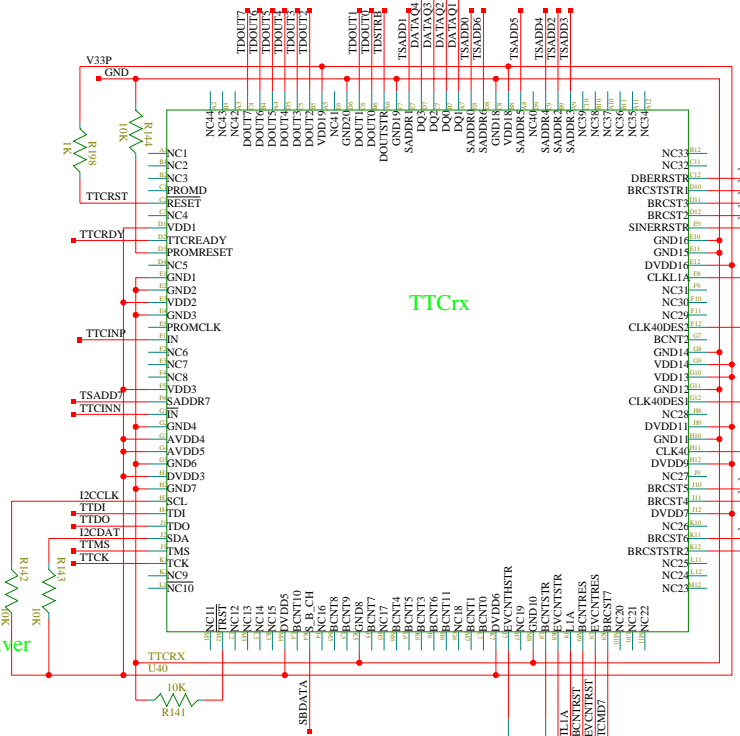
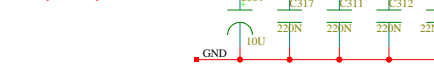
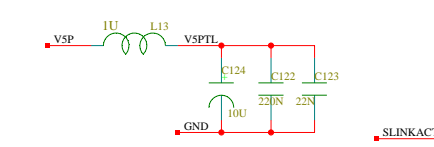
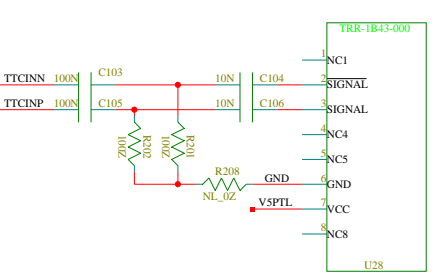
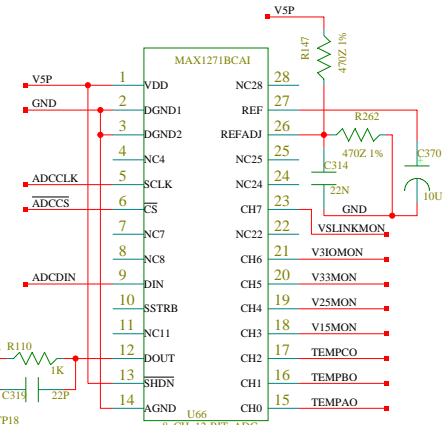
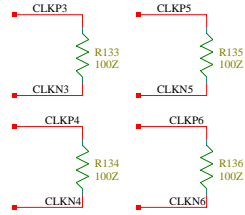
To be shared with next page's 921v090



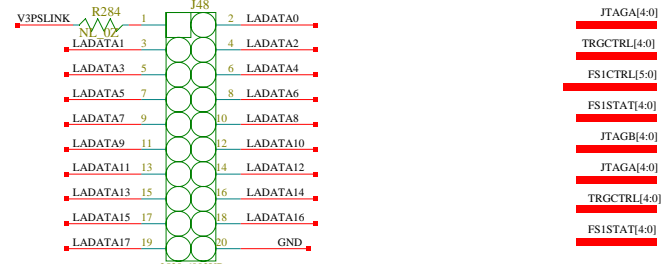
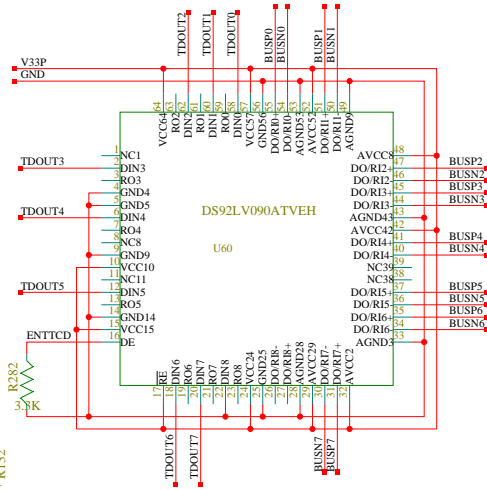
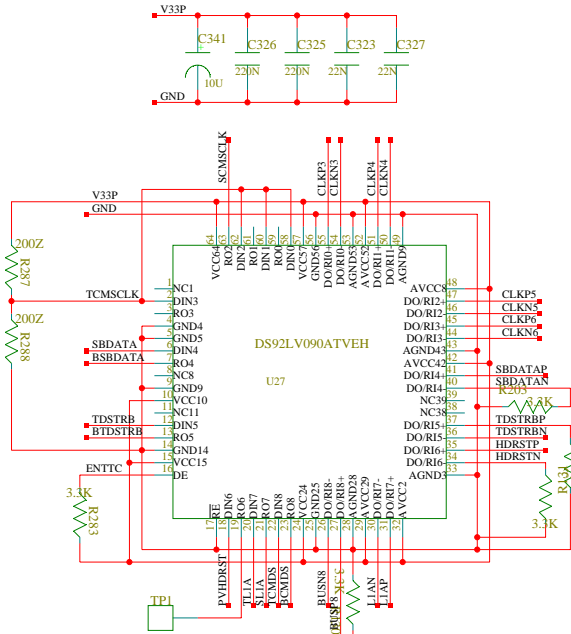
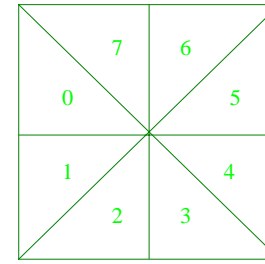
Use three pads for a pair of resistors, This is used to set the TTCrx ID



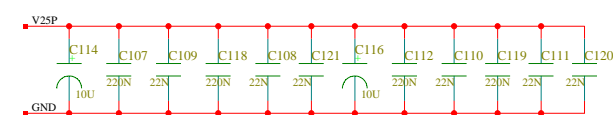
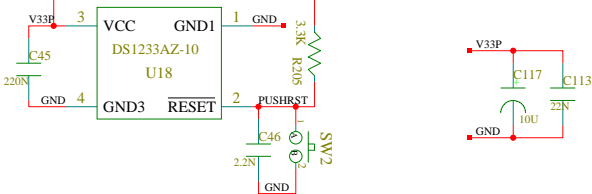
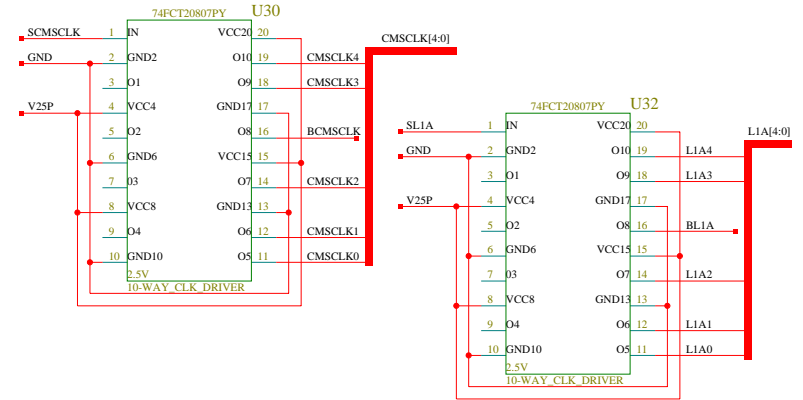
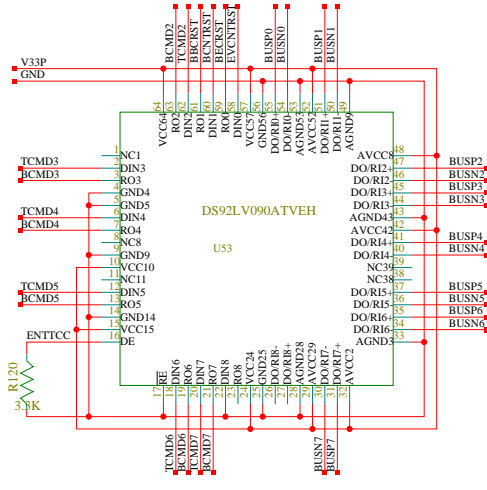
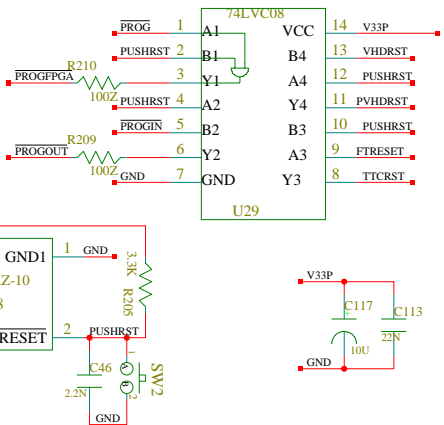
Tsadd7: Test mode when 1  
Tsadd6: Disable Serial/Parallel Converter when 1

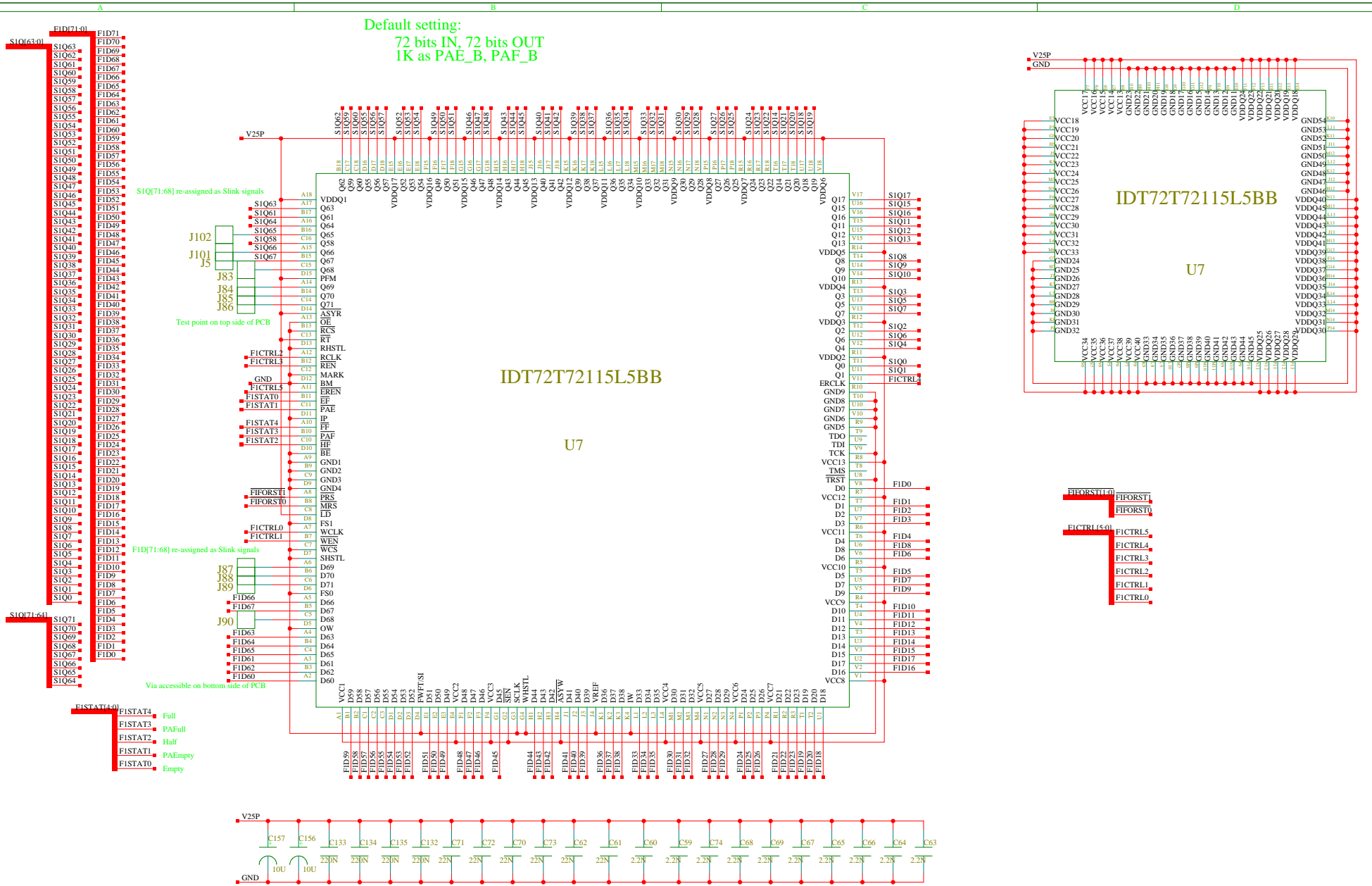


If BAP and BAN is connected on the backplane, the SENSEOUT will be high, or else it will be low  
 The bus signals are terminated on both ends of the backplane with 100 Ohm  
 The clock signals are terminated on this board and the backplane, except the passive DCC slot  
 clock3: slot 3,4,5,6,7; clock5: 8,9,10,11,12,13; clock6: 14,15,16,17; clock4: 18,19,20  
 (slot 8 is the active DCC, slot 17 is the passive DCC)



- JTAGB[4:0]
- JTAGA[4:0]
- TRGCTRL[4:0]
- FS1CTRL[5:0]
- FS1STAT[4:0]
- JTAGB[4:0]
- JTAGA[4:0]
- TRGCTRL[4:0]
- FS1STAT[4:0]

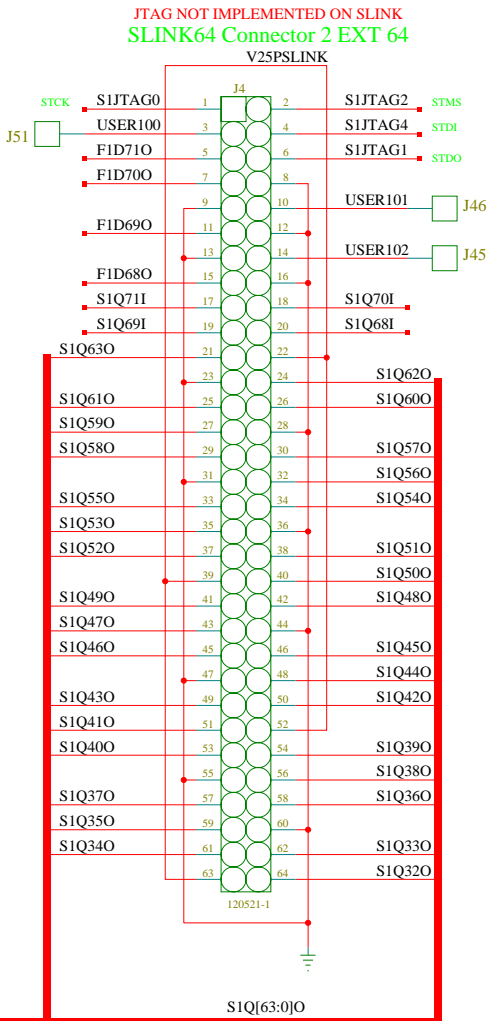
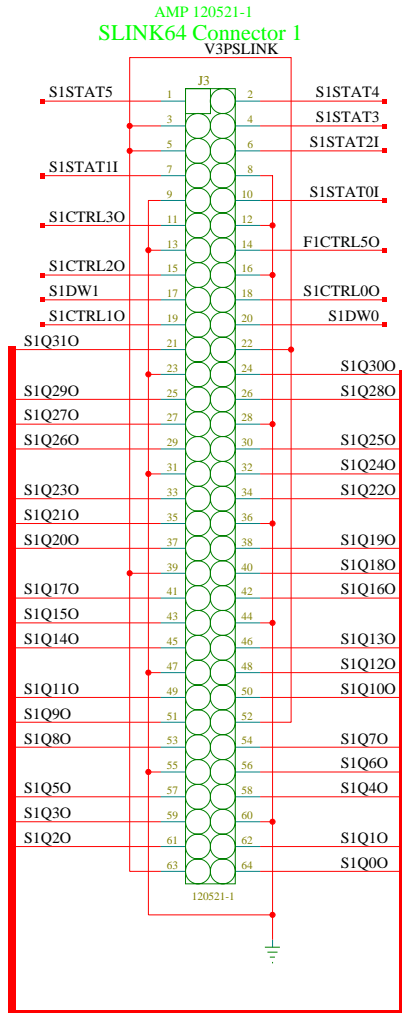




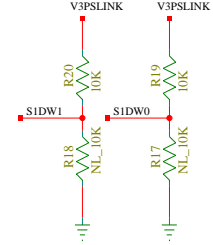


# Implement basic S-LINK architecture on DDU board?

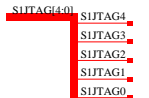
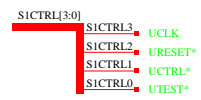
Replace these control with S1STAT[4:0] and S1CTRL[4:0]

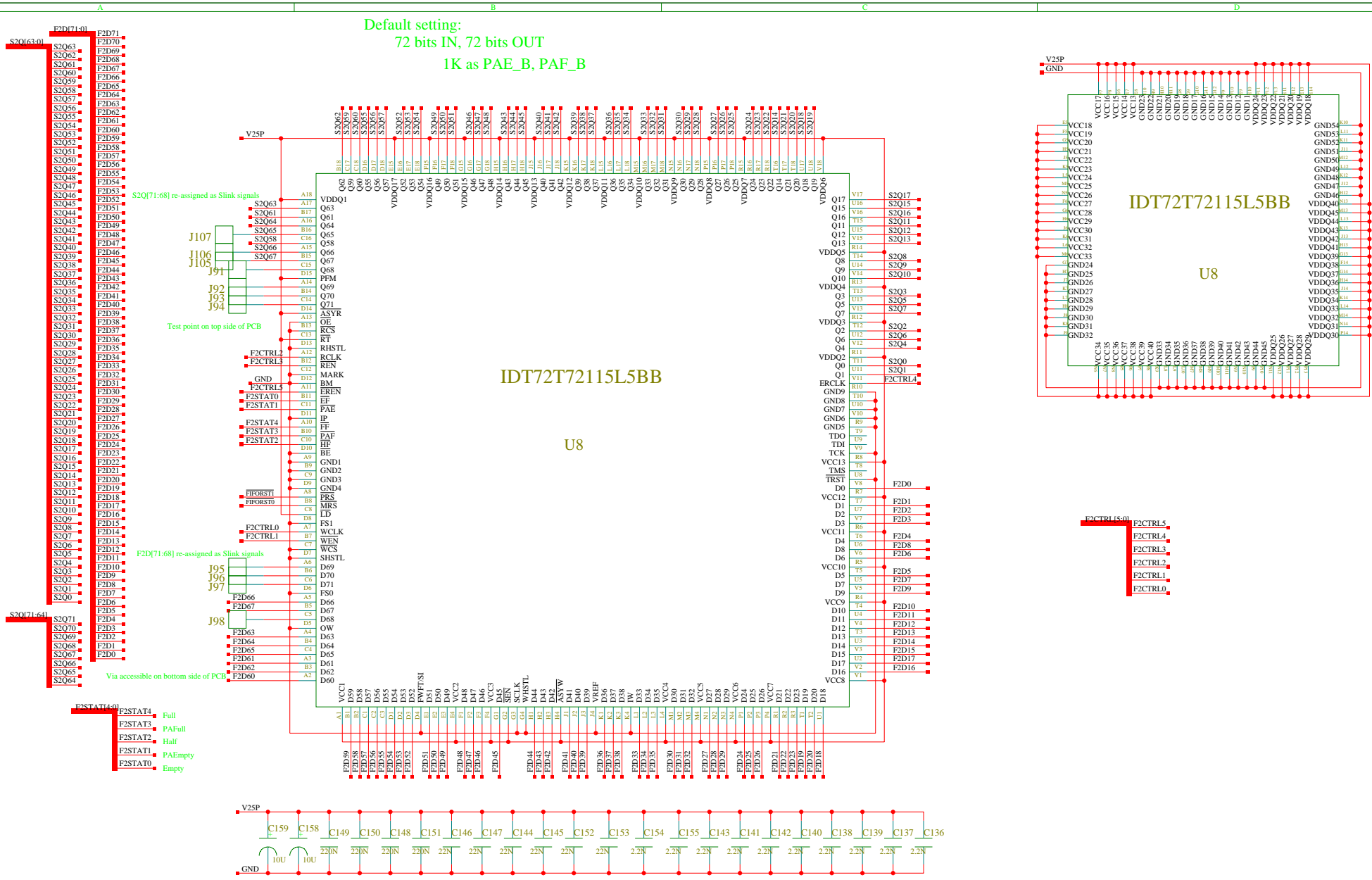


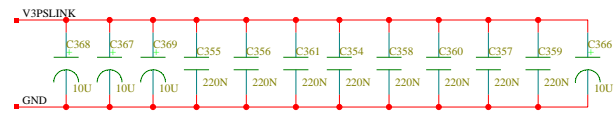
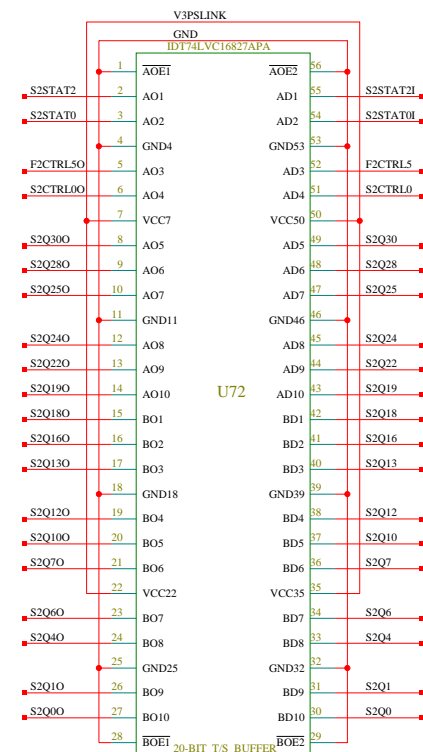
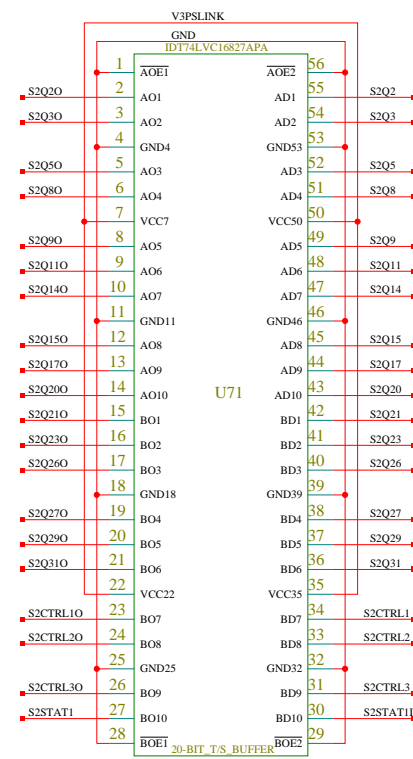
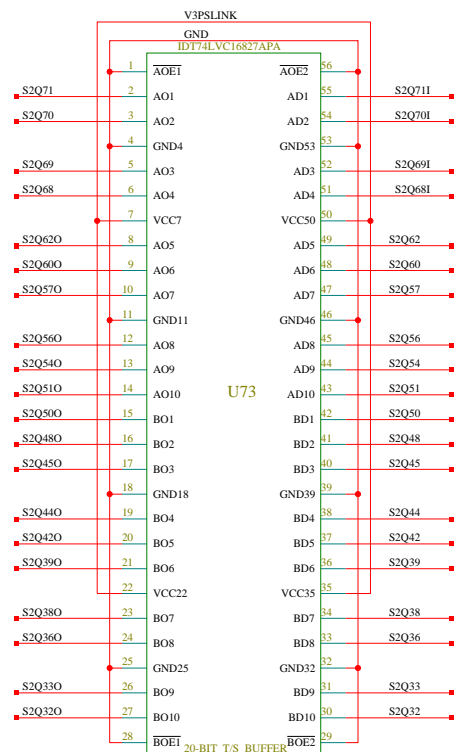
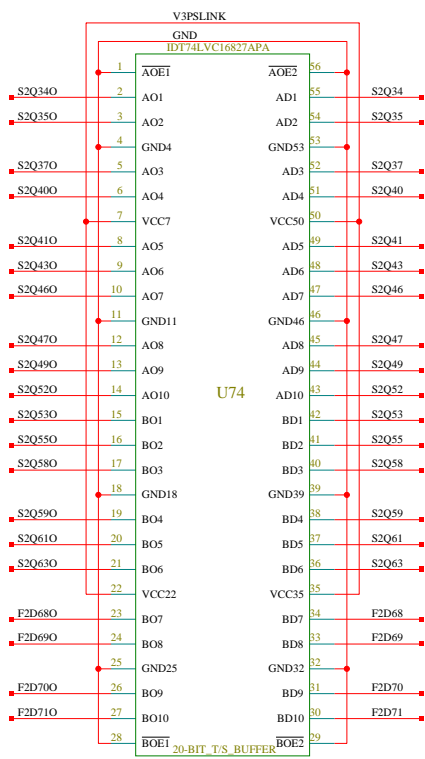
Not Used on Current LSC  
S1QW[0:1] = 11 FOR 64 BIT TRANSFERS



SLINK64/LSC Standoff Holes  
Isolated per SLINK Spec pg. 43/62

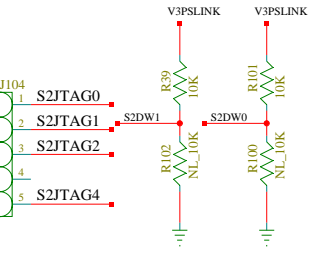
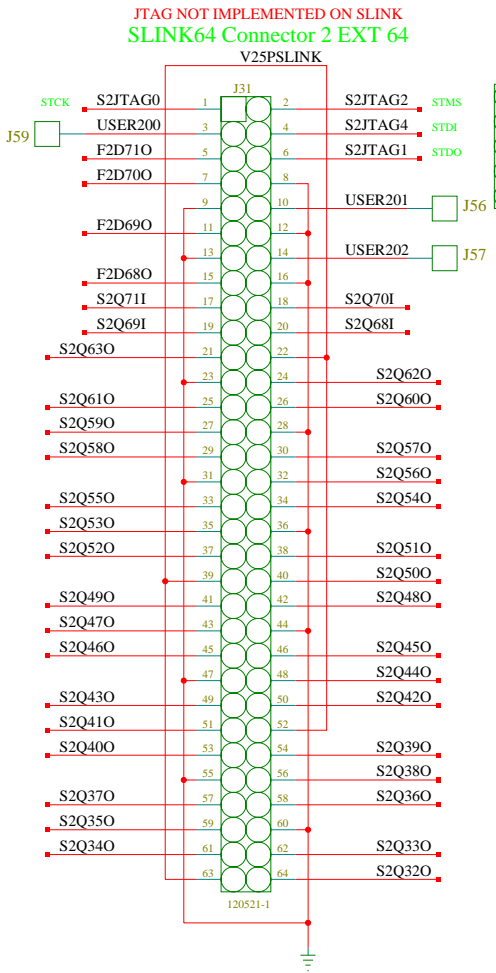
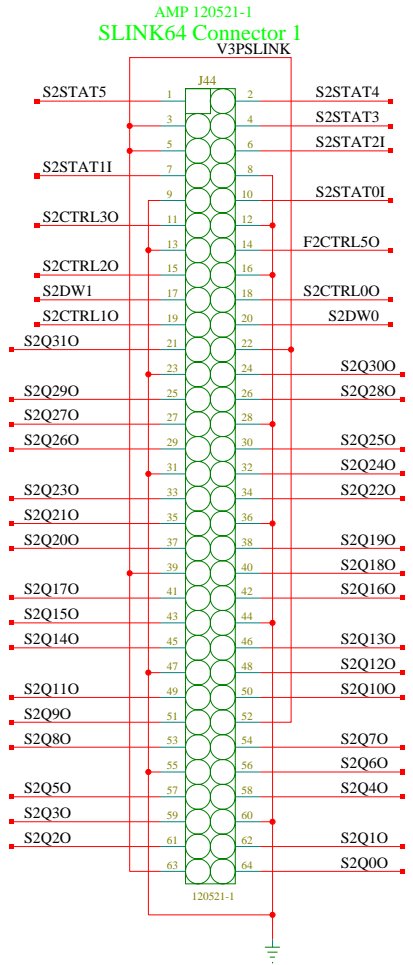






# Implement basic S-LINK architecture on DDU board?

Replace these control with S2STAT[4:0] and S2CTRL[4:0]



SLINK64/LSC Standoff Holes  
Isolated per SLINK Spec pg. 43/62

