Cathode FE Board

The Ohio State University
University of California Davis
University of California Los Angeles
CERN
Cathode FE Board

96 Channels

<table>
<thead>
<tr>
<th>ASIC(chip) Type</th>
<th>chip's / CFEB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamp-Shaper (16 ch)</td>
<td>6</td>
</tr>
<tr>
<td>SCA (16 ch)</td>
<td>6</td>
</tr>
<tr>
<td>Comparator (16 ch)</td>
<td>6</td>
</tr>
<tr>
<td>ADC (12 bits, 20 MHz)</td>
<td>6</td>
</tr>
<tr>
<td>Readout Control FPGA</td>
<td>1</td>
</tr>
</tbody>
</table>

BUCKEYE (ASIC) - amplifies and shapes input pulse

SCA (ASIC) - analog storage for 20 MHz sampled input pulse

ADC - events with LVL1ACC digitized and sent to DAQ Motherboard (25 nsec/word)

Comparator ASIC - generates trigger hit primitives from shaped pulse

Controller FPGA - controls SCA storage and digitization
# Cathode FE Board

## Input/Output Signals

### Inputs

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>96 channels input from chamber strips</td>
<td></td>
</tr>
<tr>
<td>LCT</td>
<td>from DMB, if CLCT is available, CLCT---&gt;DMB---&gt;CFEB, if CLCT is not available, FTC---&gt;DMB---&gt;CFEB, if Calibration mode, DMB---&gt;CFEB</td>
</tr>
<tr>
<td>L1ACC</td>
<td>From DAQMB, - if CCB is available, CCB---&gt;DMB---&gt;CFEB, or CCB---&gt;FTC---&gt;DMB---&gt;CFEB - if CCB is not available, FTC (LCT delay)---&gt;DMB---&gt;CFEB, or, DMB (LCT delay)---&gt;CFEB, - if Calibration mode, DMB---&gt;CFEB;</td>
</tr>
<tr>
<td>DAC</td>
<td>0-5V adjustable for external, internal charge injection for BUCKEYE from DAC on DMB</td>
</tr>
<tr>
<td>BUCKEYE</td>
<td>+10V and -5V voltage references from DMB</td>
</tr>
</tbody>
</table>

### Outputs

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAQ data</td>
<td>Strip charge ADC data, Through 21-bit channel link to DMB</td>
</tr>
<tr>
<td>Trigger data</td>
<td>Comparator Triads through two 28-bit multiplexers to CLCT; End channel signals to neighboring boards, analog preamp signals and digital comparator signals</td>
</tr>
<tr>
<td>Monitor</td>
<td>Temperature sensor output, to DMB, program done</td>
</tr>
</tbody>
</table>

### Controls

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global-reset</td>
<td>from DMB, reset DMB and CFEBs, and synchronize the 50ns clock on DMB and CFEBs</td>
</tr>
<tr>
<td>Clock</td>
<td>40MHz, from DMB</td>
</tr>
<tr>
<td>FPGA-program</td>
<td>from DMB, re-program the FPGA from PROM on CFEB</td>
</tr>
<tr>
<td>JTAG port</td>
<td>from DMB, controls: BUCKEYE data shift, FPGA resets, ISP-PROM download, CFEB status monitor, etc.</td>
</tr>
</tbody>
</table>

### Downloaded Constants

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PREBLOCKEND</td>
<td>(4 bits) Block Phase Shift</td>
</tr>
<tr>
<td>PROM programming data</td>
<td>(about 500K bits); BUCKEYE working mode (normal, internal capacitor select, external, kill, 3bits/channel); Comparator timing (3 bits), working mode (2 bits) and threshold</td>
</tr>
</tbody>
</table>

### Power

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+6V</td>
<td>for BUCKEYE clean power (550-600mA)</td>
</tr>
<tr>
<td>+5V</td>
<td>for SCA, ADC, comparator, etc. (900-1000mA)</td>
</tr>
<tr>
<td>+3.3V</td>
<td>for FPGA, Channel link, CPLD, etc. (450-500mA)</td>
</tr>
<tr>
<td>+5V and +3.3V power supplies are subject to change.</td>
<td></td>
</tr>
</tbody>
</table>
BUCKEYE ASIC

Physics Demands

\[ \sigma \sim 150\mu m \text{ ME1/2} \]
\[ \sigma \sim 300\mu m \text{ MEX/X} \]

\[ \Rightarrow \quad \frac{dQ}{Q} < 3\% \]

Rate is demanding 100 KHz/strip 300 KHz track/chamber

0.8 \mu m AMI CMOS with Linear Capacitor

- 5 pole semigaussian
- 1 pole 1 zero tail cancellation
- 100 nsec peaking time (delta function)
- 170 nsec peaking time (real pulse)
- Gain 0.9 mV/fC
- Equivalent Noise 1 mV
- Nonlinearity < 1 % at 17 MIPS
- Rate 3 MIPs at 3 MHz with no saturation
- Two track resolution 125 nsec
BUCKEYE (cont.)

Noise Spectrum of BUCKEYE chip

\[ \sigma(\text{noise}) \sim C \times 20e/pF + 4770e \]

Output Pulses of BUCKEYE Chip

Chamber Pulses with BUCKEYE Chip

L.S. Durkin, ESR 9/00
BUCKEYE / SCA

Switched Capacitor Array (SCA)

SCA Specifications

- 96 capacitor for each of 16 channels
- LVDS addressing read/write
- Simultaneous read/write
- Gray Code address sequencing
- Input impedance < 300Ω
- Non-Linearity (0-2V) 0.25%
- Pedestal Cell-Cell variation 0.25 mV
- Maximum Sampling rate 20 MHz
- Channel-channel access 100 nsec

BUCKEYE meets all Requirements!
Controller FPGA (XILINX Virtex)

- does SCA bookkeeping
  - given LCT set aside
    2 blocks of 8 capacitors
  - generates greycode addressing
- controls digitization
  - given LVL1ACC starts digitization
  - multiplexes ADC output to motherboard
  - digitization take 25 µsec
  - 12 bit ADC

<1 error for 125 Hrs Running
Comparator ASIC

- 16 channel, 40 MHz output
- Input amplified and shaped BUCKEYE output
- Generate trigger primitive 1/2 strip hits
- Programmable threshold
- Programmable timing, working mode

![Comparator Network Diagram]

Goal: 92% half-strip ID efficiency

![Graph: Efficiency vs. Threshold]

0.7µm Alcatel
J.C. Santiard CERN

Efficiency
Correct 1/2 strip  90.4 %
Nearest N. or Correct  98.3 %

![Graph: Layer 6 Track Position vs. Half-Strip Efficiency]
Comparator ASIC ...

ASIC Performs to Specifications

Removing the Channel Link (3 crossing delay) ...

Status
- one crossing required to sync signals
- prototype has been built and is being tested at Ohio State and UCLA
- multiplexer will be rad tested
BUCKEYE has internal shift register which controls calibration

**JTAG Shift Register Modes**
- Normal
- Precision Ext. Cap (<1%)
- Int. Cap Small (1x)
- Int. Cap Medium (2x)
- Kill

**Precision DAQ and Delay on Motherboard Control Pulsing**

- CCB board generates pseudo pulse, LCT, and LVL1ACC

- Precision Ext Cap. Allows gain, linearity, crosstalk, timing measurement. Oscilloscope-like output for each channel.

- Any channel can be selectively killed

- Trigger logic and thresholds can be checked using small and medium cap
Calibration ...

Calibration from FNAL Chamber Electronics

- 12 bit ADC
- 0.5 mV/count  0.54 fC/count
- Landau Peak ~ 400 counts
- RMS noise for 9216 capacitors

Total Noise $\sigma \sim 1.25$ mV!

- linearity for 480 channels

System linearity $< 1\%$ at 17 MIPs!
Gain Constant

- gain varies ~1% within chip
- gain varies ~2% chip to chip

Pulser + $^{137}$Cs (20 kHz/strip)

BUCKEYE can take LHC Rate!
Timing and Synchronization

Cathode FE Board allow ±1 Beam Crossing uncertainty on LCT relative to LVL1ACC

Timing is a Trigger Issue

- FE Board 40 MHz clock has programmable delay on Motherboard
- Comparator 40 MHz clock has programmable delay on CLCT Board
- LCT and LVL1ACC synchronized to 40 MHz Clock

Interface with Fast and Slow Control

Fast Control Signals (CCB) to FE Board

- reprogram logic (see rad discussion)
- reset logic
- pulse, pseudo-LCT, pseudo-LVL1ACC (calibration)

Slow Control Signals to FE Board

- JTAG signals, TDO, TDI, TCLK, TMS
Slow Control System

- one PC (running SCADA CMS slow control software) serves 24 crates
- ethernet 10 Base-T → embedded VME computer
- VME Bus within Crate
- DAQ Motherboard has VME interface -FPGA
- VME interface generates JTAG for FE Board

Cathode FE Board Slow Control

- Buckeye Shift Registers
- 1 Xilinx EPROM (program and readback)
- 1 Xilinx Virtex (readback)
- FPGA status checks (check on startup)
- comparator thresholds
- comparator mode/timing
- thermistor (temperature)
- access boards unique serial number
Monitoring

Each FE Board has a 4 bit Beam Crossing counter
- stored in data transferred to Motherboard

Each Digitized event has 8 checksum words (CRC15)
- stored in data transferred to Motherboard
- sensitive to channel link problems

LCT-LVL1ACC Coincidence Calculated both on
FE Board and Motherboard Separately
- motherboard knows when FE data not present
- lack of data reported to DAQ

FE Boards send fixed data length records to FIFO on
Motherboard
- motherboard knows when data is missing
- lack of data reported to DAQ
- CFEB-Motherboard transmission timeout (10 μsec)

Most failures will be detected before Periodic
Radiation reload and resets allowing CCB to
Reset the system!
Radiation Levels in Endcap Muon

Calculated by M. Huhtinen

Integrated over 10 LHC years
(5x10^7 s at 10^{34} cm^{-2}s^{-1})

Neutron Fluence (>100 keV): (0.02 - 6) x 10^{11} cm^{-2}
Total Ionizing Dose: (0.007 - 1.8) kRad
Worst-case Radiation Environment
(Use calculated levels times a safety factor of 3)

- Measure SEE (SEU and SEL) cross sections for neutron fluence of $2 \times 10^{12} \text{cm}^{-2}$
- Measure TID effects up to a dose of 5 kRad
- Measure degradation for an equivalent neutron fluence of $2 \times 10^{12} \text{cm}^{-2}$

<table>
<thead>
<tr>
<th>Radiation Source</th>
<th>SEU, SEL, TID</th>
<th>SEU, SEL, TID</th>
<th>Displacement</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 MeV Protons</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(UC Davis)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 MeV Neutrons</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Ohio State)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMOS Devices</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bipolar Devices</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Gain vs Dose**
- Expected dose in 10 LHC years
- New runs with same chip
- Curves for all 16 channels

**Noise vs Dose**

L.S. Durkin, ESR 9/00
### Radiation Test Summary

<table>
<thead>
<tr>
<th>Device (Function)</th>
<th>Proton Fluence ($10^{11}$ cm$^2$)</th>
<th>Dosage (kRad)</th>
<th>Number of SEU's</th>
<th>SEU Xection ($10^{-10}$ cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XILINX Spartan XCS30XL (Readout Controller)</td>
<td>1.0</td>
<td>13.4</td>
<td>27</td>
<td>2.7</td>
</tr>
<tr>
<td>XILINX Spartan XCS30XL (Multiplexer)</td>
<td>2.9</td>
<td>38.1</td>
<td>34</td>
<td>1.2</td>
</tr>
<tr>
<td>XILINX CPLD XC9536XL (Chip 1)</td>
<td>2.8</td>
<td>42.7</td>
<td>106</td>
<td>3.8</td>
</tr>
<tr>
<td>XILINX CPLD XC9536XL (Chip 2)</td>
<td>3.1</td>
<td>41.3</td>
<td>117</td>
<td></td>
</tr>
<tr>
<td>XILINX Virtex XCV50 (Readout Controller &amp; MUX)</td>
<td>0.9</td>
<td>12.5</td>
<td>16</td>
<td>1.7</td>
</tr>
<tr>
<td>Channel Link Receiver</td>
<td>14.8</td>
<td>200</td>
<td>277</td>
<td>1.9</td>
</tr>
<tr>
<td>Channel Link Transmitter</td>
<td>14.8</td>
<td>200</td>
<td>1023</td>
<td>6.9</td>
</tr>
</tbody>
</table>

- **Fluence** = 2.8 x $10^{12}$ / cm$^2$
- **Following devices passed the test**
  - LM1117-adj (adjustable voltage regulator)
  - LM4120-2.5 (voltage reference; 3.3 V, 5 mA)
  - LM4120-1.8 (voltage reference; 3.3 V, 5 mA)
  - LM4041 (shunt voltage reference)
  - SDA321 (Diode Array – reversed biased)
  - Red LED
  - AD8011 (300 MHz Current Feedback OpAmp)
- **Need a rad-tolerant 2.5 V regulator**
  - Good candidate identified. Presently testing.
Radiation Tests ...

Cumulative effects
- **Total ionization** dosage (with 63 MeV protons)
  - No deterioration of analog performance up to 10 krad for all three CMOS ASIC’s
  - All FPGA’s survive beyond dosage of 30 krad
- **Displacement** damage (with $2 \times 10^{12} \text{ cm}^{-2} \text{ n’s @ 1 MeV}$)
  - Usable voltage regulators and references identified
  - Protection diodes OK

Single-Event Effects
- No latch-up for all ASIC’s up to $2 \times 10^{12} \text{ p cm}^{-2}$
- Single Event Upset (SEU)
  - Cross sections measured for all FPGA’s, C-Links.
  - All SEU’s in FPGA’s recoverable by reloading

**SEU Rate on FE Board given by Controller FPGA**

Controller FPGA (XILINX Virtex)
- triple voting logic on crucial gates
- SEU cross section $1.7 \times 10^{-10} \text{ cm}^{-2}$ ($410,000 \text{ s/SEU}$)

**Must Reload Virtex Every ~17 minutes**
EPROM (XC1802) JTAG Reloadable

- $2.76 \times 10^{11} \text{p/cm}^2$ 37.0 kRad
- 3 SEU’s, No Memory Errors
- Must reload every 1.5 LHC years!

Reload every 17 minutes or when error is detected

Note: Almost all virtex errors will be detected as errors by DAQ system!
Tested calibration, noise, pedestal, linearity. Only difference was a time shift of 6 nsec.

**Passive Delays**
- Rhombus LVMDM 100 nsec contain iron
- have switched to

**Passive Delays**
- Data Delay Devices 3D7105 for short delays
- Virtex Delay-Lock loops for long delays
- no difference seen
Spark Protection

Scheme has protected Buckeye for Simulated 3000 Sparks

Two Options Under Study

1. Inductor is Chamber- FE Board cable (100 nH/ft)

2. Put 96 Air-core (~68 nH) Inductors on FE Board
We have procured a large oven at OSU

What do other people do?

CDF: 50-60 C for 8-24 Hrs

US Military: 125 C for 320 Hrs

• CDF sufficient for things like backward tantalums no sensitivity to semiconductor failure

• Replacing boards in CMS forward muon chambers will be difficult

We will start conservatively and measure failure rate vs time. Hopefully full US military burn-in will not be needed!
Production

PC boards will be etched and stuffed commercially

ASIC Testing

BUCKEYE Preamp/Shaper

- ~ 15000 ASIC chips will be produced by AMI
- Bonded in Indonesia by AIT LTD
- Tested at Ohio State

Measure gain, noise, linearity, peaking time, delay time, … for each channel

AMI Preproduction

1000 chips
Yield ~50%

(problem found in one of two AMI assembly lines. They are fixing and will make new samples. Yield increase to >80%)
Production …

SCA ASIC

- AMI will manufacture wafers
- AMI will measure chips guaranteeing quality
- AMI will bond chips

Comparator ASIC

- Alcatel will manufacture wafers
- an outside company will measure chips
- Chips will be bonded in Hong Kong

Alcatel Preproduction

- yield 66 % (working on it)
- chips are excellent
Stuffed Boards will be tested and debugged before Burn-In and after Burn-In at O.S.U.

Boards will be measured and debugged on computerized tester presently being designed and built at O.S.U.

Data Cables

- Cables are being assembled and tested by outside companies

9 m skew-clear cable tester
Material Safety

FE Board Cables

<table>
<thead>
<tr>
<th>Cable</th>
<th>Conductors</th>
<th>Insulation</th>
<th>Shield</th>
<th>Jacket</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE Board - FE Board</td>
<td>40</td>
<td>HF Polyolefin</td>
<td>none</td>
<td>none</td>
<td>3M</td>
</tr>
<tr>
<td>Chamber - FE Board</td>
<td>34</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>Amphenol</td>
</tr>
<tr>
<td>FE Board - Motherboard</td>
<td>25 pair</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>Amphenol</td>
</tr>
<tr>
<td>FE Board - CLCT</td>
<td>25 pair</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>HF FR Polyolefin</td>
<td>Amphenol</td>
</tr>
</tbody>
</table>

(all board and cable connectors have glass filled Polyester (PBT) rated UL 94-V0 as the insulator)

Following CMS Cable Colour Codes:
FE Board - Motherboard Cable will be **BLUE**

Date: Thu, 11 May 2000 08:58:49 +0200
From: Marc TAVLET <Marc.Tavlet@cern.ch>
Subject: Re: cable approval
To: LING@mps.ohio-state.edu
Cc: ron.pintus@cern.ch, Reiner.Schmidt@cern.ch, dgreen@fnal.gov, Alain.Herve@cern.ch

Dear Mr Ling,

Yes, I have received the information on the Amphenol/Spectra-Strip cable (Round, jacketed, 25 shielded parallel pairs, 28 AWG). The construction of the cable seems to be very good as regard to fire-resistance; the cable is rated IEC-332-3 which is ok. The proposed materials are halogen-free.

Also the PBT used for the connectors is rated UL 94-V0.

In conclusion, **this cable and connector are perfectly acceptable from a fire-safety point of view**. I approve their use.

Thanks for your collaboration.
Marc Tavlet
Ohio State University will maintain the FE Boards

10% Spare Boards will be Built

We anticipate swapping bad boards during accesses and fixing them.

Each board has a unique electronic serial number. Swaps can be monitored using software.

Cathode FE Board Meets All Design Specifications!

It is time to start procuring parts and begin manufacturing...