



## XC1700 and XC1800 Design Migration Considerations

XAPP161 September 28, 1999 (Version 1.0)

Application Note

### Summary

Designing a board with Xilinx PROMs is advantageous because migration between XC1700 and XC1800 series devices is simple. This application note discusses two migration paths: XC1700 designs upgrading to XC1800, and XC1800 designs migrating to XC1700 for production-stable cost reductions. The topics discussed are pin-out compatibility, power and ground connections, and boundary-scan chain integrity.

### Xilinx Family

XC1700E/L, XC1800

## Introduction

The XC1700 series of OTP (one-time programmable) configuration SPROMs is a popular choice for FPGA configuration. The XC1800 series of PROMs accommodates the serial download method of the XC1700 series along with Express and SelectMAP mode parallel-load innovations. The XC1800 devices also offer full IEEE Std 1149.1 boundary-scan (JTAG) support allowing in-system PROM programming and board level testing via the TAP port. In design environments where in-system re-programmability is a desired feature, the XC1800 series of PROMs is the best solution.

Upgrading from the XC1700 family to the XC1800 family is beneficial to system designers using the newer configuration modes, boundary-scan testing, or PROM re-programmability. The system designer may also choose to replace a XC1800 family device with a XC1700 device for production-stable cost reductions.

## Pin-out Compatibility

The XC1700 pin-out is a subset of the XC1800 pin-out for specific packages (Table 1). The footprint of a XC1700 device is not compatible with the XC1800 in a PLCC 20-pin package. All other available packages are compatible: VQFP 44-pin, PLCC 44-pin and SOIC 20-pin.

Table 1 shows all XC1800 specific pins (D7 to D1, VCCO, TCK, TMS, TDI, TDO,  $\overline{CF}$ ) corresponding to no-connect pins on XC1700 devices. These additional signals can be safely connected to the no-connect pins on a design using the XC1700.

The reset polarity on the XC1800 is active low and is not programmable. This will not be an issue when used with Xilinx FPGAs because the reset signal on Xilinx FPGAs is always active low.

## Power & Ground Connections

There are additional power and ground pins on XC1800 devices that correspond to no-connects on the XC1700. These pins (additional VCC, VCCO) can be safely connected to the no-connect pins on a XC1700 device.

The VPP pins on the XC1700 device correspond to the VCC pins on the XC1800. The VPP pin is the programming voltage pin for the XC1700 series and is connected to VCC for normal operation.

## Designing for Boundary-Scan Integrity

The XC1800 is designed for use in a boundary-scan chain with other JTAG-compliant devices. If PROM re-programmability is only required for development and is not necessary in volume production, the boundary-scan chain can be designed for eventual production cost savings by migrating to an OTP XC1700.

In the design example shown in Figure 1, there are three Xilinx devices: an FPGA, a CPLD, and a PROM. From one JTAG header on the board, both the PROM and the CPLD can be connected for in-system programming. Boundary-scan testing can also be performed from this header.

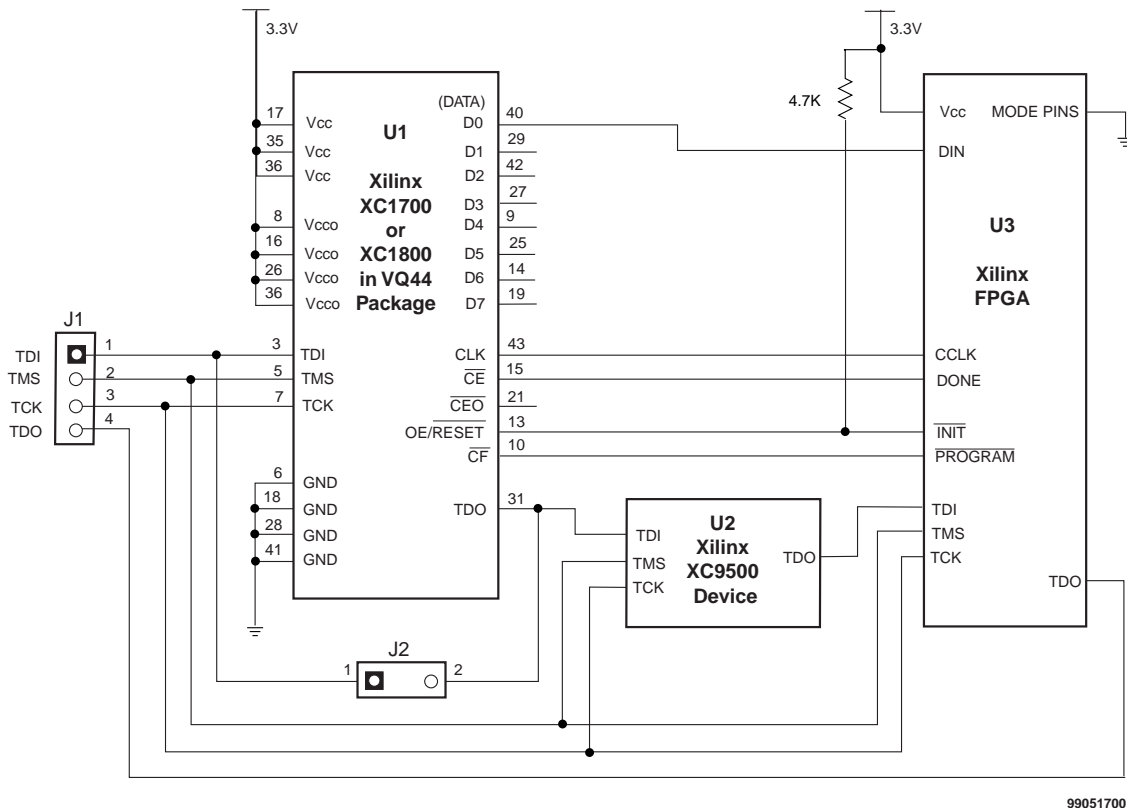
Jumper J2 is necessary in the design example to maintain the continuity of the boundary-scan chain when migrating between XC1800 and XC1700 devices. The jumper (J2) is connected between the TDI and TDO pins of the PROM footprint. This jumper is left open when the XC1800 is used and closed when the XC1700 is installed to preserve the boundary-scan chain.

If the designer plans to use the XC1800 but does not need to use the JTAG capabilities of the PROM, the TCK pin on the PROM can be connected to ground to prevent entering JTAG mode. The TDI, TDO, and TMS have internal 50K pull-ups, and can be left unconnected.

**Table 1: Pinout Comparison of XC1700 and XC1800**

Pin	XC1700 Pinout			XC1800 Pinout		
	VQ44	PC44	SO20	VQ44	PC44	SO20
1			DATA			D0/DATA
2		DATA			D0/DATA	D2
3		GND	CLK	TDI	GND	CLK
4					D2	TDI
5		CLK		TMS	CLK	TMS
6				GND		TCK
7				TCK		D4, CF <sup>1</sup>
8			OE/RESET	VCCO		OE/RESET
9				D4	TDI	D6
10			CE	CF		CE
11			GND		TMS	GND
12					GND	D7
13	OE/RESET		CEO	OE/RESET	TCK	CEO
14				D6	VCCO	D5
15	CE			CE	D4	D3
16				VCCO	CF	D1
17				VCC		TDO
18	GND		VPP	GND		VCC
19		OE/RESET		D7	OE/RESET	VCCO
20			VCC		D6	VCC
21	CEO	CE		CEO	CE	
22					VCCO	
23					VCC	
24		GND			GND	
25				D5	D7	
26				VCCO		
27		CEO		D3	CEO	
28				GND		
29				D1		
30						
31				TDO	D5	
32					VCCO	
33					D3	
34					GND	
35	VPP			VCC	D1	
36				VCCO		
37					TDO	
38	VCC			VCC		
39						
40	DATA			D0/DATA		
41	GND	VPP		GND	VCC	
42				D2	VCCO	
43	CLK			CLK		
44		VCC			VCC	

1. On 1801 and 18512, programmable for serial mode only.



99051700

Figure 1: Migration Design Example Using Master Serial Download Configuration

## Revision History

Date	Version	Revision
9/28/99	1.0	Initial Xilinx Release