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# Virtex Package Compatibility Guide

## Summary

This package compatibility guide describes the pinouts and established guidelines for package compatibility between the Virtex™ family and the Virtex-E and Virtex-E Extended Memory (Virtex-EM) devices. For the latest information regarding the Virtex-E families, see the Xilinx web site at <http://www.xilinx.com>.

## Introduction

The 1.8V Virtex-E and Virtex-EM families combine 0.18  $\mu\text{m}$  technology with a synthesis-friendly silicon architecture to provide a new level of FPGA performance and density. Package compatibility in the Virtex series allows systems to migrate from using Virtex devices to Virtex-E or Virtex-EM devices. Package pinout and pin functionality differences between the Virtex-E families and the Virtex family are covered in this document. The Virtex-EM devices are pin-for-pin compatible with Virtex-E devices in the same package.

## Virtex, Virtex-E, Virtex-EM Family Differences

### Power Supplies

As in the Virtex series, the Virtex-E families positive supply is divided into two separate power supplies,  $V_{\text{CCO}}$  and  $V_{\text{CCINT}}$ .  $V_{\text{CCO}}$  powers output pins and LVTTTL, LVCMOS, and PCI output and input pins.  $V_{\text{CCINT}}$  powers internal logic and all input pins except LVTTTL, LVCMOS, and PCI inputs. Virtex-E  $V_{\text{CCINT}}$  is 1.8V instead of the Virtex  $V_{\text{CCINT}}$  2.5V. This is a result of more advanced processing and 0.18  $\mu\text{m}$  design rules, which also offer reduced die size, reduced power consumption, and increased speed.  $V_{\text{CCO}}$  is adjustable up to 3.3V, depending on the I/O standard used. See [Table 1](#) for supported I/O standards.

Voltage regulator modules with programmable output voltages can be used to power the  $V_{\text{CCO}}$  and  $V_{\text{CCINT}}$  inputs and accommodate the lower 1.8V  $V_{\text{CCINT}}$  in the Virtex-E families.

### I/O Standards Supported

Virtex-E devices can be used with 20 high-performance interface standards, including LVDS and LVPECL differential signalling standards. A new LVCMOS I/O standard based on 1.8V  $V_{\text{CCO}}$  is also supported. [Table 1](#) shows a complete listing. All I/O pins are 3V tolerant and can be 5V tolerant with an appropriate external resistor. PCI 5V is not supported.

### I/O Banking

There are eight I/O banks in the Virtex-E families, as in the Virtex family, and each bank has multiple  $V_{\text{CCO}}$  pins. All of the  $V_{\text{CCO}}$  pins in one bank must be connected to the same voltage level, as determined by the I/O standard in use.

In Virtex-E devices the banking rules are different because the input buffers with LVTTTL, LVCMOS, and PCI standards are powered by  $V_{\text{CCO}}$  instead of  $V_{\text{CCINT}}$ . For these standards, only input and output buffers that have the same  $V_{\text{CCO}}$  can be mixed together in the same bank.

Table 1: Supported I/O Standards

I/O Standard	Output $V_{CCO}$	Input $V_{CCO}$	Input $V_{REF}$	Board Termination Voltage ( $V_{TT}$ )
LVTTTL	3.3	3.3	N/A	N/A
LVC MOS2	2.5	2.5	N/A	N/A
LVC MOS18	1.8	1.8	N/A	N/A
SSTL3 I and II	3.3	N/A	1.50	1.50
SSTL2 I and II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III and IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS/LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

## Low Voltage Differential Signals

The Virtex-E families incorporates differential signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

$I/O\_L\#[P/N]$

where L= LVDS or LVPECL pin

# = Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the differential pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. [Table 2](#) defines the names and function of the different types of differential pin pairs in the Virtex-E families.

Table 2: Differential Pin Pairs

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general I/O or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general I/O or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general I/O or a synchronous input/output differential signal, or an asynchronous output differential signal (for all devices within the same package.)
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general I/O or a synchronous input/output differential signal, or a differential clock input signal or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

### Differential Clock Pins

In addition to the four GCLKs in the Virtex family, the Virtex-E families have four IO\_LVDS\_DLL pins that can be paired with GCLKs to support up to four differential clocks. A differential clock input pair always includes one GCLK and the adjacent IO\_LVDS\_DLL pin. The GCLK pin is always the positive input in differential clock input configurations.

When differential clocks are not in use, these IO\_LVDS\_DLL pins can be used as single-ended I/Os or as DLL input pins.

### DLL Input Pins

Four additional DLL input pins (IO\_LVDS\_DLL) can be used as inputs to the DLLs, for a total of eight usable inputs for DLLs in the Virtex-E families. This is very useful in clock mirroring applications.

## Pinout Differences Between the Virtex and Virtex-E Families

Equivalent Virtex-E, Virtex-EM and Virtex devices are pin-compatible (within the same package) with some minor exceptions listed in [Table 3](#).

### XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

### XCV300E Device, BG432 Package

The Virtex-E XCV300E has eight pins (B26, C7, F1, F30, AE29, AF1, AH8, and AH24) connected to  $V_{CCINT}$  that are no-connect in the Virtex XCV300.

### XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing. The same comparison is applicable for the Virtex-EM family (XCV405E.)

### All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have  $V_{CCO}$  banking, but Virtex-E and Virtex-EM devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146,

P116, P85, P55, and P25) are now  $V_{CCO}$  pins in the Virtex-E family. This change also requires one Virtex IO\_VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E devices caused some IO\_VREF differences in the XCV400E and XCV600E devices only. Virtex IO\_VREF pins P215 and P87 are Virtex-E IO\_VREF pins P216 and P86, respectively. Virtex-E pins P215 and P87 are now IO\_LVDS\_DLL.

**Table 3: Virtex-E Families Compared to Virtex Family Pinout Differences**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV300	BG432	B26, C7, F1, F30, AE29, AF1, AH8, and AH24	No Connect	$V_{CCINT}$
XCV400 XCV400E XCV405E	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/H Q240	P215, P87	IO_VREF	IO_LVDS_DLL
		P216, P86	I/O	IO_VREF
All	PQ240/H Q240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	$V_{CCO}$
		P231	I/O	IO_VREF

**Table 4: FG900 Package Compatibility Between XCV600E and XCV812E**

Pins	XCV600E	XCV812E
J1, F9, A7, C10, G12, A13, B18, D20, B21, C23, P23, C26, J25, H25, K30, M23, N23, T24, V24, Y27, AB27, Y21, AH26, AH23, AB19, AD19, AF19, AD14, AK12, AE12, AE10, AH8, AD8, Y10, AD1, AA4, V7, U6, N8, M7, L3, J4, J6	No Connect	I/O
A10	IO-L23-N-YY	IO-VREF-O-L23-N-YY
F19	IO-L45-P-YY	IO-VREF-1-L45-P-YY
L30	IO-L94-P-YY	IO-VREF-2-L94-P-YY
Y29	IO-L117-N-YY	IO-VREF-3-L117-N-YY
AK22	IO-L166-P-YY	IO-VREF-4-L166-P-YY
AJ12	IO-L188-N-YY	IO-VREF-5-L188-N-YY
Y5	IO-L236-N-YY	IO-VREF-6-L236-N-YY
M1	IO-L259-P-YY	IO-VREF-7-L259-P-YY

**Table 5: BG560 Package Compatibility**

Pins	XCV1000E	XCV812E
D29	IO-VREF-O-LOP	IO-LOP
E7	IO-VREF-1-L43-P-Y	IO-L43-P-Y
B3	IO-VREF-2-L46N	IO-L46N

Table 5: BG560 Package Compatibility (Continued)

Pins	XCV1000E	XCV812E
AH4	IO-VREF-3-L90N-Y	IO-L90N-Y
AN3	IO-VREF-4-L93N	IO-L93N
AK28	IO-VREF-5-L136N-Y	IO-L136N-Y
AH30	IO-VREF-6-L138P	IO-L138P
D31	IO-VREF-7-L182P-Y	IO-L182P-Y

Table 6: FG900 Package Compatibility Between XCV1000E and XCV812E

Pins	XCV1000E	XCV812E
VCCO_0	VCCO_0	No Connect
VCCO_1	VCCO_1	No Connect
VCCO_2	VCCO_2	No Connect
VCCO_3	VCCO_3	No Connect
C5, H24, G26, A25, F22, G20, L18, D16, J16, B17, J17, E19, L13, D13, C14, AA14, AJ13, AG12, AE15, AD18, AE18, AJ18, AK27, AD21, AD26, AA23, T29, T26, T22, V25, AB29, M25, M24, P30, AF10, AG9, AA11, AF6, J1, J3, F1, L10, T3, P9, N2, N10, T2, V1, T10, U7, AB7, AC5, C6	I/O	No Connect
A3	IO_VREF_0_L2N_Y	IO_L2N_Y
A9	IO_VREF_0_L16P	IO_VREF_0
G23	IO_VREF_1_L66P_Y	IO_L66P_Y
E28	IO_VREF_2_L73P_YY	IO_L73P
J30	IO_VREF_2_L87N_YY	IO_VREF_2
AG29	IO_VREF_3_L138N_YY	IO_L138N
AB21	IO_VREF_4_L145P_Y	IO_L145P_Y
AA18	IO_VREF_4_L159N	IO_VREF_4
AJ4	IO_VREF_5_L209N_Y	IO_L209N_Y
AC1	IO_VREF_6_L229P_YY	IO_VREF_6
AE3	IO_VREF_6_L215N_YY	IO_L215N
C2	IO_VREF_7_L280P_YY	IO_L280P
C4	IO_L0N_YY	No Connect
F7	IO_L0P_YY	I/O
B4	IO_L3N_Y	No Connect
J10	IO_L3P_Y	I/O
D9	IO_L14N	No Connect
C9	IO_L14P	I/O
E10	IO_L16N	No Connect
H12	IO_L18N_YY	No Connect
C10	IO_L18P_YY	I/O

**Table 6: FG900 Package Compatibility Between XCV1000E and XCV812E (Continued)**

<b>Pins</b>	<b>XCV1000E</b>	<b>XCV812E</b>
B11	IO_L21N_Y	No Connect
G12	IO_L21P_Y	I/O
B15	IO_L32N	No Connect
H15	IO_L32P	I/O
F15	IO_L33N_YY	I/O
D15	IO_L33P_YY	No Connect
D20	IO_L47N_Y	I/O
A20	IO_L47P_Y	No Connect
B21	IO_L50N_YY	I/O
D21	IO_L50P_YY	No Connect
C26	IO_L65N_Y	I/O
F23	IO_L65P_Y	No Connect
B28	IO_L68N_YY	I/O
A28	IO_L68P_YY	No Connect
C29	IO_L71P	No Connect
D28	IO_L71N	I/O
K22	IO_L74P	No Connect
F27	IO_L74N	I/O
K26	IO_L85P_YY	No Connect
J28	IO_L85N_YY	I/O
K27	IO_L87P_YY	No Connect
K28	IO_L89P_YY	I/O
L25	IO_L89N_YY	No Connect
L29	IO_L92P	No Connect
M23	IO_L92N	I/O
R21	IO_L103P_YY	No Connect
R28	IO_L103N_YY	I/O
P24	IO_L105P_YY	No Connect
R27	IO_L105N_YY	I/O
V24	IO_L119P	I/O
Y28	IO_L119N	No Connect
Y27	IO_L122P	I/O
W23	IO_L122N	No Connect
AG30	IO_L137P	I/O
AC25	IO_L137N	No Connect
AF28	IO_L140P	I/O
AD25	IO_L140N	No Connect
AG26	IO_L143P_YY	No Connect

Table 6: FG900 Package Compatibility Between XCV1000E and XCV812E (Continued)

Pins	XCV1000E	XCV812E
AH27	IO_L143N_YY	I/O
AC22	IO_L146P_Y	No Connect
AH26	IO_L146N_Y	I/O
AK24	IO_L157P	No Connect
AD20	IO_L157N	I/O
AH22	IO_L159P	No Connect
AH21	IO_L161P_YY	No Connect
AD19	IO_L161N_YY	I/O
AC18	IO_L164P_Y	No Connect
AF19	IO_L164N_Y	I/O
AD15	IO_L175P	No Connect
AH17	IO_L175N	I/O
AC15	IO_L178P_YY	No Connect
AG15	IO_L178N_YY	I/O
AK12	IO_L190P_Y	I/O
Y13	IO_L190N_Y	No Connect
AE12	IO_L193P_YY	I/O
AG10	IO_L193N_YY	No Connect
AD8	IO_L208P_Y	I/O
AK5	IO_L208N_Y	No Connect
AH5	IO_L211P_YY	I/O
AG3	IO_L211N_YY	No Connect
AH2	IO_L213N	No Connect
AG2	IO_L213P	I/O
AB8	IO_L216N	No Connect
AD6	IO_L216P	I/O
AA5	IO_L227N_YY	No Connect
W10	IO_L227P_YY	I/O
Y7	IO_L229N_YY	No Connect
AA2	IO_L231N_YY	I/O
U10	IO_L231P_YY	No Connect
AA1	IO_L234N	No Connect
V7	IO_L234P	I/O
R9	IO_L245N_YY	No Connect
T6	IO_L245P_YY	I/O
R5	IO_L248N_YY	I/O
R6	IO_L248P_YY	No Connect
M7	IO_L261N	I/O

Table 6: FG900 Package Compatibility Between XCV1000E and XCV812E (Continued)

Pins	XCV1000E	XCV812E
L5	IO_L261P	No Connect
L3	IO_L264N	I/O
M10	IO_L264P	No Connect
D1	IO_L279N	I/O
H7	IO_L279P	No Connect
D3	IO_L282N_YY	No Connect
K10	IO_L282P_YY	I/O

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
9/23/99	1.0	Initial Xilinx release
11/12/99	1.1	Revised I/O Standards supported on page 1.
3/21/00	1.2	Addition of Virtex-EM family compatibility
6/20/00	1.3	Add BG560 and FG900 compatibility