IBL & nSQP Opto-board Test Procedure

Prepared by:	*Checked by:*	*Approved by:*
K.K. Gan, H.Kagan, R.D. Kass, J. Moore, D.S. Smith, B. Tar, Yi Yang		

Distribution List

Atlas Collaboration for comments

History of Changes

Rev. No.	*Date*	*Pages*	*Description of changes*
1	3/12/2012	All	First Revision
2	5/25/2019		Minor wording update

Table of Contents

1. Introduction

The opto-board test procedure is meant to verify the complete functionality of all of the DORIC/PIN and VDC/VCSEL pairs on each opto-board. As a part of this verification, a burn in and thermal cycling of each board is completed prior to making detailed QA measurements. Our QA test setup allows us to measure the recovered data and clock (TTC) bit error rate for a given PIN current, the bit error rate on the transmitted data (DTO), and it allows for the characterization of both the LVDS outputs of the DORICs and the optical outputs of the VCSELs driven by the VDCs.

2. Test System

The opto-board QA test system, shown in Fig. 1, contains 24 independent pattern generating and error detecting channels for performing bit error rate tests (BERT) on a maximum of eight TTC links and 16 DTO links on an opto-board. The system is capable of sending the 8 TTC signals at 40 Mb/s over a fiber ribbon to the opto-board using a commercial VCSEL driver chip (IPtronics IPVD3X4) and VCSEL array (Finisar V850-2093-001). The system is also capable of receiving 16 optical DTO signals from an opto-board at 160 Mb/s using two commercial optical receiver chips (IPtronics IPTA3X4) and PIN arrays (ULM ULMPIN-04-TN-U0112U). A relay matrix is included to allow re-routing of the DORIC recovered data and clock LVDS to an oscilloscope for characterization. The BERT channels and control logic are generated by a Xilinx Spartan 6 FPGA housed on a commercial FPGA module from Opal Kelly Incorporated (XEM6001). Through a USB interface a LabVIEW program controls the FPGA and in turn the operation of the main QA board. Each BERT channel can independently generate various patterns of test bit strings, including a pseudo-random bit sequence (PRBS) to emulate conditions in the experiment. The generated pattern for the TTC is bi-phase mark (BPM) encoded and converted into an optical signal transmission via a fiber to the PIN. The DORIC decodes the electrical signal from the PIN to extract the clock and command LVDS signals. Each recovered LVDS signal is fed into the FPGA or to the relay matrix for BERT or analog measurements. To test the DTO channels, a pattern is sent via LVDS to the VDC on the opto-board. The VDC then converts this signal to one that is appropriate to drive a VCSEL. These optical signals are then sent back to the PIN arrays and receiver chips on the main QA board. The system then compares the received and generated signals to search for bit errors.

For the QA, all measurements are performed with a VDC/DORIC supply voltage (VVDC) of 2.5 V, a PIN bias voltage of +5 V, and an I_{set} of 2.0 mA per VDC chip (this corresponds to 10 mA in each VCSEL channel). These quantities are adjustable if desired. During the burn-in and thermal cycling, the boards are operated under normal conditions with a 40 Mb/s PRBS signal being sent to the PINs/DORICs and a 160 Mb/s signal transmitted to the VDCs/VCSELs. The environmental chamber is connected to a nitrogen line at 20 psi input pressure to prevent condensation. Nitrogen flows at all times during the tests. All QA measurements are recorded on the opto-board QA data sheet. These measurements will be posted on the web and linked to the production data base (PDB).

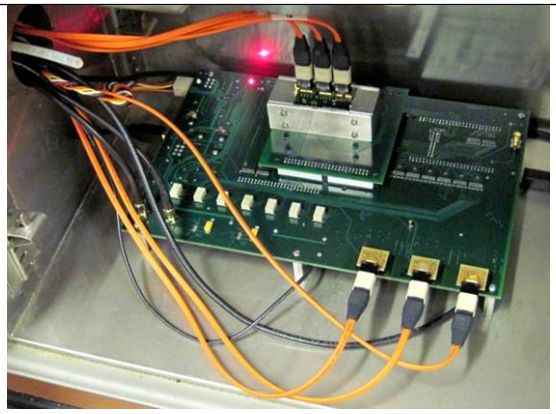

Figure 1: QA test board with fibers and opto-board attached.

2.1 Apparatus

The following is a list of apparatus needed for the testing:

- opto-board QA system
- +10 V power supply @ 1 A
- -10 V power supply @ 100 mA
- three MPO-MPO fibers (50 μm GRIN)
- three MPO-ST fan-out fibers (50 μm GRIN)
- DC opto-meter to measure optical power
- optical probe and scope to measure optical rise and fall times

3. Steps in the Opto-Board Test Procedure

The following is a summary of the major steps in the opto-board test procedure:

3.1 Basic functionality test after wire bonding (room temperature)

- Set I_{set} to 2 mA
- Set I_{PIN} on all TTC links to 100 μA (pk-pk)
- Measure the VVDC supply current
- Check for error free operation on all links
- Measure the optical power on all DTO
- If all pass, encapsulate wire bonds

3.2 Burn-in at 50ºC (ambient) for 72 hours

- Set I_{set} to 2 mA
- Set I_{PIN} on all TTC links to 100 μA (pk-pk)
- Measure the VVDC supply current
- Check for error free operation on all links
- Ensure nitrogen purge is active
- Set oven to 50°C
- Run for 72 hours

3.3 Thermal cycling: 0°C to +50°C (ambient)

- Set I_{set} to 2 mA
- Set I_{PIN} on all TTC links to 100 µA (pk-pk)
- Measure the VVDC supply current
- Check for error free operation on all links
- Ensure nitrogen purge is active
- Activate the oven thermal cycling program
- Thermal cycle the opto-board ten times between 0° C and +50° C with a soak of one hour at each 50° C point. The duration of each cycle is 2.0 hours.

3.4 Opto-board QA Procedure at 10°C (ambient)

The following is a list of the individual steps in the QA test:

1) Mount the opto-board onto the QA interface board
2) Clean the MPO connectors on the QA test board with a cotton swab and ethanol
3) Insert the MPO fibers into the optical connectors on the opto-board
4) Activate the powering
   a. +2.5 V for VVDC
   b. +5 V for VPIN
   c. I_{set} of 2 mA (0.5 mA per VDC).
   d. Check to make sure that the current consumption of VVDC is in range
5) Measure the total dark current of the PIN array
   a. Send no light to all channels in the PIN array
   b. Measure the PIN current
6) Set the input current to 100 µA for all channels in the PIN array
7) Initialize the DORICs
   a. Set the test system to generate 20 MHz BPM signals (all low commands) for all channels
   b. Send a reset signal for 10 µs to the opto-board
8) Check that all channels operate error free
   a. Set the test system to generate 40 Mb/s PRBS BPM signals on all TTC channels
   b. Set the test system to generate 160 Mb/s PRBS signals on all DTO channels
   c. Verify that all channels work with no bit errors for 30 seconds
9) Measure the current consumption of the VVDC power supply
10) Perform electrical characterization on all recovered TTC clock and data LVDS lines
   a. Repeat step 6 but set the PIN current to 50 µA for each channel in the PIN array
   b. Measure the LVDS recovered clock duty cycle
   c. Measure the LVDS recovered clock jitter
   d. Repeat steps a-c for the PIN current of 1000 µA
   e. Repeat step 6 to set the PIN current to 100 µA for each channel in the PIN array
   f. Measure the rise time of the LVDS recovered clock and data
   g. Measure the fall time of the LVDS recovered clock and data

h. Measure the LVDS recovered clock and data amplitude and common mode voltages

11) Perform the optical measurements for all channels

a. Send 40 MHz signals to all DTOs
b. Disconnect the opto-board DTO MPO fibers from the QA board receiver MPO fibers
c. Connect the opto-board DTO MPO fibers to the MPO-ST fan out
d. Clean the ST connectors with a cotton swap and ethanol
e. For each DTO, plug the ST connector into the opto-meter and measure the optical power (because of the 40 MHz, multiply the result by a factor of two to get the actual power)
f. For each DTO, connect the ST connector into the oscilloscope optical probe and measure the optical rise and fall times

12) Perform extended bit error rate tests at PIN currents of 50 and 1000 μA

a. Repeat step 6 to set the PIN current to 50 μA for each channel in the PIN array
b. Set the test system to generate 40 Mb/s PRBS BPM signals on all TTC channels
c. Set the test system to generate 160 Mb/s PRBS signals on all DTO channels
d. Verify that all channels work with no bit errors for 1 hour
e. Repeat steps a-d for the PIN current of 1000 μA