EndCap Muon CSC

Triggering, TTC, and Buffering Issues 15 June, 1999

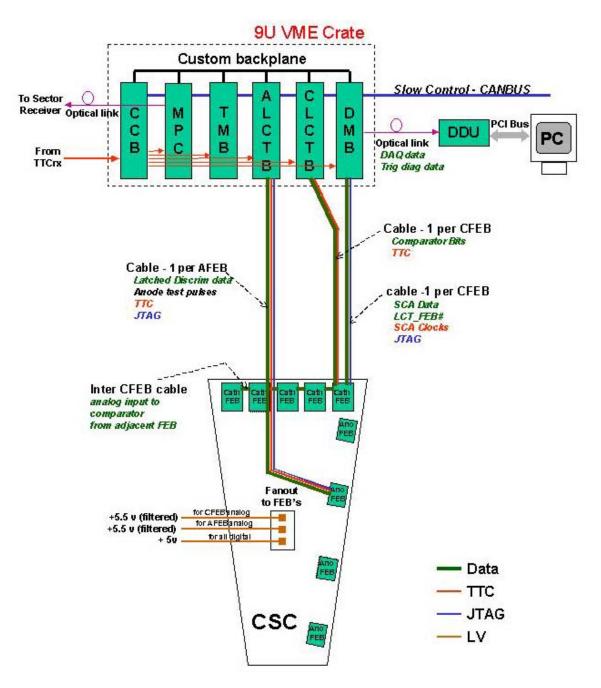
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Fundamentals

Electronics on CSC:





<u>CSC Buffering occurs in 2 places:</u>

1. DAQ Motherboard (DMB)

- 4 5 CFEB/DMB
- 16-bit X 16k FIFO per CFEB
- Typical CFEB event: ~800 Words
- **2. DDU**
 - Single 16-bit X 64k FIFO
 - 8 time samples per event
 - Average event: ~1k Words
 - FIFOs have programmable "almost empty" and "almost full"
 Trigger Throttle System?

Entire system holds ~85 Events • With L1Acc & Local Charged Track



Distribution

- 1. Clock & Control Board in VME crate: TTCRx to DMB, ALCT, CLCT, ...
- 2. DMB distributed TTC Signals to FEBs
- 3. DDU also needs signals for independant counters

Signals to be Used

- Global Reset
- **BC0**
- Clock

How much checking is enough?

- "Original" on CFEB
- Check on DDU! Also check on DMB?



L1Acc with LCT Rate: 600 Hz/CFEB

- L1Acc rate: 100 kHz
- LCT Rate: 60 kHz/CFEB, from "conservative" 300 kHz/chamber
- Estimate worst time slop: 100 ns
- 100 KHz x 60 kHz X 100ns = 600 Hz

Switched Capacitor Array (Buffer) Size

- Preamp output is continiously sampled at 20 MHz
- 96 time samples (SCA cells)/channel are grouped into 12 blocks of 8 cells
- 2 blocks must be saved to sample any 8 consecutive time samples
- A block is released when

 no LCT is found (400 ns)
 LCT, but no L1Acc (3 μs)
 sample is digitized (19.2 μs)



SCA Utilization:

- From the LCT rate, OVER 99% of the time, only 4 SCA blocks are in use
- During digitization, 2 of the remaining 8 blocks are held for the 19.2 μ s
- This leaves 6 blocks: room for 3 additional L1Acc with LCT
- Averageprobability of another L1Acc with LCT is

 $x = 600 Hz \times 19.2 \mu s = 0.0115$

Probability of 4 or more L1Acc+LCT is:

$$P = 1 - \sum_{n=0}^{3} \frac{x^n e^{-x}}{n!} = 7.2 \times 10^{-10}$$

- Equivalent to ~0.04 lost events per CFEB per 24 hours of running!
- IF it happens, just send an empty tagged error event
- No "almost full" warning available