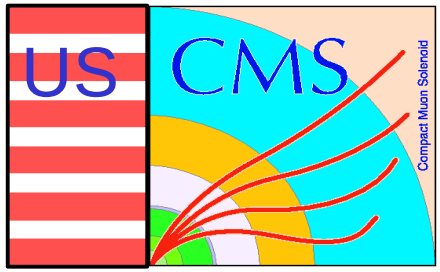
EMU DDU/FED Status



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CMS Week Meetings, CERN

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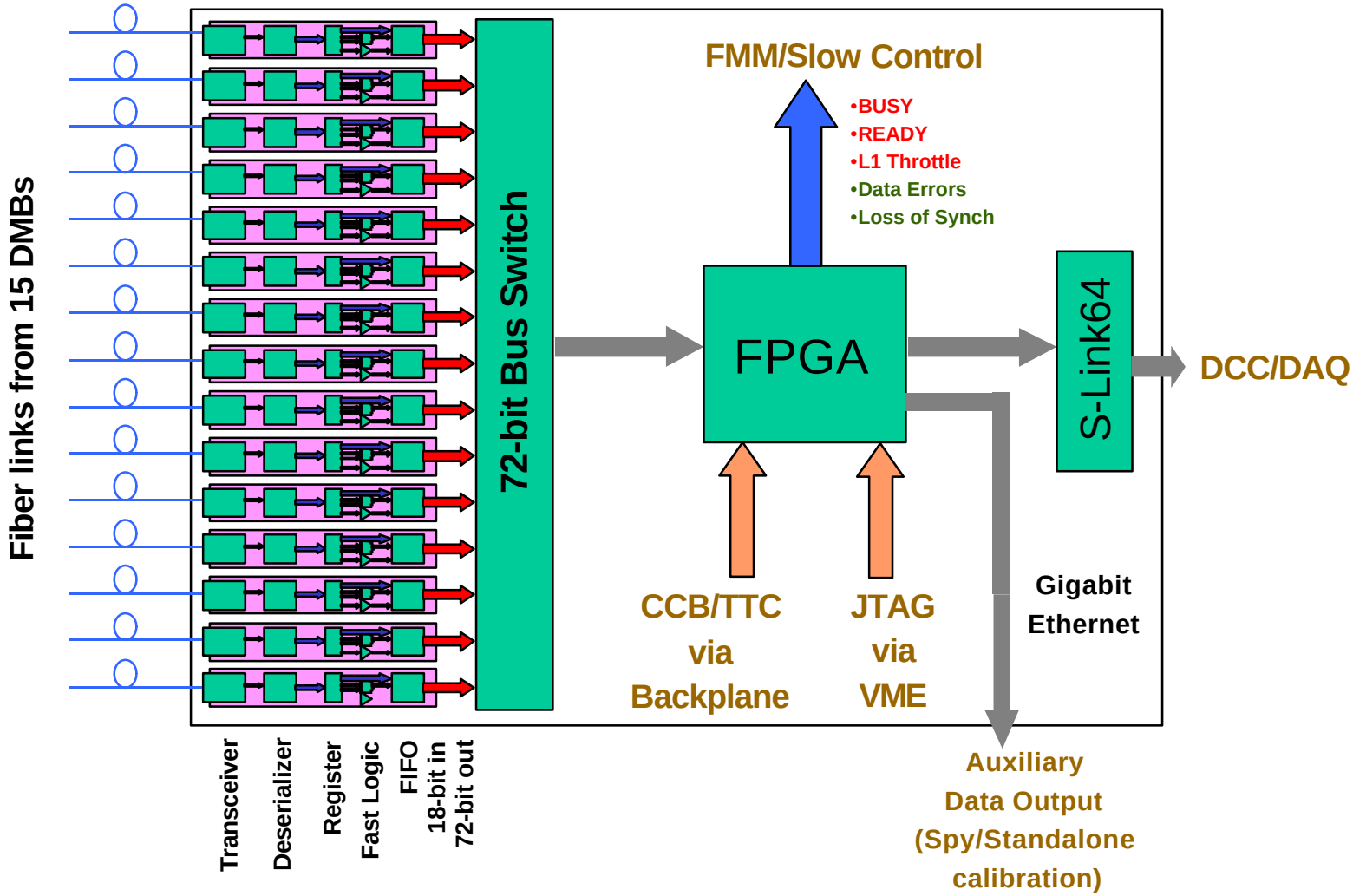
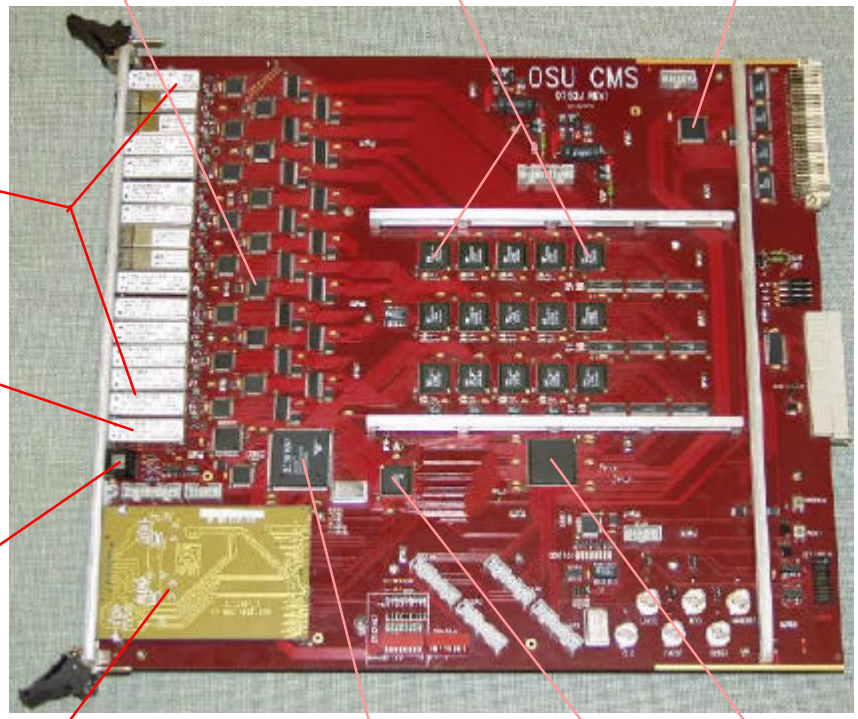
DDU Functions

- **What does the DDU do?**
  - High-Bandwidth data concentration
    - 15 DMB ⇨ 1 S-Link64, capable of continuous 640 MB/sec rate
  - Full error checking and status monitoring
    - CRC check, word count, event number, overflow, link status
  - FMM communication path for EMU DAQ
- **Current DDU Prototype Tests**
  - 15 DMB inputs via fiber link, up to 160 MB/sec each
  - Full error checking implemented
  - Interface to Slow Control (via VME/Dynatem)
  - PC data readout via Gigabit Ethernet (spy/calibration data path)
  - DMB calibration pulse tests, regular and random timing
  - 90 MB/sec data transfer rate via Gigabit Ethernet
    - Limited by PC memory and ~20 MB/sec hard drive access
  - FEDkit/S-Link tests successful, handles 640 MB/sec burst output

DDU Design


Fiber links from 15 DMBs
72-bit Bus Switch
FMM/Slow Control
•BUSY
•READY
•L1 Throttle
•Data Errors
•Loss of Synch
FPGA
S-Link64
DCC/DAQ
CCB/TTC via Backplane
JTAG via VME
Gigabit Ethernet
Auxiliary Data Output (Spy/Standalone calibration)
Transceiver
Deserializer
Register
Fast Logic
FIFO 18-bit in 72-bit out

DDU Prototype Board



De-serializer *(TLK2501)*

64 KB **FIFOs (15 total)**

VME CPLD *XILINX 9572XL*

15 Optical fiber inputs

Gbit Ethernet Output *To Standalone DAQ*

FMM output port

SLINK Mezzanine board

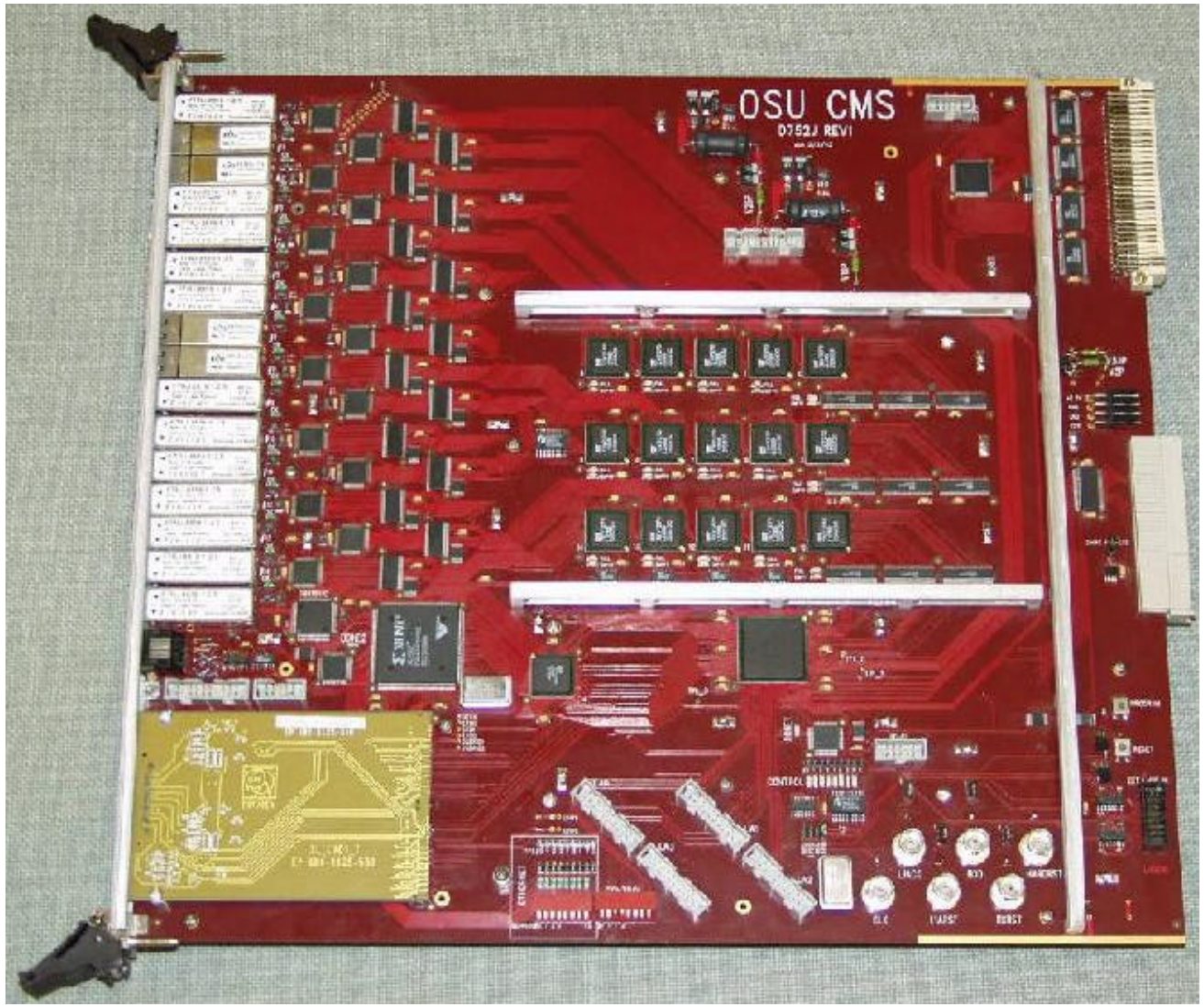
512 KB **FIFO**

Gbit Ethernet FPGA *XILINX Virtex 50E*

DDU Control FPGA *XILINX Virtex 600E*

- ✓ **Full error checking implemented**
- ✓ **Interface to VME**
- ✓ **PC readout via Gigabit Ethernet (90 MB/s data transfer)**
- ✓ **Tested DMB calibration pulses, regular and random timing**
- ✓ **S-Link64/FED Kit tested up to 640 MB/sec bursts**
- – **Need to integrate with FMM and TTS**

DDU Prototype Pic



DDU: Current and Future

- **Current DDU Design**
  - ✓ Full 15 DMB input prototype, 17 ball-grid arrays!
    - NO ball-grid problems out of ~4800 ball-grid solder joints
  - ✓ Implemented Slow Control support via VME
  - ✓ Gigabit Ethernet readout for spy data/standalone calibration
  - ✓ S-Link64 readout tested
  - – FMM communication port (LVDS via RJ45): not tested yet
- **Next DDU Prototype (2003?)**
  - – Faster FIFOs: gives more time, simplifies control scheme
  - – Add one CPLD on each input (15 total)
    - replaces discrete input logic, so cost increase is minimal
    - improves communication and control capabilities
    - adds flexibility for future protocol changes
  - – Put all VME control logic into a separate FPGA
    - frees up I/O pins for other uses…
  - – Implement two-way fiber communication
    - DMB-DDU and also DDU-DMB

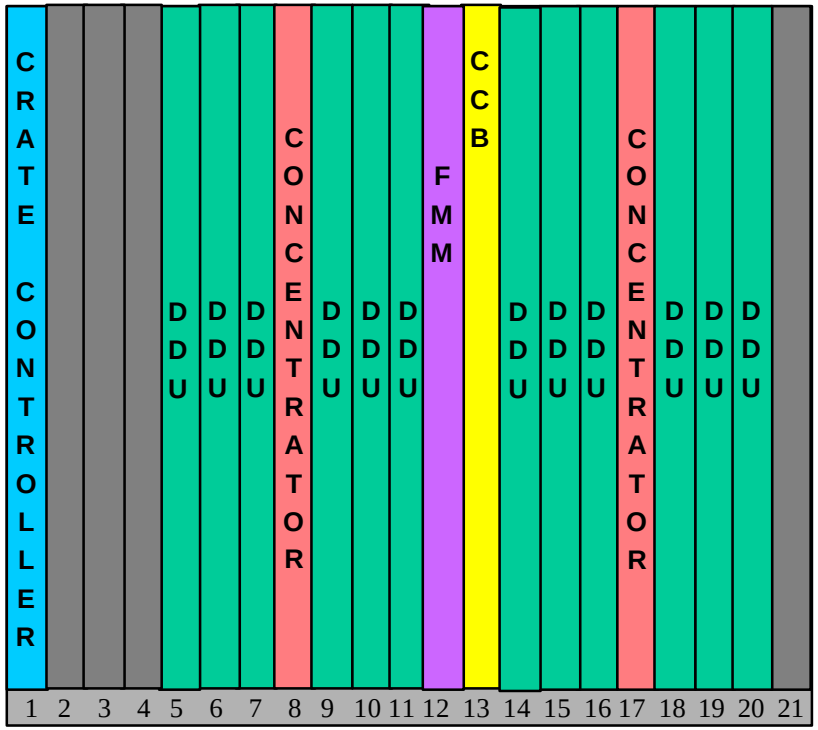
Other Concerns

- **Monitoring Issues**
  - **FMM and TTS**
    - **No FMM prototypes available yet...**
- **Readout Issues**
  - **Gigabit Ethernet data volume (calibration and spy data)**
    - **90 MB/s continuous data transfer (direct to memory, no processing)**
      - **Data analysis processes further reduce this rate**
    - **Data storage is SLOW: fastest disk only ~20 MB/s (SCSI Ultra 160)**
    - **4 GB RAM (current Linux limit) ⇨ ~45 seconds maximum storage**
    - **Calibration run may use ~12 GB per DDU * (2-3 DDUs per readout PC)**
    - **We need a fast storage solution! (closer to 90 MB/sec)**
  - **Data concentration for main DAQ readout**
    - **Bandwidth goal is 200 MB/sec average per readout link**
    - **One DDU averages 30 MB/sec**
    - **Need 6-to-1 concentration**
      - **build Data Concentrator Card...**

EMU DAQ Bandwidth

- **Three CSC Stations (no ME4)**
  - Expect 700 MB/sec data rate (due to minimum-bias events) at full LHC luminosity
  - Add ~50% to account for through-going muons in L1 triggers *(D. Acosta)*, gives total data rate of 1060 MB/s
  - S-Link capability is ~200 MB/s average per Readout Link
  - ➢ Need 6 Data Concentrator Cards (6-to-1 data merging)
- **Four CSC Stations (with ME4)**
  - Total CSC data rate increases to 1440 MB/s
  - ➢ Requires 9 Data Concentrator Cards (4-to-1 data merging)
- **Caveats**
  - The above quoted data rates are based on simulations using minimum-bias events. We won't know the data rate for sure until LHC turn-on.

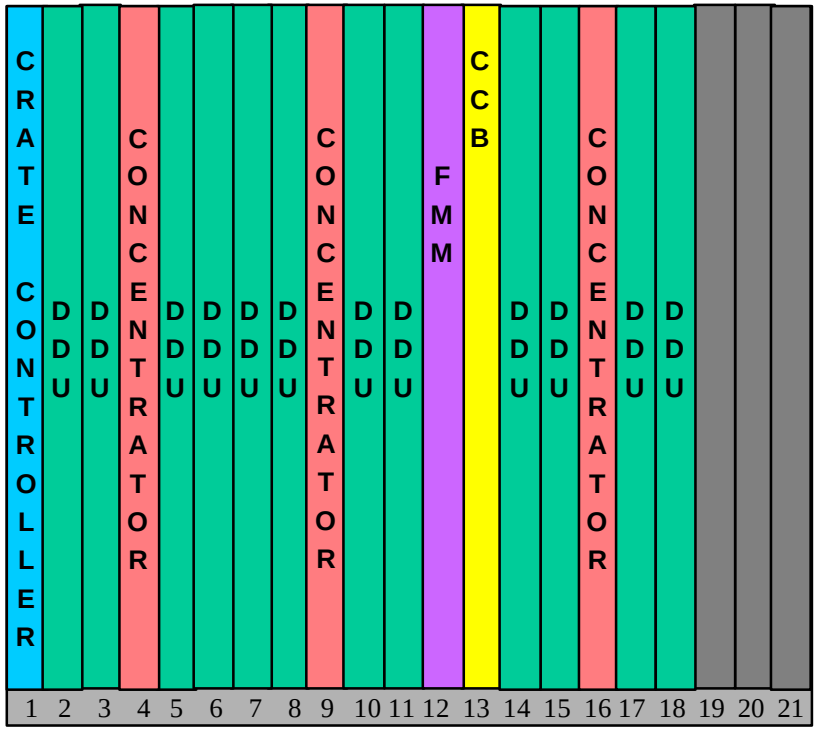
EMU DDU/FED Crate (1)



- Each of the 36 DDUs receive input from 15 DMBs
- EMU Readout needs 3 crates with 12 DDUs / crate
- Uses peripheral crate backplane and CCB
- Concentrator (DCC): 6 to 1 data merging
- FMM collects (from DDU)
  BUSY, READY, L1_Throttle
- Slow Control via controller

- **6 Data Concentrator Cards (DCC): 6-to-1 DDU concentration**
  - **Where does SR/SP DDU come into the DCC?**
- **Need 12-18 standalone PCs in nearby racks for calibration and spy data readout**

EMU DDU/FED Crate (2)

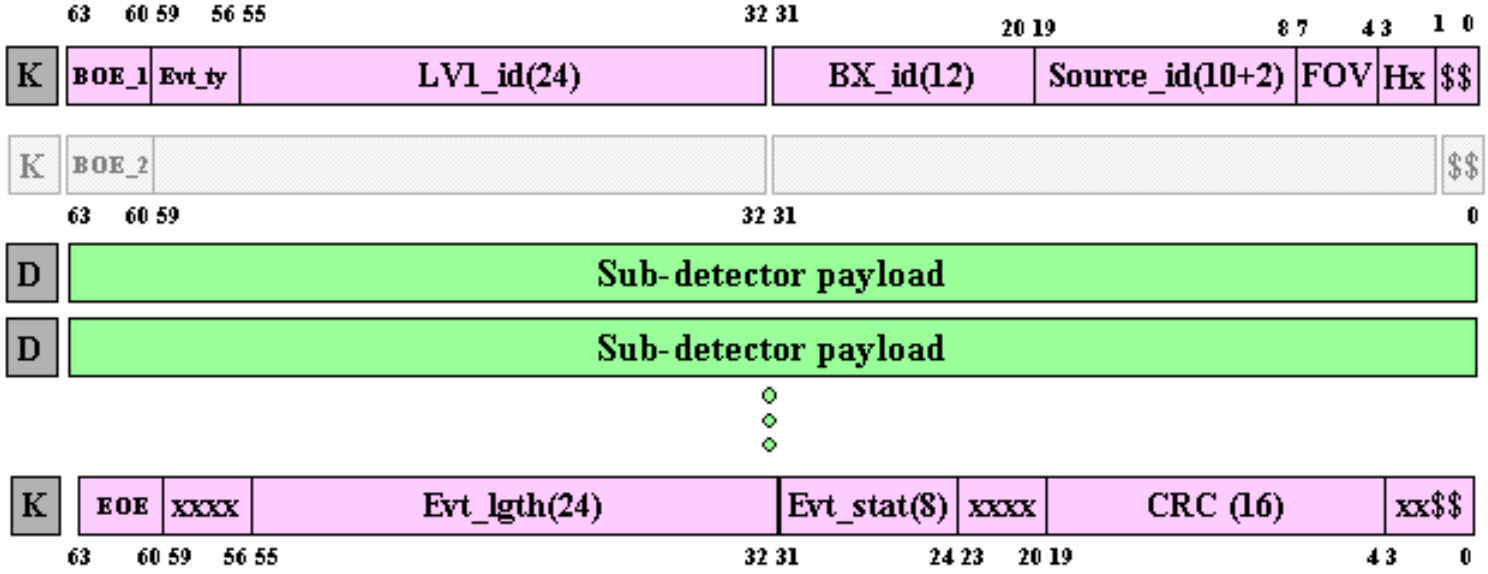


- Each of the 36 DDUs receive input from 15 DMBs
- EMU Readout needs 3 crates with 12 DDUs / crate
- Uses peripheral crate backplane and CCB
- Concentrator (DCC): 4 to 1 data merging
- FMM collects (from DDU) BUSY, READY, L1_Throttle
- Slow Control via controller

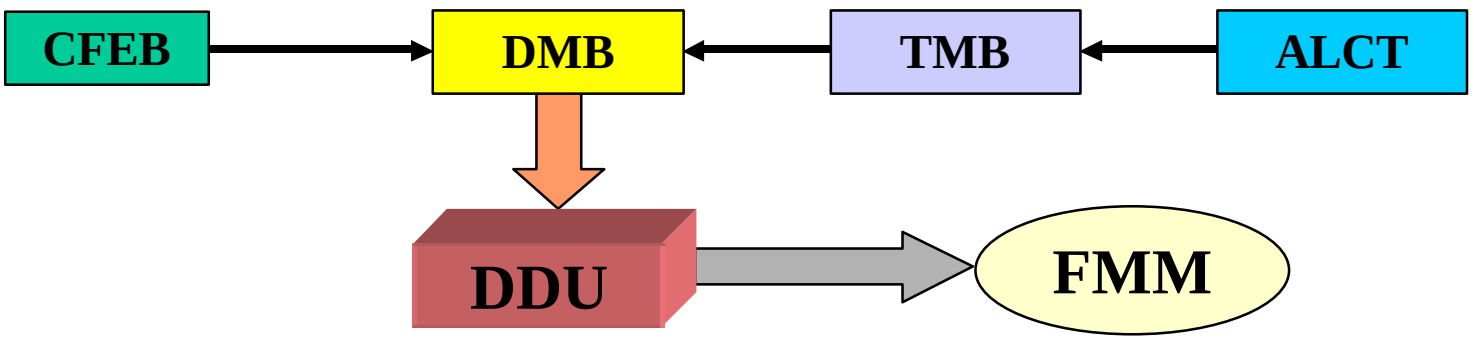
- **9 DCC option: 4-to-1 concentration**
  - **Where does SR/SP DDU come into the DCC?**
- **Need 12-18 standalone PCs in nearby racks for calibration and spy data readout**

EMU DDU/FED Data Format

- **S-Link64 Format**
  - As specified in RUWG minutes, 4 Dec. 2001
  - 1 Header and 1 Trailer with K bit set
- **EMU Detector Payload**
  - 2 DDU words, followed by CSC data (up to 15 DMB packets)
    - See http://www.physics.ohio-state.edu/~gilmore/cms/DDUformat.html
  - 2 more DDU status words after last DMB packet



EMU Status/FMM Communication



- **EMU DAQ Communicates to FMM via DDU**
  - Peripheral crate status gets to DDU via DMB fiber
  - CFEBs go to DMB
  - ALCT goes through TMB, and both go to DMB
  - Exact protocol not yet defined, but many options exist
  - Ready/Busy, Warning, Error, and Sync Loss can be implemented
- **MPC via Level 1 SR/SP system?**

FED Kit Experience

- **Few minor problems**
  - Start-Stop S-Link transmission problems
    - > Fixed in G-III firmware!
  - Byte-Blaster connection not polarized…it is in fact REVERSED!
    - > Very confusing; fix in next FED kit?
  - Problem with handling of clock interruptions
    - > Fixed in next FED Kit
  - PC occasionally hangs after several thousand events
    - > Requires installation of Linux kernel fix for memory handling
      - » Not done yet… but does not prevent further testing
- **FED Kit/S-Link tests successful!**
  - Handles 640 MB/sec burst output
  - FED Kit readout integrated into latest OSU DAQ